PHILIPS

Data handbook

Electronic
components
and materials

Integrated circuits

Part 1 January 1983

Bipolar ICs for radio and audio equipment

INTEGRATED CIRCUITS

PART 1 - JANUARY 1983

BIPOLAR ICs FOR RADIO AND AUDIO EQUIPMENT

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DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, subassemblies and materials; it is made up of four series of handbooks each comprising several parts.

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

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ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks is comprised of the following parts:

T1	**Tubes for r.f. heating**
T2	**Transmitting tubes for communications**
T3	**Klystrons, travelling-wave tubes, microwave diodes**
ET3	**Special Quality tubes, miscellaneous devices** (will not be reprinted)
T4	**Magnetrons**
T5	**Cathode-ray tubes** Instrument tubes, monitor and display tubes, C.R. tubes for special applications
T6	**Geiger-Müller tubes**
T7	**Gas-filled tubes** Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories
T8	**Picture tubes and components** Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display
T9	**Photo and electron multipliers** Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates
T10	**Camera tubes and accessories, image intensifiers**
T11	**Microwave components and assemblies**

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks is comprised of the following parts:

S1 **Diodes**
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes(< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2 **Power diodes, thyristors, triacs**
Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs

S3 **Small-signal transistors**

S4 **Low-frequency power transistors and hybrid IC modules**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Microminiature semiconductors for hybrid circuits**

S8 **Devices for optoelectronics**
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.

S9 Taken into handbook T11 of the blue series

S10 **Wideband transistors and wideband hybrid IC modules**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks is comprised of the following parts:

IC1	**Bipolar ICs for radio and audio equipment**
IC2	**Bipolar ICs for video equipment**
IC3	**ICs for digital systems in radio, audio and video equipment**
IC4	**Digital integrated circuits** LOCMOS HE4000B family
IC5	**Digital integrated circuits — ECL** ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs
IC6*	**Professional analogue integrated circuits**
IC7	**Signetics bipolar memories**
IC8	**Signetics analogue circuits**
IC9	**Signetics TTL logic**

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* This handbook will be available later this year.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks is comprised of the following parts:

C1	**Assemblies for industrial use** PLC modules, PC20 modules, HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices, hybrid ICs, peripheral devices
C2	**Television tuners, video modulators, surface acoustic wave filters**
C3	**Loudspeakers**
C4	**Ferroxcube potcores, square cores and cross cores**
C5	**Ferroxcube for power, audio/video and accelerators**
C6	**Electric motors and accessories** Permanent magnet synchronous motors, stepping motors, direct current motors
C7	**Variable capacitors**
C8	**Variable mains transformers**
C9	**Piezoelectric quartz devices** Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements
C10	**Connectors**
C11	**Non-linear resistors** Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
C12	**Variable resistors and test switches**
C13	**Fixed resistors**
C14	**Electrolytic and solid capacitors**
C15	**Film capacitors, ceramic capacitors**
C16	**Piezoelectric ceramics, permanent magnet materials**

FUNCTIONAL AND NUMERICAL INDEX
MAINTENANCE TYPE LIST

SELECTION GUIDE BY FUNCTION

type number	description	package code	pins
AM channels			
TDA1072	AM receiver circuit	SOT-38	16
TEA5550	AM car radio receiver circuit	SOT-38	16
TEA5570	AM/FM radio receiver circuit	SOT-38	16
FM channels			
TDA1571	balanced mixer/modulator/demodulator	SOT-38	16
TDA1576	FM/IF amplifier	SOT-102C	18
TEA5560	FM/IF system	SOT-142	9
TEA5570	AM/FM radio receiver circuit	SOT-38	16
TEA6000	FM/IF system and microcomputer-based tuning interface	SOT-102HE	18
AM/FM combined channels			
TBA570A	AM/FM radio receiver circuit	SOT-38	16
TBA570AQ	AM/FM radio receiver circuit	SOT-58	16
TDA1571	balanced mixer/modulator/demodulator	SOT-38	16
TDA5700	AM/FM radio receiver circuit	SOT-38	16
TDA5700Q	AM/FM radio receiver circuit	SOT-58	16
TEA5570	AM/FM radio receiver circuit	SOT-38	16
Stereo decoders			
TDA1005A	frequency multiplex PLL stereo decoder	SOT-38	16
TDA1005AT	frequency multiplex PLL stereo decoder	SOT-109A (SO-16)	16
TDA1578A	time multiplex PLL stereo decoder	SOT-102C	18
TEA5580	PLL stereo decoder	SOT-38	16
Interference suppressors			
TDA1001B	interference and noise suppression circuit for FM receivers	SOT-38	16
TDA1001BT	interference and noise suppression circuit for FM receivers	SOT-109A (SO-16)	16
Tuning circuits			
SAA1057	radio tuning PLL frequency synthesizer	SOT-102HE	18
SAA1300	tuner switching circuit	SOT-142B	9
TDA1580	automatic tuning circuit	SOT-102CS	18
TDA1584	memory converter for 4 presets	SOT-102C	18

SELECTION GUIDE BY FUNCTION (continued)

type number	description	package code	pins
D.C. controlled audio circuits			
TCA730A	d.c. volume and balance stereo control circuit	SOT-38	16
TCA740A	d.c. treble and bass stereo control circuit	SOT-38	16
TDA1028	signal-sources switch (2 x four channels)	SOT-38	16
TDA1029	signal-sources switch (4 x two channels)	SOT-38	16
TDA1074A	dual tandem electronic potentiometer circuit	SOT-102CS	18
TDA1524	stereo-tone volume control circuit	SOT-102CS	18
TDA1527	signal sources switch	SOT-142	9
Audio power amplifiers			
TDA1010A	6 W audio power amplifier in car and 10 W audio power amplifier in mains-fed applications	SOT-110B	9
TDA1011	2 to 6 W audio power amplifier	SOT-110B	9
TDA1011A	2 to 6 W audio power amplifier with inverted input/output	SOT-110B	9
TDA1013A	4 W audio power amplifier with d.c. volume control	SOT-110B	9
TDA1015	1 to 4 W audio power amplifier	SOT-110B	9
TDA1020	12 W car radio power amplifier	SOT-110B	9
TDA1510	24 W BTL or 2 x 12 W stereo car radio power amplifier	SOT-141B	13
TDA1512	12 to 20 W hi-fi audio power amplifier	SOT-131B	9
TDA1512Q	12 to 20 W hi-fi audio power amplifier	SOT-157B	9
TDA1515	24 W BTL or 2 x 12 W stereo car radio power amplifier	SOT-141B	13
TDA1520	20 W hi-fi audio power amplifier	SOT-131A	9
TDA2611A	5 W audio power amplifier	SOT-110B	9
Recorder (cassette) amplifiers/control circuits			
TDA1002A	recording and playback amplifier	SOT-38	16
TDA1012	recording/playback and 2 W audio power amplifier	SOT-38WE-2	16
TDA1016	recording/playback and 2 W audio power amplifier	SOT-38WE-2	16
TDA1508	auto-reverse car radio cassette deck steering circuit	SOT-102	18
TDA1522	stereo cassette head preamplifier and equalizer	SOT-142	9

type number	description	package code	pins
Motor speed control circuits			
TDA1006A	motor regulator with automatic tape-end indicator	SOT-38BE-2	16
TDA1059B	motor speed regulator with thermal shut-down	SOT-32	3
TDA1059C	motor speed regulator	SOT-32	3
TDA1506	motor regulator and function controller for car cassette systems	SOT-38	16
TDA1533	PLL motor speed control circuit for hi-fi applications	SOT-102C	18
TDA1559	motor speed regulator	SOT-32	3
Display drivers			
SAA1060	LED display/interface circuit	SOT-101A	24
SAA1062A	LCD display/interface circuit	SOT-117	28
SAA1062AT	LCD display/interface circuit	SOT-136A (SO-28)	28
SAA1063	fluorescent display/interface circuit	SOT-101A	24
TDA1594	display/driver circuit for 11 LEDs	SOT-102C	18
Miscellaneous			
OM200/S2	integrated amplifier for use in hearing aids	SOT-20	4
TAA263	low-level amplifier	SOT-18/17	4
TAA320	integrated MOSTamplifier	SOT-18/13	3
TAA320A	integrated MOST level sensor	SOT-18/13	3
TDA1008	gating/frequency divider for electronic musical instruments	SOT-38	16
TDA1540D	14-bit DAC with 85 dB S/N ratio	SOT-135A	28

NUMERICAL INDEX

type number	description	package code	pins
OM200/S2	integrated amplifier for use in hearing aids	SOT-20	4
SAA1057	radio tuning PLL frequency synthesizer	SOT-102HE	18
SAA1060	LED display/interface circuit	SOT-101A	24
SAA1062A	LCD display/interface circuit	SOT-117	28
SAA1062AT	LCD display/interface circuit	SOT-136A (SO-28)	28
SAA1063	fluorescent display/interface circuit	SOT-101A	24
SAA1300	tuner switching circuit	SOT-142B	9
TAA263	low-level amplifier	SOT-18/17	4
TAA320	integrated MOST amplifier	SOT-18/13	3
TAA320A	integrated MOST level sensor	SOT-18/13	3
TBA570A	AM/FM radio receiver circuit	SOT-38	16
TBA570AQ	AM/FM receiver circuit	SOT-58	16
TCA730A	d.c. volume and balance stereo control circuit	SOT-38	16
TCA740A	d.c. treble and bass stereo control circuit	SOT-38	16
TDA1001B	interference and noise suppression circuit for FM receivers	SOT-38	16
TDA1001BT	interference and noise suppression circuit for FM receivers	SOT-109A (SO-16)	16
TDA1002A	recording and playback amplifier	SOT-38	16
TDA1005A	frequency multiplex PLL stereo decoder	SOT-38	16
TDA1005AT	frequency multiplex PLL stereo decoder	SOT-109A (SO-16)	16
TDA1006A	motor regulator with automatic tape-end indicator	SOT-38BE-2	16
TDA1008	gating/frequency divider for electronic musical instruments	SOT-38	16
TDA1010A	6 W audio power amplifier in car and 10 W audio power amplifier in mains-fed applications	SOT-110B	9
TDA1011	2 to 6 W audio power amplifier	SOT-110B	9
TDA1011A	2 to 6 W audio power amplifier with inverted input/output	SOT-110B	9
TDA1012	recording/playback and 2 W audio power amplifier	SOT-38WE-2	16
TDA1013A	4 W audio power amplifier with d.c. volume control	SOT-110B	9
TDA1015	1 to 4 W audio power amplifier	SOT-110B	9
TDA1016	recording/playback and 2 W audio power amplifier	SOT-38WE-2	16
TDA1020	12 W car radio power amplifier	SOT-110B	9
TDA1028	signal-sources switch (2 x four channels)	SOT-38	16

type number	description	package code	pins
TDA1029	signal-sources switch (4 x two channels)	SOT-38	16
TDA1059B	motor speed regulator with thermal shut-down	SOT-32	3
TDA1059C	motor speed regulator	SOT-32	3
TDA1072	AM receiver circuit	SOT-38	16
TDA1074A	dual tandem electronic potentiometer circuit	SOT-102CS	18
TDA1506	motor regulator and function controller for car cassette systems	SOT-38	16
TDA1508	auto-reverse car radio cassette deck steering circuit	SOT-102	18
TDA1510	24 W BTL or 2 x 12 W stereo car radio power amplifier	SOT-141B	13
TDA1512	12 to 20 W hi-fi audio power amplifier	SOT-131B	9
TDA1512Q	12 to 20 W hi-fi audio power amplifier	SOT-157B	9
TDA1515	24 W BTL or 2 x 12 W stereo car radio power amplifier	SOT-141B	13
TDA1520	20 W hi-fi audio power amplifier	SOT-131A	9
TDA1522	stereo cassette head preamplifier and equalizer	SOT-142	9
TDA1524	stereo-tone volume control circuit	SOT-102CS	18
TDA1527	signal sources switch	SOT-142	9
TDA1533	PLL motor speed control circuit for hi-fi applications	SOT-102C	18
TDA1540D	14-bit DAC with 85 dB S/N ratio	SOT-135A	28
TDA1559	motor speed regulator	SOT-32	3
TDA1571	balanced mixer/modulator/demodulator	SOT-38	16
TDA1576	FM/IF amplifier	SOT-102C	18
TDA1578A	time multiplex PLL stereo decoder	SOT-102C	18
TDA1580	automatic tuning circuit	SOT-102CS	18
TDA1584	memory converter for 4 presets	SOT-102C	18
TDA1594	display/driver circuit for 11 LEDs	SOT-102C	18
TDA2611A	5 W audio power amplifier	SOT-110B	9
TDA5700	AM/FM radio receiver circuit	SOT-38	16
TDA5700Q	AM/FM radio receiver circuit	SOT-58	16
TEA5550	AM car radio receiver circuit	SOT-38	16
TEA5560	FM/IF system	SOT-142	9
TEA5570	AM/FM radio receiver circuit	SOT-38	16
TEA5580	PLL stereo decoder	SOT-38	16
TEA6000	FM/IF system and microcomputer-based tuning interface	SOT-102HE	18

MAINTENANCE TYPE LIST

The types listed below are not included in this handbook.
Detailed information will be supplied on request.

TBA700
TCA420A
TCA530
TCA750
TCA760B

TDA1001A;AT	successor type: TDA1001B;BT
TDA1003A	
TDA1004A	
TDA1010	successor type: TDA1010A
TDA1013	successor type: TDA1013A
TDA1074	successor type: TDA1074A

GENERAL

Type designation
Rating systems

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : Microcomputer
Central processing unit
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : –55 to + 125 °C
D : –25 to + 70 °C
E : –25 to + 85 °C
F : –40 to + 85 °C
G : –55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

PACKAGE OUTLINES

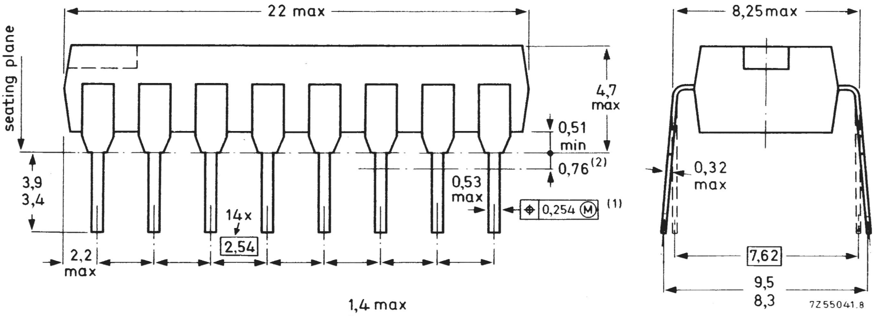
PACKAGE OUTLINES

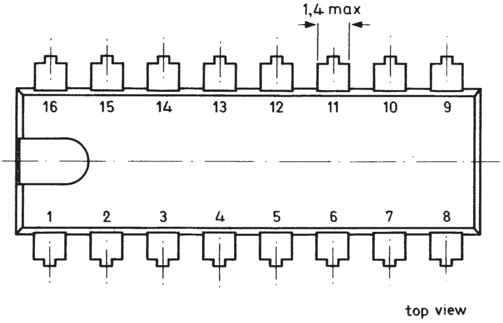
In this chapter the package outlines are given for the following types, except for those marked with an asterisk which are included in the device data sheet.

type number	package code	description
OM200/S2*		
SAA1057	SOT-102HE	18-lead dual in-line; plastic (SOT-102HE)
SAA1060	SOT-101A	24-lead dual in-line; plastic (SOT-101A)
SAA1062A	SOT-117	28-lead dual in-line; plastic (SOT-117)
SAA1062AT	SOT-136A	28-lead mini-pack; plastic (SO-28; SOT-136A)
SAA1063	SOT-101A	24-lead dual in-line; plastic (SOT-101A)
SAA1300	SOT-142B	9-lead single in-line; plastic (SOT-142)
TAA263*		
TAA320*		
TAA320A*		
TBA570A	SOT-38	16-lead dual in-line; plastic (SOT-38)
TBA570AQ	SOT-58	16-lead quadruple in-line; plastic (SOT-58)
TCA730A	SOT-38	16-lead dual in-line; plastic (SOT-38)
TCA740A	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1001B	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1001BT	SOT-109A	16-lead mini-pack; plastic (SO-16; SOT-109A)
TDA1002A	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1005A	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1005AT	SOT-109A	16-lead mini-pack; plastic (SO-16; SOT-109A)
TDA1006A	SOT-38BE-2	16-lead dual in-line; plastic power (SOT-38BE-2)
TDA1008	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1010A	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TDA1011	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TDA1011A	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TDA1012	SOT-38WE-2	16-lead dual in-line; plastic with internal heat spreader (SOT-38WE-2)
TDA1013A	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TDA1015	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TDA1016	SOT-38WE-2	16-lead dual in-line; plastic with internal heat spreader (SOT-38WE-2)
TDA1020	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TDA1028	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1029	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1059B*		
TDA1059C*		
TDA1072	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1074A	SOT-102CS	18-lead dual in-line; plastic (SOT-102CS)
TDA1506	SOT-38	16-lead dual in-line; plastic power (SOT-38)
TDA1508	SOT-102	18-lead dual in-line; plastic (SOT-102)
TDA1510	SOT-141B	13-lead SIL-bent-to-DIL; plastic power (SOT-141B)
TDA1512	SOT-131B	9-lead single in-line; plastic power (SOT-131A, B)

type number	package code	description
TDA1512Q	SOT-157B	9-lead SIL-bent-to-DIL; plastic power (SOT-157B)
TDA1515	SOT-141B	13-lead SIL-bent-to-DIL; plastic power (SOT-141B)
TDA1520	SOT-131A	9-lead single in-line; plastic power (SOT-131A, B)
TDA1522	SOT-142	9-lead single in-line; plastic (SOT-142)
TDA1524	SOT-102CS	18-lead dual in-line; plastic (SOT-102CS)
TDA1527	SOT-142	9-lead single in-line; plastic (SOT-142)
TDA1533	SOT-102C	18-lead dual in-line; plastic (SOT-102C)
TDA1540D	SOT-135A	28-lead dual in-line; ceramic (SOT-135A)
TDA1559*		
TDA1571	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA1576	SOT-102C	18-lead dual in-line; plastic (SOT-102C)
TDA1578A	SOT-102C	18-lead dual in-line; plastic (SOT-102C)
TDA1580	SOT-102CS	18-lead dual in-line; plastic (SOT-102CS)
TDA1584	SOT-102C	18-lead dual in-line; plastic (SOT-102C)
TDA1594	SOT-102C	18-lead dual in-line; plastic (SOT-102C)
TDA2611A	SOT-110B	9-lead single in-line; plastic (SOT-110B)
TDA5700	SOT-38	16-lead dual in-line; plastic (SOT-38)
TDA5700Q	SOT-38	16-lead quadruple in-line; plastic (SOT-58)
TEA5550	SOT-38	16-lead dual in-line; plastic (SOT-38)
TEA5560	SOT-142	9-lead single in-line; plastic (SOT-142)
TEA5570	SOT-38	16-lead dual in-line; plastic (SOT-38)
TEA5580	SOT-38	16-lead dual in-line; plastic (SOT-38)
TEA6000	SOT-102HE	18-lead dual in-line; plastic (SOT-102HE)

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)


22 max
seating plane
4,7
max
0,51
min
0,76(2)
3,9
3,4
0,53
max
0,254 Ⓜ (1)
14x
2,54
2,2
max
8,25max
0,32
max
7,62
9,5
8,3
7Z55041.8


1,4 max
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
top view

⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

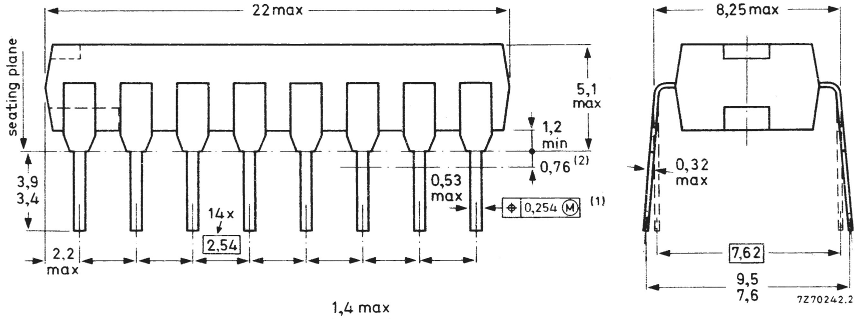
2. By dip or wave

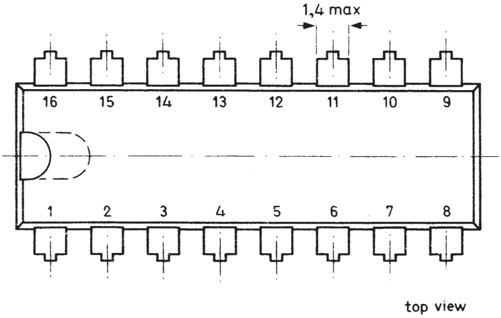
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC POWER (SOT-38BE-2)


22 max
seating plane
5,1
max
1,2
min
0,76 (2)
3,9
3,4
0,53
max
0,254 Ⓜ (1)
14x
2.54
2,2
max
8,25 max
0,32
max
7,62
9,5
7,6
7Z70242.2


1,4 max
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
top view

⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

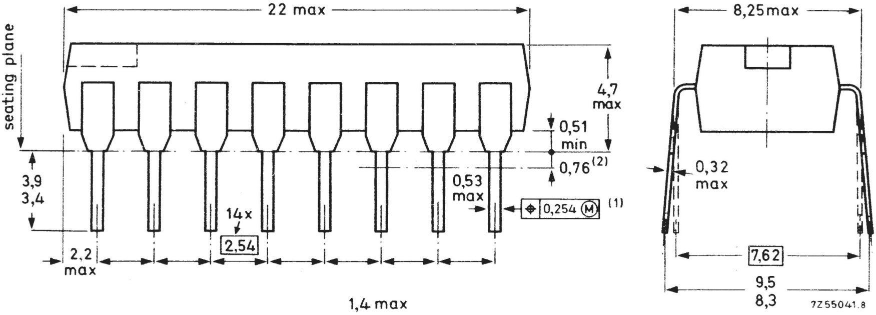
2. By dip or wave

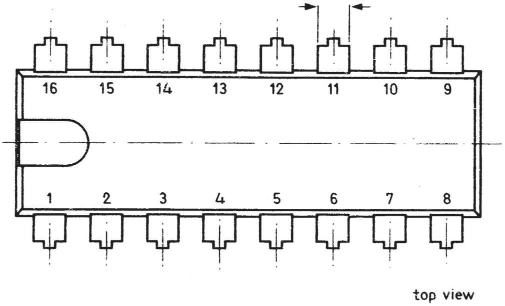
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT-38WE-2)


22 max
seating plane
4,7
max
0,51
min
0,76 (2)
3,9
3,4
0,53
max
14x
2,54
0,254 M (1)
2,2
max
8,25 max
0,32
max
7,62
9,5
8,3
7Z55041.8
1,4 max


16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
top view

⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

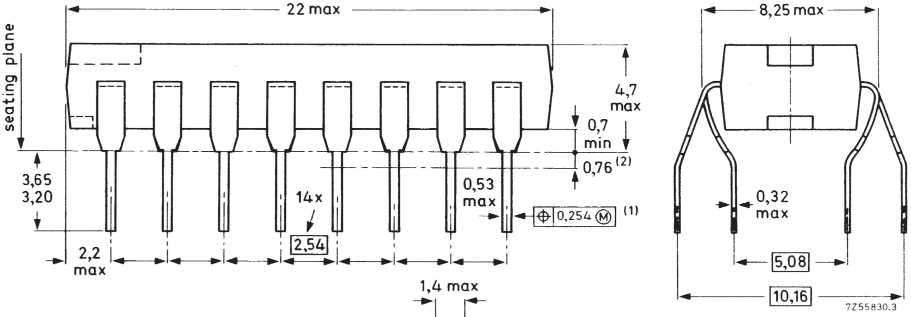
2. By dip or wave

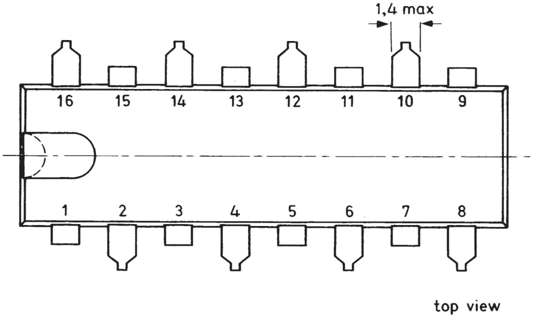
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD QUADRUPLE IN-LINE; PLASTIC (SOT-58)


22 max
seating plane
4,7
max
0,7
min
0,76 (2)
3,65
3,20
14x
2,54
0,53
max
0,254 M (1)
2,2
max
8,25 max
0,32
max
5,08
10,16
7Z55830.3


1,4 max
16
15
14
13
12
11
10
9
1
2
3
4
5
6
7
8
top view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

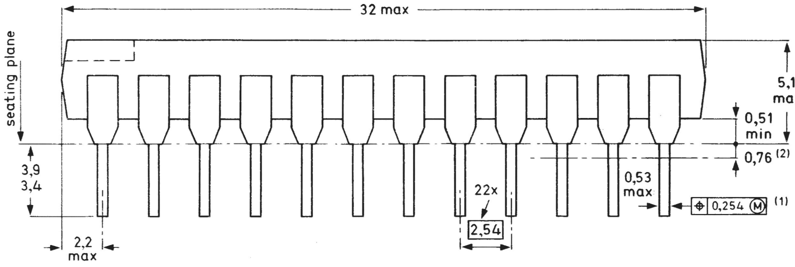
2. By dip or wave

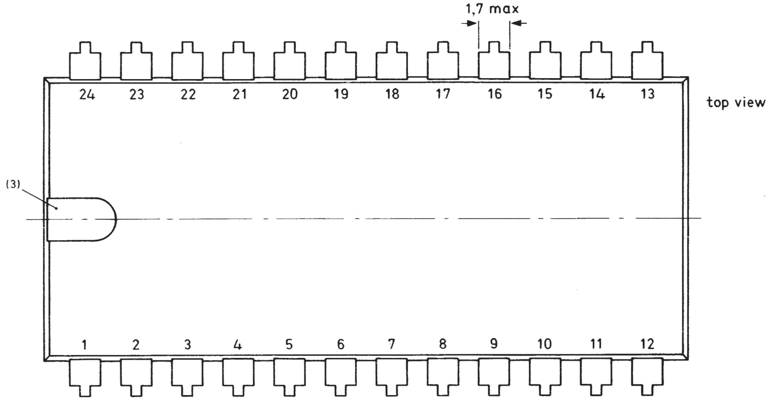
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

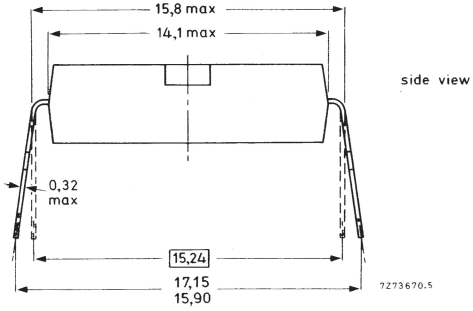
3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)


32 max
seating plane
5,1
max
0,51
min
0,76 (2)
3,9
3,4
22x
2,54
0,53
max
⊕ 0,254 Ⓜ
(1)
2,2
max


1,7 max
24 23 22 21 20 19 18 17 16 15 14 13
top view
(3)
1 2 3 4 5 6 7 8 9 10 11 12


15,8 max
14,1 max
side view
0,32
max
15,24
17,15
15,90
7Z73670.5

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

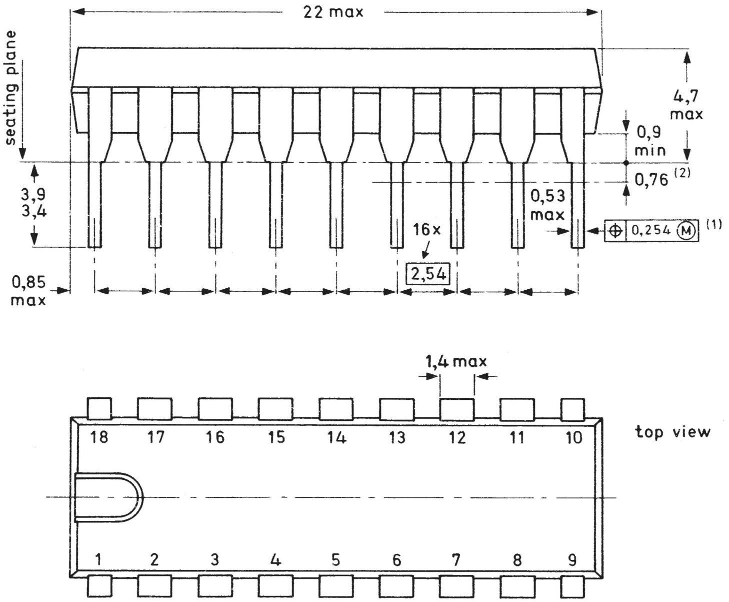
(3) Index may be horizontal as shown, or vertical.

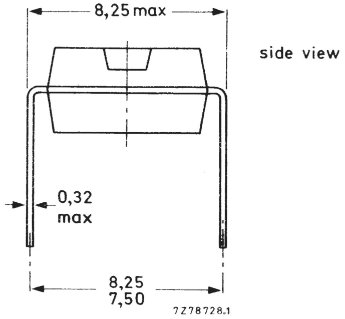
Dimensions in mm

SOLDERING

See page 5 of this chapter (SOT-38).

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102C)


22 max
seating plane
4,7
max
0,9
min
0,76 (2)
3,9
3,4
0,53
max
16x
2,54
0,254 Ⓜ (1)
0,85
max
1,4 max
18
17
16
15
14
13
12
11
10
top view
1
2
3
4
5
6
7
8
9


8,25 max
side view
0,32
max
8,25
7,50
7Z78728.1

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

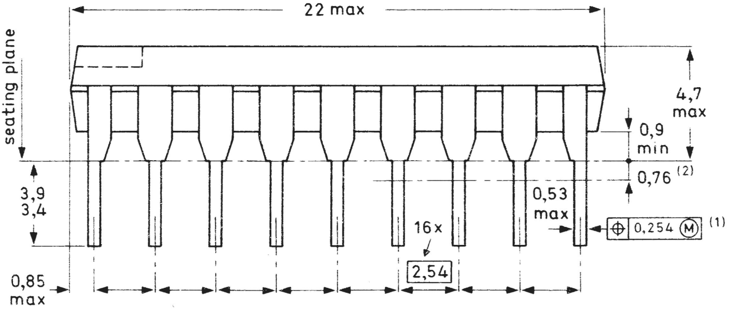
(2) Lead spacing tolerances apply from seating plane to the line indicated.

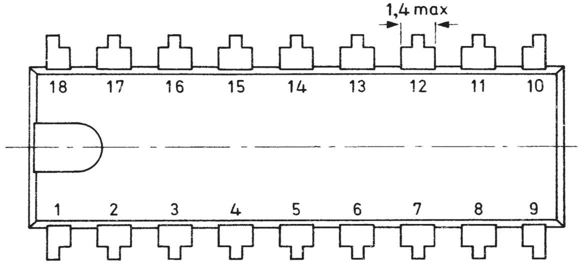
Dimensions in mm

SOLDERING

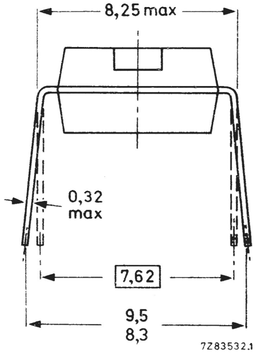
See page 5 of this chapter (SOT-38).

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102CS)


22 max
seating plane
4,7
max
0,9
min
0,76 (2)
3,9
3,4
0,53
max
16x
2,54
0,254 M (1)
0,85
max


1,4 max
18
17
16
15
14
13
12
11
10
1
2
3
4
5
6
7
8
9

top view


8,25 max
0,32
max
7,62
9,5
8,3
7Z83532.1

side view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

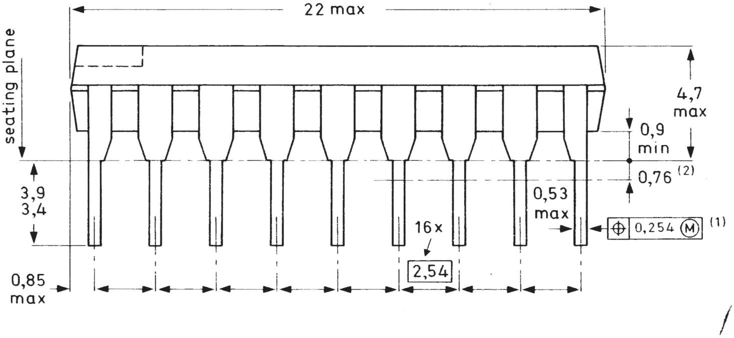
(2) Lead spacing tolerances apply from seating plane to the line indicated.

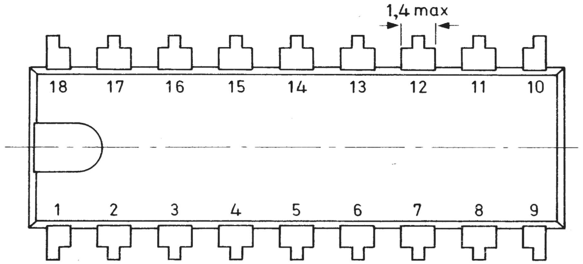
Dimensions in mm

SOLDERING

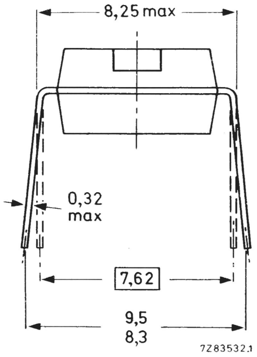
See page 5 of this chapter (SOT-38).

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102HE)


22 max
seating plane
4,7
max
0,9
min
0,76 (2)
3,9
3,4
0,53
max
16 x
2,54
0,254 Ⓜ (1)
0,85
max


1,4 max
18
17
16
15
14
13
12
11
10
1
2
3
4
5
6
7
8
9

top view


8,25 max
0,32
max
7,62
9,5
8,3
7Z83532.1

side view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

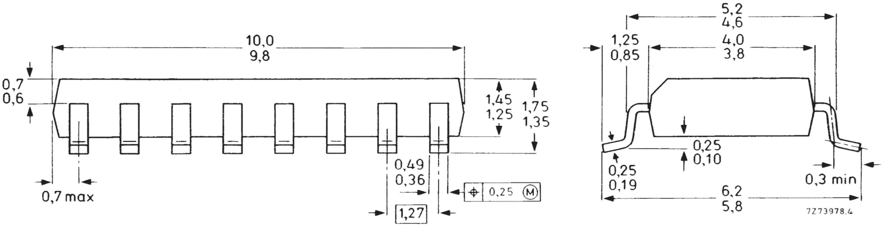
(2) Lead spacing tolerances apply from seating plane to the line indicated.

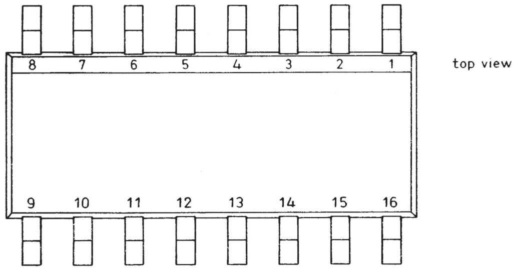
Dimensions in mm

SOLDERING

See page 5 of this chapter (SOT-38).

16-LEAD MINI-PACK; PLASTIC (SO-16; SOT-109A)





Dimensions in mm

⨁ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

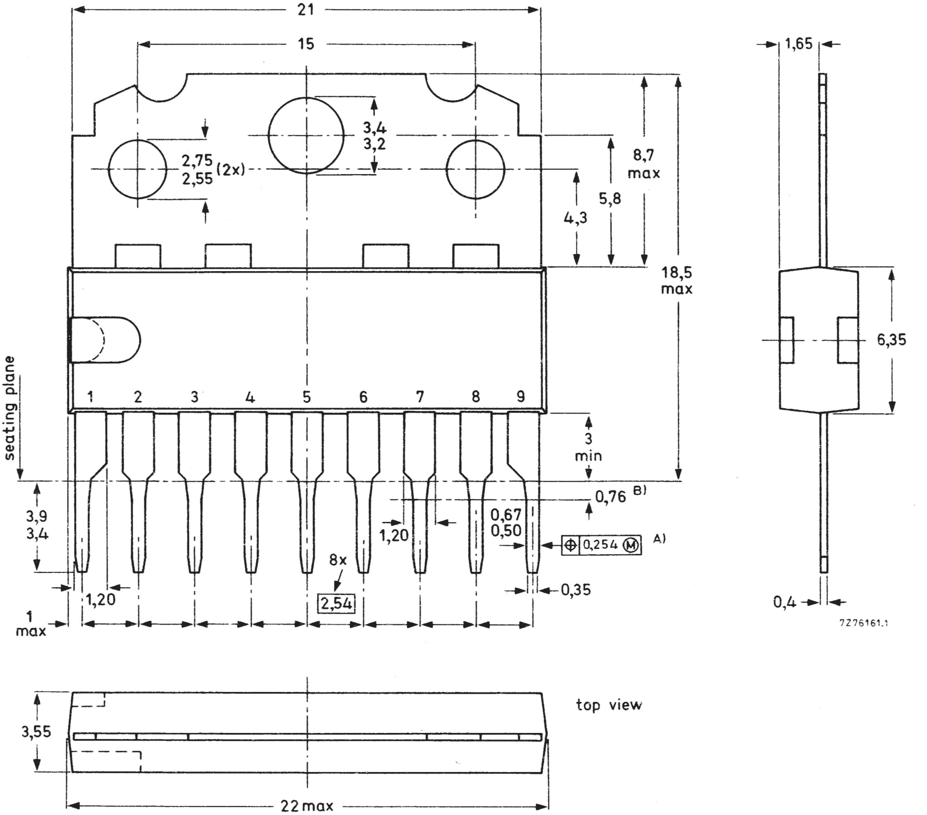
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110B)


21
15
1,65
3,4
3,2
2,75
2,55
(2x)
8,7
max
5,8
4,3
18,5
max
6,35
seating plane
1 2 3 4 5 6 7 8 9
3
min
0,76 B)
3,9
3,4
0,67
0,50
1,20
0,254 Ⓜ A)
8x
2,54
0,35
1,20
1
max
0,4
7Z76161.1
3,55
top view
22 max

Dimensions in mm

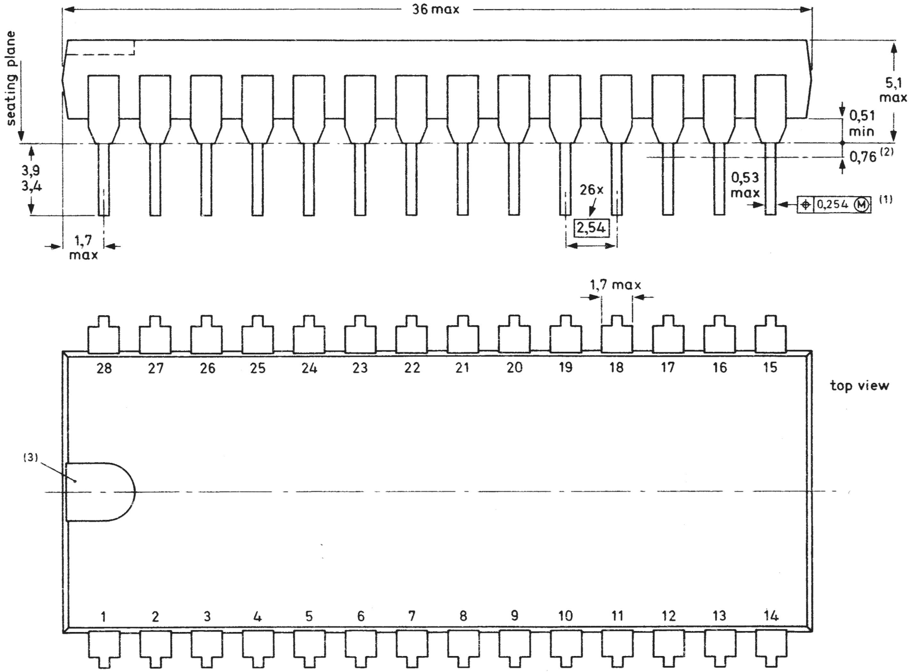
⌖ Positional accuracy.

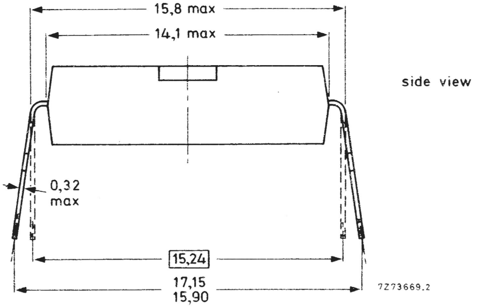
Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)


36 max
seating plane
5,1
max
0,51
min
0,76 (2)
3,9
3,4
0,53
max
26x
2,54
0,254 (M) (1)
1,7
max
1,7 max
28 27 26 25 24 23 22 21 20 19 18 17 16 15
top view
(3)
1 2 3 4 5 6 7 8 9 10 11 12 13 14


15,8 max
14,1 max
side view
0,32
max
15,24
17,15
15,90
7Z73669.2

⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

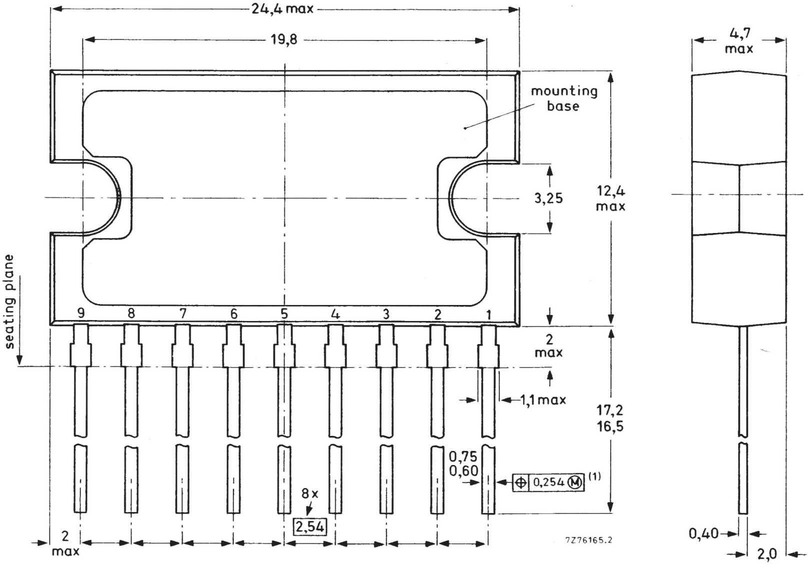
(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

See page 5 of this chapter (SOT-38).

9-LEAD SINGLE IN-LINE; PLASTIC POWER (SOT-131A, B)


24,4 max
19,8
mounting base
3,25
12,4 max
seating plane
9
8
7
6
5
4
3
2
1
2 max
1,1 max
17,2
16,5
0,75
0,60
0,254 (M) (1)
8x
2,54
2 max
7Z76165.2
4,7 max
0,40
2,0

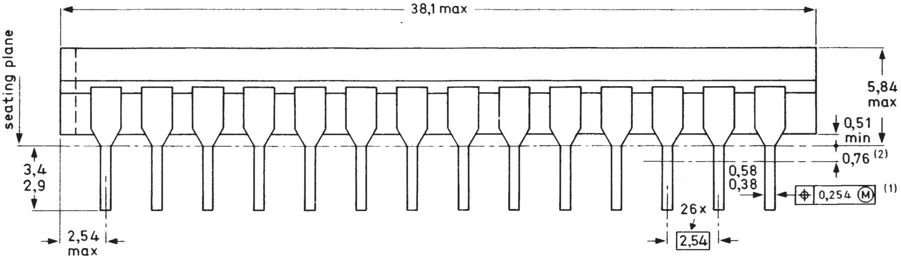
Dimensions in mm

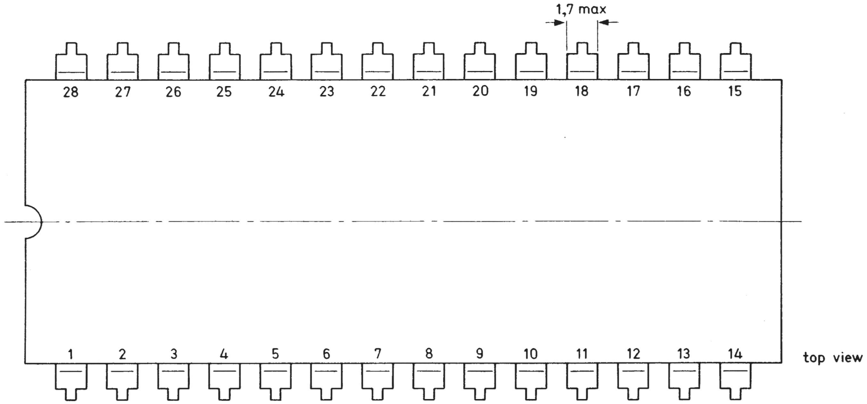
⊕ Positional accuracy.

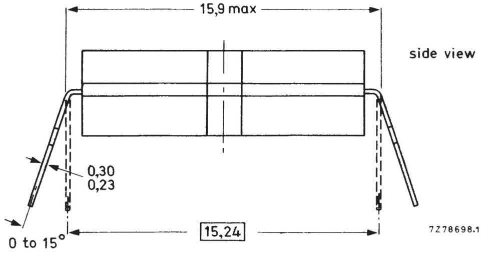
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

28-LEAD DUAL IN-LINE; CERAMIC (SOT-135A)


38,1 max
seating plane
5,84
max
0,51
min
0,76 (2)
3,4
2,9
0,58
0,38
0,254 M
(1)
26x
2,54
2,54
max


1,7 max
28
27
26
25
24
23
22
21
20
19
18
17
16
15
1
2
3
4
5
6
7
8
9
10
11
12
13
14
top view


15,9 max
side view
0,30
0,23
0 to 15°
15,24
7Z78698.1

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

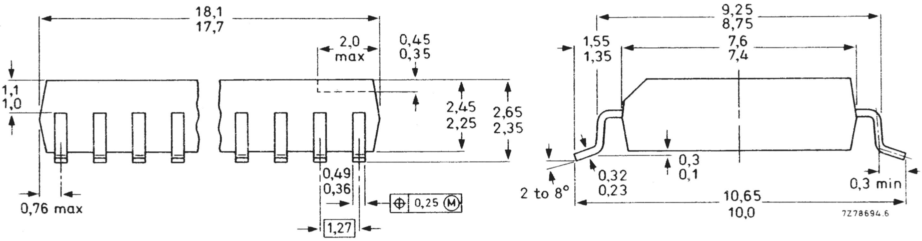
(2) Lead spacing tolerances apply from seating plane to the line indicated.

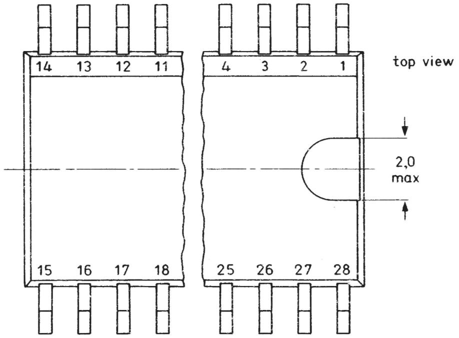
Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

28-LEAD MINI-PACK; PLASTIC (SO-28; SOT-136A)





Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

The reflow solder technique

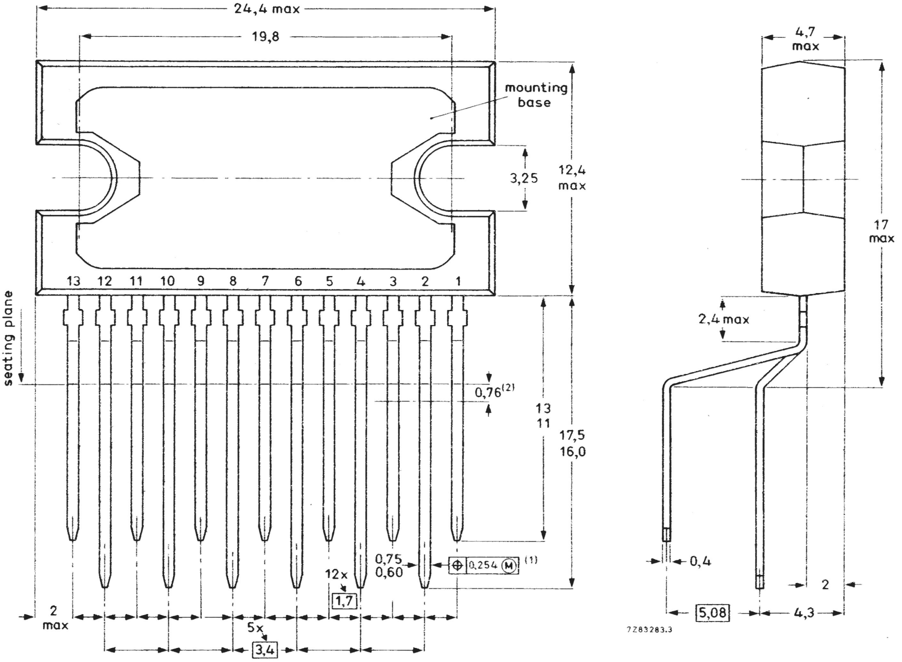
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 °C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

13-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-141B)


24,4 max
19,8
mounting base
3,25
12,4 max
13 12 11 10 9 8 7 6 5 4 3 2 1
seating plane
0,76(2)
13
11
17,5
16,0
0,75
0,60
12x
1,7
0,254 M (1)
2 max
5x
3,4
4,7 max
17 max
2,4 max
0,4
2
5,08
4,3
7Z83283.3

Dimensions in mm

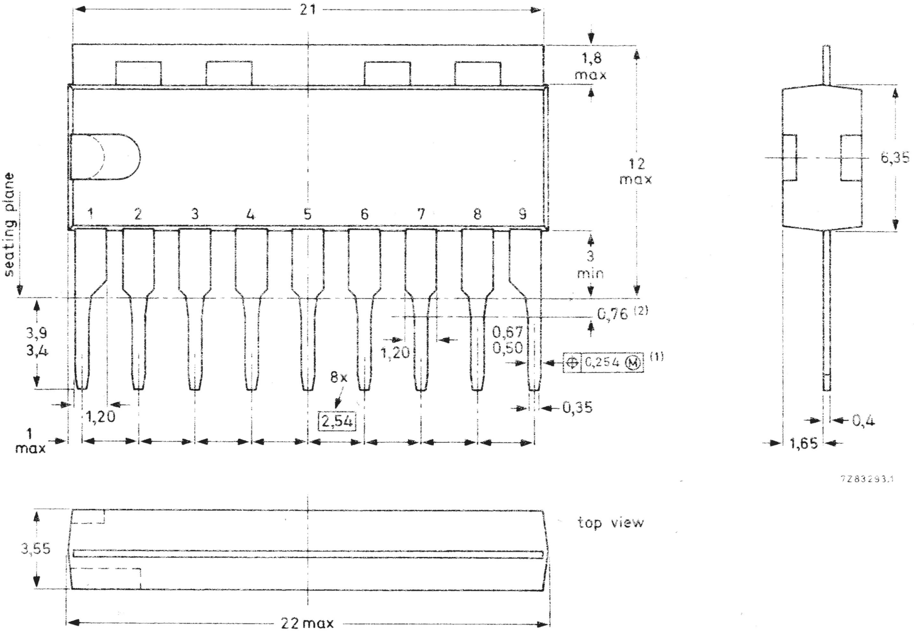
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-142)


21
1,8
max
12
max
seating plane
1
2
3
4
5
6
7
8
9
3
min
0,76 (2)
3,9
3,4
0,67
0,50
1,20
0,254 (M) (1)
8x
2,54
0,35
1,20
1
max
6,35
0,4
1,65
7Z83293.1
3,55
top view
22 max

Dimensions in mm

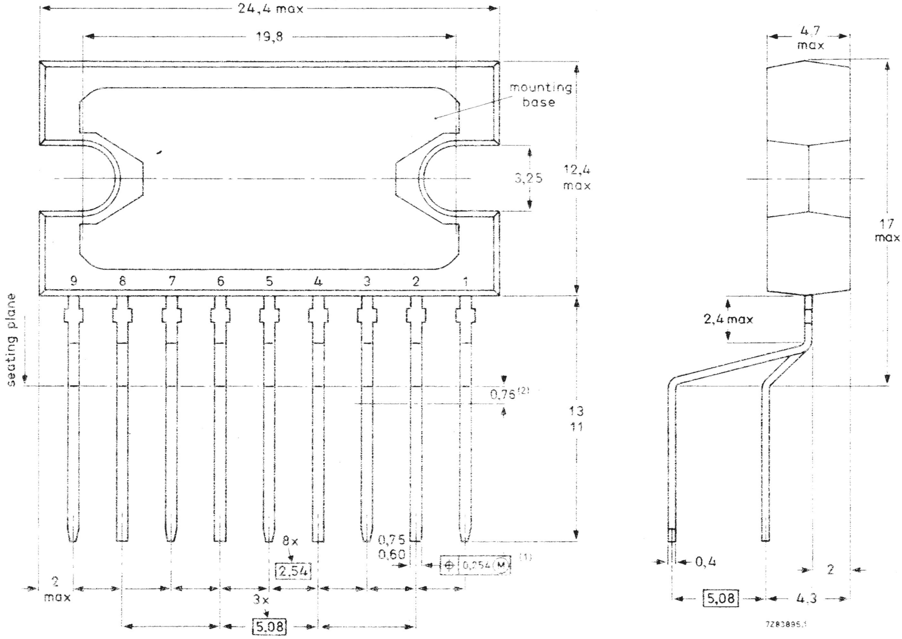
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

9-LEAD SIL-BENT-TO-DIL; PLASTIC POWER (SOT-157B)


24,4 max
19,8
mounting base
3,25
12,4 max
9
8
7
6
5
4
3
2
1
seating plane
0,76 (2)
13
11
8x
2,54
0,75
0,60
⌖ 0,254 Ⓜ (1)
2 max
3x
5,08
4,7 max
17 max
2,4 max
0,4
2
5,08
4,3
7Z83895.1

Dimensions in mm

⌖ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

DEVICE DATA

INTEGRATED AMPLIFIER

for use in ear hearing aids

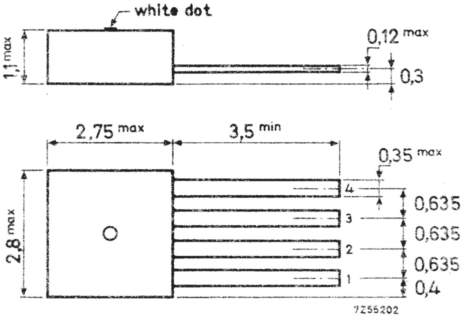
Monolithic integrated circuit amplifier in a plastic envelope, primarily intended for use in ear hearing aids.

QUICK REFERENCE DATA

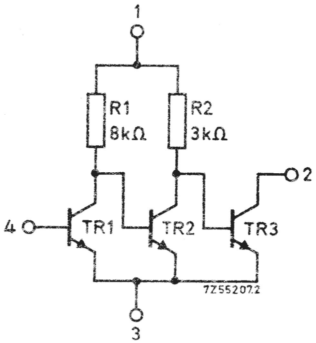
For meaning of symbols see test circuit on page 3				
Supply voltage	V_{1-3}	max.	5	V
Supply current	I_2	max.	5	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	25	mW
The following data are measured in test circuit on page 3				
Total supply current	I_{tot}	typ.	1	mA
Transducer gain	G_{tr}	> typ.	77 85	dB dB
Output power at d_{tot} = 10%	P_o	>	0,2	mW
Cut-off frequency (−3 dB)	f_c	>	20	kHz

PACKAGE OUTLINE (Dimensions in mm)

SOT-20


white dot
1,1 max
0,12 max
0,3
2,75 max
3,5 min
0,35 max
4
3
2
1
0,635
0,635
0,635
0,4
2,8 max
7Z55202

CIRCUIT DIAGRAM


1
R1
8kΩ
R2
3kΩ
2
4
TR1
TR2
TR3
3
7Z55207.2

The sealing of the plastic envelope withstands the accelerated damp heat test of IEC recommendation 68-2 (test D, severity IV, 6 cycles).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

For meaning of symbols test circuit on page 3.

Voltages

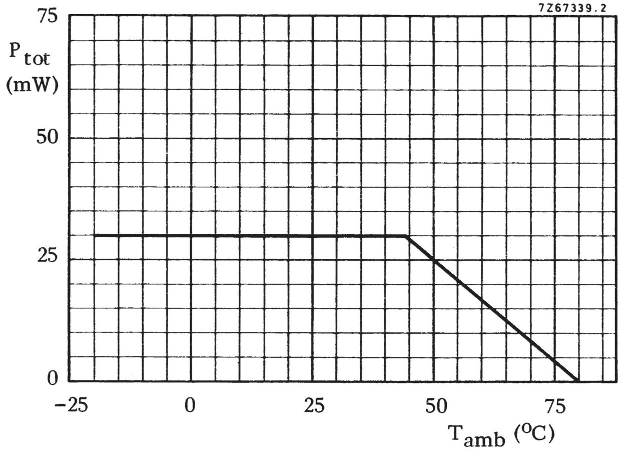
Supply voltage	V_{1-3}	max.	5	V	
Output voltage	V_{2-3}	max.	5	V	1)
Input voltage	$-V_{4-3}$	max.	5	V	

Currents

Output current	I_2	max.	5	mA
Input current	I_4	max.	5	mA

Power dissipation

Power derating curve



Temperatures

Storage temperature	T_{stg}	−20 to +80	°C
Ambient temperature (see derating curve above)	T_{amb}	−20 to +80	°C

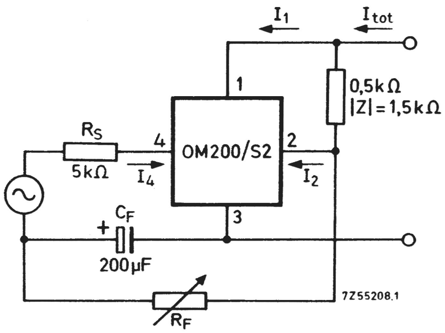
---

1) This value may be exceeded during inductive switch-off for transient energies $< 10 \mu Ws$.

CHARACTERISTICS at $V_{1-3} = 1,3\ V$; $I_2 = 0,7\ mA$ and $T_{amb} = 25\ ^{o}C$ unless otherwise specified

Supply currents (no signal)	I_{tot}	<	1,1	mA	
	I_1	typ.	0,30	mA	
Transducer gain at f = 1 kHz	G_{tr}	>	77	dB	1)
		typ.	85	dB	
Total distortion at f = 1 kHz					
P_o = 100 μW	d_{tot}	typ.	4	%	
		<	6	%	
P_o = 200 μW	d_{tot}	<	10	%	
Noise figure at R_S = 5 kΩ					
B = 400 to 3200 Hz	F	typ.	2,5	dB	
		<	6	dB	2)
Cut-off frequency (−3 dB)	f_c	>	20	kHz	
Value of R_F to adjust I_2 at 0,7 mA	R_F		170 to 1000	kΩ	
		typ.	400	kΩ	

Test circuit



Note

$I_2 = 0,7$ mA; adjusted by means of R_F
$V_{1-3} = 1,3$ V; $T_{amb} = 25\ ^{o}C$

---

1) The transducer gain is defined as the ratio of the output power in the load |Z| = 1,5 kΩ and the available input power of the source with R_S = 5 kΩ.

$$G_{tr} = \frac{P_o}{V_i^2/4\,R_S}$$

2) Due to special processing and pre-measuring, the flutter-noise level is extremely low.

SOLDERING RECOMMENDATIONS

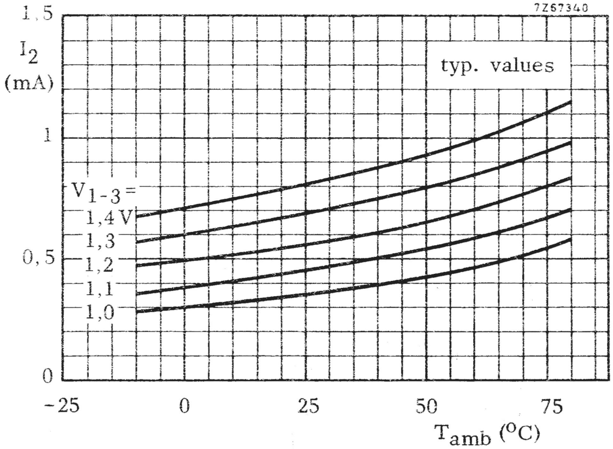
1. Iron soldering

   At a maximum iron temperature of 300 °C the maximum permissible soldering time is 3 seconds, provided the solder spot is at least 0,5 mm from the seal and the leads are not soldered at the same time. Soldering in immediate subsequence is allowed.

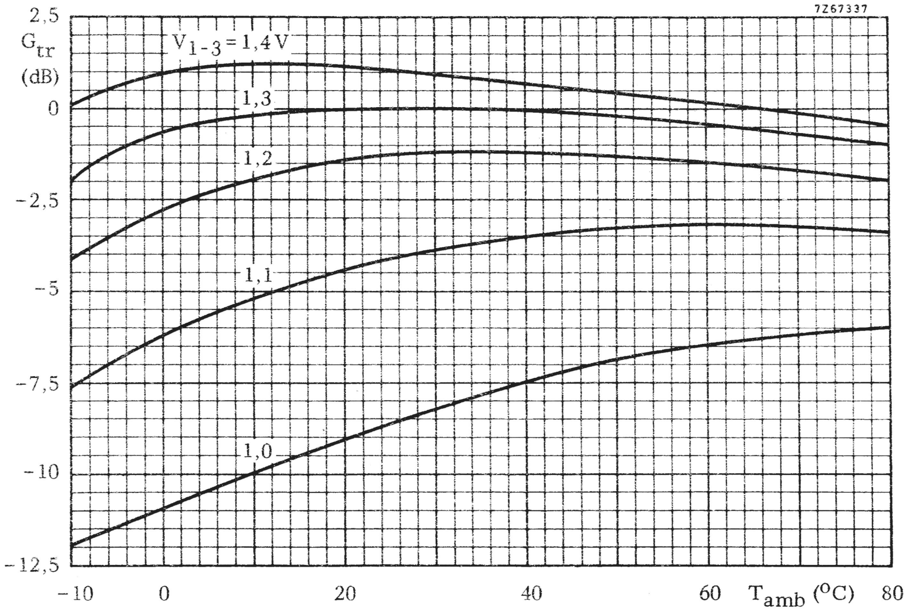
2. Dipsoldering

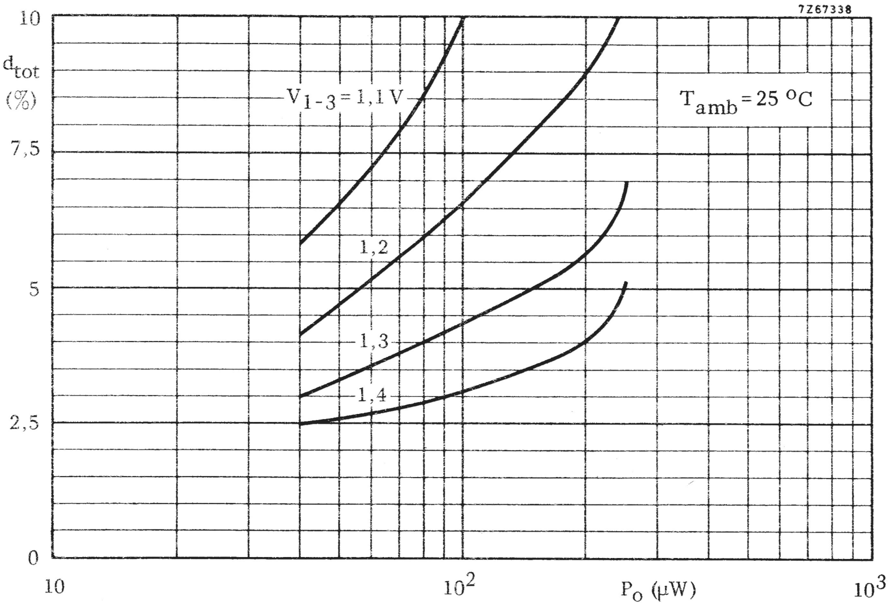
   At a maximum solder temperature of 250 °C the maximum permissible soldering time is 3 seconds, provided the soldered spot is at least 0,5 mm from the seal.

CHARACTERISTICS



The graph applies to test circuit on page 3


7Z67337
2,5
G_{tr}
(dB)
0
-2,5
-5
-7,5
-10
-12,5
V_{1-3} = 1,4 V
1,3
1,2
1,1
1,0
-10
0
20
40
60
T_{amb} (°C)
80


7Z67338
10
d_{tot}
(%)
7,5
5
2,5
0
V_{1-3} = 1,1 V
1,2
1,3
1,4
T_{amb} = 25 °C
10
10^2
P_o (µW)
10^3

RADIO TUNING PLL FREQUENCY SYNTHESIZER

The SAA1057 is a single chip frequency synthesizer IC in I^2L technology, which performs all the tuning functions of a PLL radio tuning system. The IC is applicable to all types of radio receivers, e.g. car radios, hi-fi radios and portable radios.

Features

- On-chip prescaler with up to 120 MHz input frequency.
- On-chip AM and FM input amplifiers with high sensitivity (30 mV and 10 mV respectively).
- Low current drain (typically 16 mA for AM and 20 mA for FM) over a wide supply voltage range (3,6 V to 12 V).
- On-chip amplifier for loop filter for both AM and FM (up to 30 V tuning voltage).
- On-chip programmable current amplifier (charge pump) to adjust the loop gain.
- Only one reference frequency for both AM and FM.
- High signal purity due to a sample and hold phase detector for the in-lock condition.
- High tuning speed due to a powerful digital memory phase detector during the out-lock condition.
- Tuning steps for AM are: 1 kHz or 1,25 kHz for a VCO frequency range of 512 kHz to 32 MHz.
- Tuning steps for FM are: 10 kHz or 12,5 kHz for a VCO frequency range of 70 MHz to 120 MHz.
- Serial 3-line bus interface to a microcomputer.
- Test/features.

QUICK REFERENCE DATA

Supply voltage ranges	V_{CC1}		3,6 to 12	V
	V_{CC2}		3,6 to 12	V
	V_{CC3}		V_{CC2} to 31	V
Supply currents	$I_{CC1} + I_{CC2}$	typ.	18	mA
	I_{CC3}	typ.	0,8	mA
Input frequency ranges				
at pin FAM	f_{FAM}		512 kHz to 32	MHz
at pin FFM	f_{FFM}		70 to 120	MHz
Maximum crystal input frequency	f_{XTAL}	>	4	MHz
Operating ambient temperature range	T_{amb}		−25 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

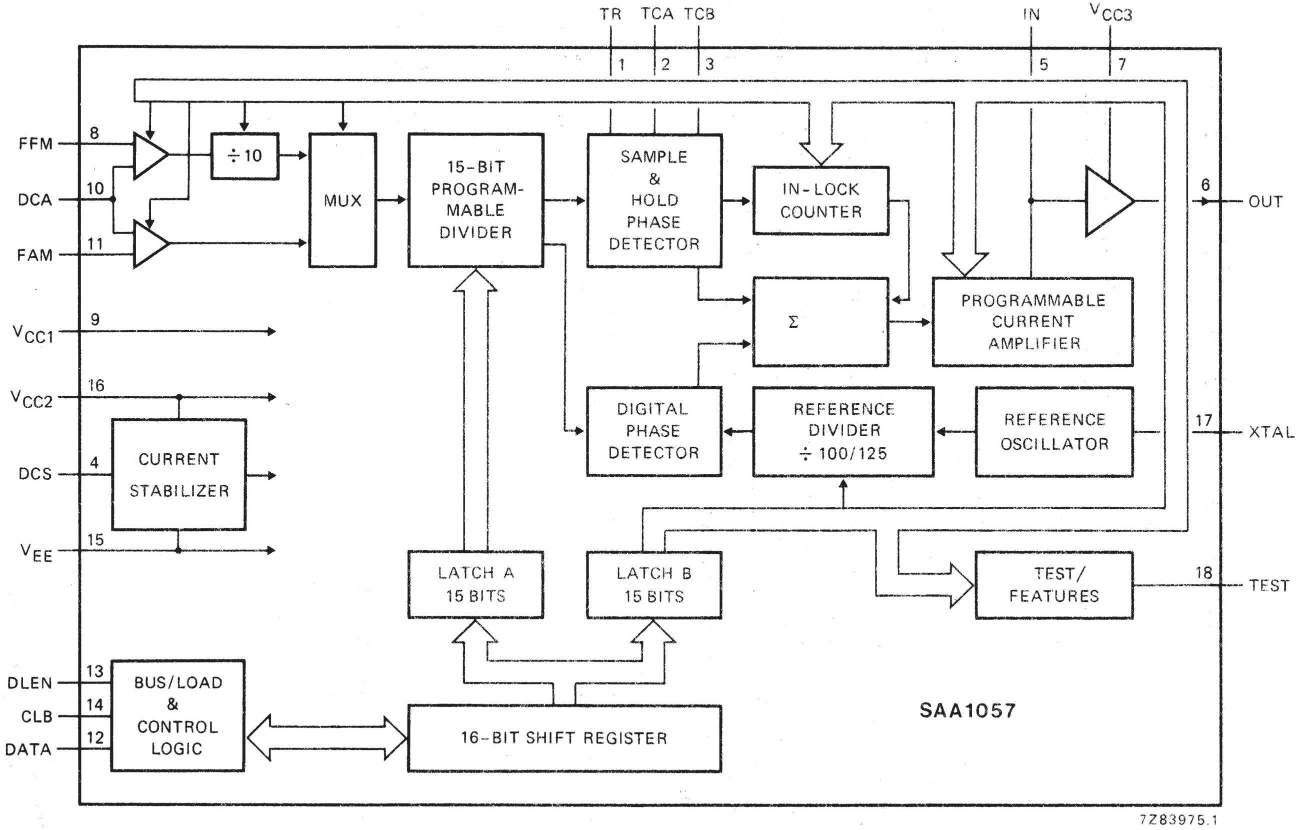

TR
TCA
TCB
IN
V_{CC3}
1
2
3
5
7
FFM
DCA
FAM
8
10
11
÷10
MUX
15-BIT PROGRAM-MABLE DIVIDER
SAMPLE & HOLD PHASE DETECTOR
IN-LOCK COUNTER
Σ
PROGRAMMABLE CURRENT AMPLIFIER
6
OUT
V_{CC1}
9
V_{CC2}
16
DCS
4
CURRENT STABILIZER
V_{EE}
15
DIGITAL PHASE DETECTOR
REFERENCE DIVIDER ÷ 100/125
REFERENCE OSCILLATOR
17
XTAL
LATCH A 15 BITS
LATCH B 15 BITS
TEST/ FEATURES
18
TEST
DLEN
CLB
DATA
13
14
12
BUS/LOAD & CONTROL LOGIC
16-BIT SHIFT REGISTER
SAA1057
7Z83975.1

Fig. 1 Block diagram.

GENERAL DESCRIPTION

The SAA1057 performs the entire PLL synthesizer function (from frequency inputs to tuning voltage output) for all types of radios with the AM and FM frequency ranges.

The circuit comprises the following:

- Separate input amplifiers for the AM and FM VCO-signals.
- A divider-by-10 for the FM channel.
- A multiplexer which selects the AM or FM input.
- A 15-bit programmable divider for selecting the required frequency.
- A sample and hold phase detector for the in-lock condition, to achieve the high spectral purity of the VCO signal.
- A digital memory frequency/phase detector, which operates at a 32 times higher frequency than the sample and hold phase detector, so fast tuning can be achieved.
- An in-lock counter detects when the system is in-lock. The digital phase detector is switched-off automatically when an in-lock condition is detected.
- A reference frequency oscillator followed by a reference divider. The frequency is generated by a 4 MHz quartz crystal. The reference frequency can be chosen either 32 kHz or 40 kHz for the digital phase detector (that means 1 kHz and 1,25 kHz for the sample and hold phase detector), which results in tuning steps of 1 kHz and 1,25 kHz for AM, and 10 kHz and 12,5 kHz for FM.
- A programmable current amplifier (charge pump), which controls the output current of both the digital and the sample/hold phase detector in a range of 40 dB. It also allows the loop gain of the tuning system to be adjusted by the microcomputer.
- A tuning voltage amplifier, which can deliver a tuning voltage of up to 30 V.
- BUS; this circuitry consists of a format control part, a 16-bit shift register and two 15-bit latches. Latch A contains the to be tuned frequency information in a binary code. This binary-coded number, multiplied by the tuning spacing, is equal to the synthesized frequency. The programmable divider (without the fixed divide-by-10 prescaler for FM) can be programmed in a range between 512 and 32 767 (see Fig. 3). Latch B contains the control information.

DEVELOPMENT SAMPLE DATA

OPERATION DESCRIPTION

Control information

The following functions can be controlled with the data word bits in latch B. For data word format and bit position see Fig. 3.

FM	FM/AM selection; '1' = FM, '0' = AM
REFH	reference frequency selection; '1' = 1,25 kHz, '0' = 1 kHz (sample and hold phase detector)
CP3 CP2 CP1 CP0	control bits for the programmable current amplifier (see section Characteristics)
SB2	enables last 8 bits (SLA to T0) of data word B; '1' = enables, '0' = disables; when programmed '0', the last 8 bits of data word B will be set to '0' automatically
SLA	load mode of latch A; '1' = synchronous, '0' = asynchronous
PDM1 PDM0	phase detector mode

PDM1	PDM0	digital phase detector
0	X	automatic on/off
1	0	on
1	1	off

BRM	bus receiver mode bit; in this mode the supply current of the BUS receiver will be switched-off automatically after a data transmission (current-draw is reduced); '1' = current switched; '0' = current always on
T3	test bit; must be programmed always '0'
T2	test bit; selects the reference frequency (32 or 40 kHz) to the TEST pin
T1	test bit; must be programmed always '0'
T0	test bit; selects the output of the programmable counter to the TEST pin

T3	T2	T1	T0	TEST (pin 18)
0	0	0	0	1
0	1	0	0	reference frequency
0	0	0	1	output programmable counter
0	1	0	1	output in-lock counter '0' = out-lock '1' = in-lock

DEVELOPMENT SAMPLE DATA

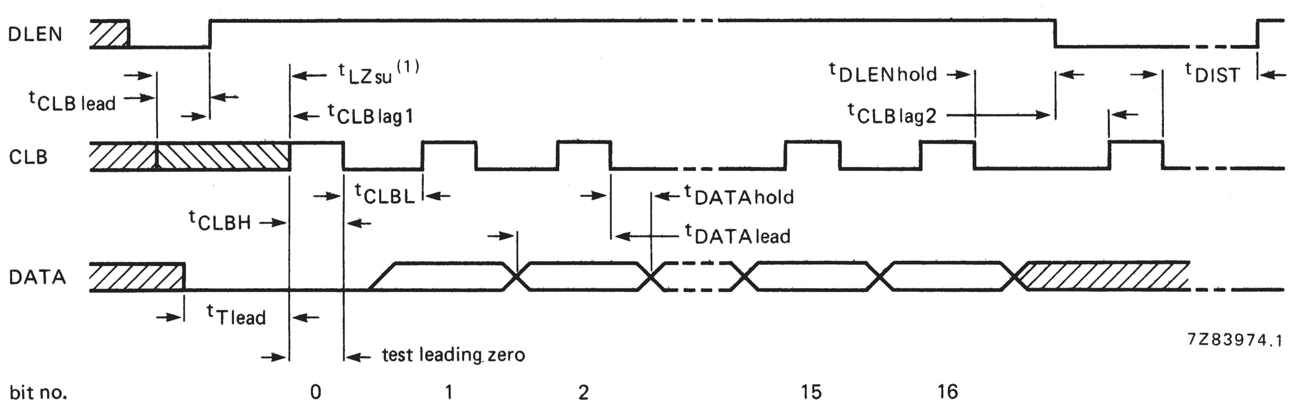

DLEN
CLB
DATA
bit no.
$t_{CLB\,lead}$
$t_{LZsu}^{(1)}$
$t_{CLB\,lag\,1}$
t_{CLBL}
t_{CLBH}
$t_{T\,lead}$
test leading zero
$t_{DATA\,hold}$
$t_{DATA\,lead}$
$t_{DLEN\,hold}$
$t_{CLB\,lag\,2}$
t_{DIST}
0
1
2
15
16
7Z83974.1

Fig. 2 BUS format.

(1) During the zero set-up time (t_{LZsu}) CLB can be LOW or HIGH, but no transient of the signal is permitted. This can be of use when an I^{2}C bus is used for other devices on the same data and clock lines.

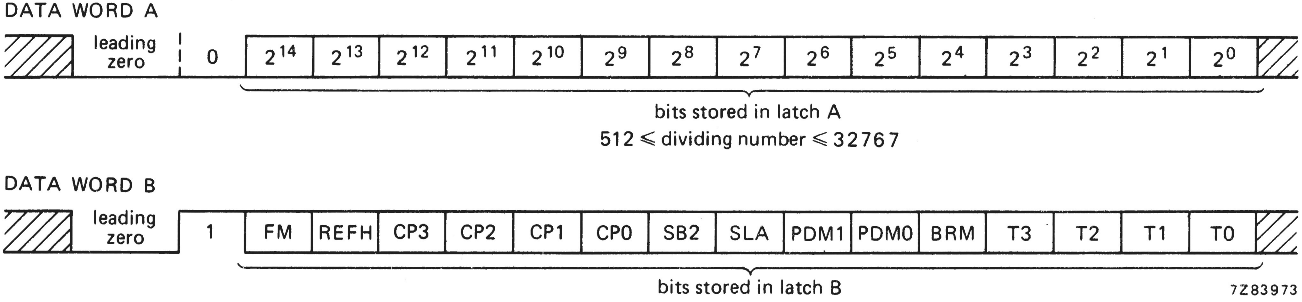

DATA WORD A
leading zero
0
2^{14}
2^{13}
2^{12}
2^{11}
2^{10}
2^{9}
2^{8}
2^{7}
2^{6}
2^{5}
2^{4}
2^{3}
2^{2}
2^{1}
2^{0}
bits stored in latch A
$512 \leqslant$ dividing number $\leqslant 32767$
DATA WORD B
leading zero
1
FM
REFH
CP3
CP2
CP1
CP0
SB2
SLA
PDM1
PDM0
BRM
T3
T2
T1
T0
bits stored in latch B
7Z83973

Fig. 3 Bit organization of data words A and B.

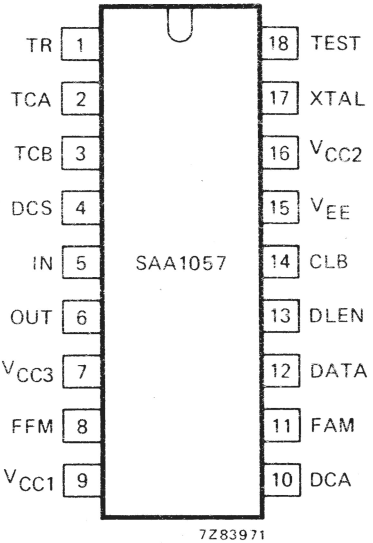

TR 1
TCA 2
TCB 3
DCS 4
IN 5
OUT 6
V_{CC3} 7
FFM 8
V_{CC1} 9
18 TEST
17 XTAL
16 V_{CC2}
15 V_{EE}
14 CLB
13 DLEN
12 DATA
11 FAM
10 DCA
SAA1057
7Z83971

Fig. 4 Pinning diagram.

PINNING

1	TR	resistor/capacitors for sample and hold circuit
2	TCA	
3	TCB	
4	DCS	decoupling of supply
5	IN	input of output amplifier
6	OUT	output of output amplifier
7	V_{CC3}	positive supply voltage of output amplifier
8	FFM	FM signal input
9	V_{CC1}	positive supply voltage of high frequency logic part
10	DCA	decoupling of input amplifiers
11	FAM	AM signal input
12	DATA	BUS
13	DLEN	
14	CLB	
15	V_{EE}	ground
16	V_{CC2}	positive supply voltage of low frequency logic part and analogue part
17	XTAL	reference oscillator input
18	TEST	test output

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; logic and analogue part	V_{CC1}; V_{CC2}		−0,3 to 13,2 V
Supply voltage; output amplifier	V_{CC3}		V_{CC2} to + 32 V
Total power dissipation	P_{tot}	max.	800 mW
Operating ambient temperature range	T_{amb}		−30 to + 85 °C
Storage temperature range	T_{stg}		−65 to + 150 °C

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS

V_{EE} = 0 V; V_{CC1} = V_{CC2} = 5 V; V_{CC3} = 30 V; T_{amb} = 25 °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Supply voltages	V_{CC1}	3,6	5	12	V	
	V_{CC2}	3,6	5	12	V	
	V_{CC3}	V_{CC2}	–	31	V	
Supply currents*						
AM mode	I_{tot}	–	16	–	mA	$I_{tot} = I_{CC1} + I_{CC2}$ in-lock: BRM = '1'; PDM = '0'
FM mode	I_{tot}	–	20	–	mA	
	I_{CC3}	0,3	0,8	1,2	mA	$I_{OUT} = 0$
Operating ambient temperature	T_{amb}	–25	–	+ 80	°C	
RF inputs (FAM, FFM)						
AM input frequency	f_{FAM}	512 kHz	–	32	MHz	
FM input frequency	f_{FFM}	70	–	120	MHz	
Input voltage at FAM	$V_{i\ (rms)}$	30	–	500	mV	
Input voltage at FFM	$V_{i\ (rms)}$	10	–	500	mV	
Input resistance at FAM	R_i	–	2	–	kΩ	
Input resistance at FFM	R_i	–	135	–	Ω	
Input capacitance at FAM	C_i	–	3,5	–	pF	
Input capacitance at FFM	C_i	–	3	–	pF	
Voltage ratio allowed between selected and non-selected input	V_s/V_{ns}	–	–30	–	dB	
Crystal oscillator (XTAL)						see note 1
Maximum input frequency	f_{XTAL}	4	–	–	MHz	
Crystal series resistance	R_s	–	–	150	Ω	
BUS inputs (DLEN, CLB, DATA)						
Input voltage LOW	V_{IL}	0	–	0,8	V	
Input voltage HIGH	V_{IH}	2,4	–	V_{CC1}	V	
Input current LOW	$-I_{IL}$	–	–	50	μA	V_{IL} = 0,8 V
Input current HIGH	I_{IH}	–	–	10	μA	V_{IH} = 2,4 V

---

* When the bus is in the active mode (see BRM in Control Information), 4,5 mA should be added to the figures given.

CHARACTERISTICS (continued)

$V_{EE} = 0$ V; $V_{CC1} = V_{CC2} = 5$ V; $V_{CC3} = 30$ V; $T_{amb} = 25$ °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
BUS inputs timing (DLEN, CLB, DATA)						see also Fig. 2 and note 2
Lead time for CLB to DLEN	$t_{CLBlead}$	1	–	–	µs	
Lead time for DATA to the first CLB pulse	t_{Tlead}	0,5	–	–	µs	
Set-up time for DLEN to CLB	$t_{CLBlag1}$	5	–	–	µs	
CLB pulse width HIGH	t_{CLBH}	5	–	–	µs	
CLB pulse width LOW	t_{CLBL}	5	–	–	µs	
Set-up time for DATA to CLB	$t_{DATAlead}$	2	–	–	µs	
Hold time for DATA to CLB	$t_{DATAhold}$	0	–	–	µs	
Hold time for DLEN to CLB	$t_{DLENhold}$	2	–	–	µs	
Set-up time for DLEN to CLB load pulse	$t_{CLBlag2}$	2	–	–	µs	
Busy time from load pulse to next start of transmission	t_{DIST}	5	–	–	µs	next transmission after word 'B' to other device
Busy time						or
asynchronous mode	t_{DIST}	0,3	–	–	ms	next transmission to SAA1057 after word 'A'
synchronous mode	t_{DIST}	1,3	–	–	ms	
Sample and hold circuit (TR, TCA, TCB)						see also notes 3; 4
Minimum output voltage	V_{TCA}, V_{TCB}	–	1,3	–	V	
Maximum output voltage	V_{TCA}, V_{TCB}	–	–	$V_{CC2}-0,7$	V	
Capacitance at TCA (external)	C_{TCA} C_{TCA}	– –	– –	2,2 2,7	nF nF	REFH = '1' REFH = '0'
Discharge time at TCA	t_{dis} t_{dis}	– –	– –	5 6,25	µs µs	REFH = '1' REFH = '0'
Resistance at TR	R_{TR}	100	–	–	Ω	external
Voltage at TR during discharge	V_{TR}	–	0,7	–	V	
Capacitance at TCB	C_{TCB}	–	–	10	nF	external
Bias current into TCA, TCB	I_{bias}	–	–	10	nA	in-lock

CHARACTERISTICS (continued)

$V_{EE} = 0$ V; $V_{CC1} = V_{CC2} = 5$ V; $V_{CC3} = 30$ V; $T_{amb} = 25$ °C; unless otherwise specified

	symbol	min.	typ.	max.		conditions
Programmable current amplifier (PCA)						
Output current of the dig. phase detector	$\pm I_{dig}$	–	0,4	–	mA	
Current gain of PCA						
CP3 CP2 CP1 CP0						
P1 0 0 0 0	G_{P1}	–	0,023	–		$V_{CC2} \geqslant 5$ V (only for P1)
P2 0 0 0 1	G_{P2}	–	0,07	–		
P3 0 0 1 0	G_{P3}	–	0,23	–		
P4 0 1 1 0	G_{P4}	–	0,7	–		
P5 1 1 1 0	G_{P5}	–	2,3	–		
Ratio between the output current of S/H into PCA and the voltage on C_{TCB}	S_{TCB}	–	1,0	–	μA/V	
Offset voltage on TCB	ΔV_{TCB}	–	–	1	V	in-lock
Output amplifier (IN,OUT)						
Input voltage	V_{IN}	–	1,3	–	V	in-lock; equal to internal reference voltage
Output voltages						
minimum	V_{OUT}	–	–	0,5	V	$-I_{OUT} = 1$ mA
maximum	V_{OUT}	$V_{CC3}-2$	–	–	V	$I_{OUT} = 1$ mA
maximum	V_{OUT}	$V_{CC3}-1$	–	–	V	$I_{OUT} = 0{,}1$ mA
Maximum output current	$\pm I_{OUT}$	5	–	–	mA	$V_{OUT} = \frac{1}{2} V_{CC3}$
Test output (TEST)*						
Output voltage LOW	V_{TL}	–	–	0,5	V	
Output voltage HIGH	V_{TH}	–	–	12	V	
Output current OFF	I_{Toff}	–	–	10	μA	V_{TH}
Output current ON	I_{Ton}	150	–	–	μA	V_{TL}
Ripple rejection**						
at $f_{ripple} = 100$ Hz						
$\Delta V_{CC1}/\Delta V_{OUT}$		–	77	–	dB	
$\Delta V_{CC2}/\Delta V_{OUT}$		–	55	–	dB	
$\Delta V_{CC3}/\Delta V_{OUT}$		–	50	–	dB	$V_{OUT} \leqslant V_{CC3}-3$ V

---

* Open collector output.

** Measured in Fig. 6.

NOTES

1. Pin 17 (XTAL) can also be used as an input for an external clock.
   The circuit for that is given in Fig. 5. The values given in Fig. 5 are a typical application example.

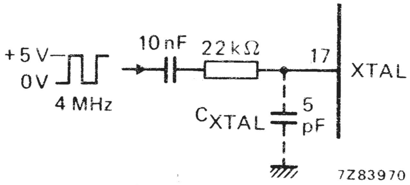


Fig. 5 Circuit configuration showing external 4 MHz clock.

2. See BUS information in section 'operation description'.
3. The output voltage at TCB and TCA is typically ½ V_{CC2} + 0,3 V when the tuning system is in-lock via the sample and hold phase detector. The control voltage at TCB is defined as the difference between the actual voltage at TCB and the value calculated from the formula ½ V_{CC2} + 0,3 V.
4. Crystal oscillator frequency f_{XTAL} = 4 MHz.

APPLICATION INFORMATION

Initialize procedure

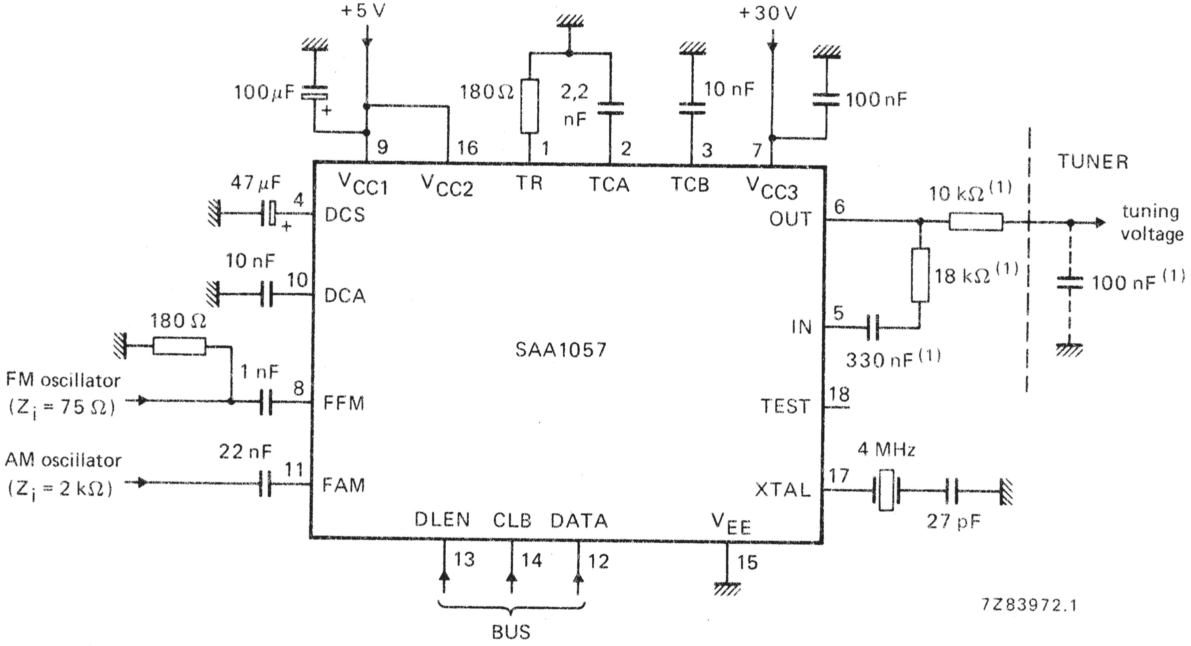
Either a train of at least 10 clock pulses should be applied to the clock input (CLB) or word B should be transmitted, to achieve proper initialization of the device.
For the complete initialization (defining all control bits) a transmission of word B should follow. This means that the IC is ready to accept word A.

Synchronous/asynchronous operation

Synchronous loading of the frequency word into the programmable counter can be achieved when bit 'SLA' of word B is set to '1'. This mode should be used for small frequency steps where low tuning noise is important (e.g. search and manual tuning). This mode should not be used for frequency changes of more than 31 tuning steps. In this case asynchronous loading is necessary. This is achieved by setting bit 'SLA' to '0'. The in-lock condition will then be reached more quickly, because the frequency information is loaded immediately into the divider.

Restrictions to the use of the programmable current amplifier

The lowest current gain (0,023) must not be used in the in-lock condition when the supply voltage V_{CC2} is below 5 V (CP3, CP2, CP1 and CP0 are all set to '0'). This is to avoid possible instability of the loop due to a too small range of the sample and hold phase detector in this condition (see also section 'Characteristics').


+5 V
100 μF
+
9
16
V_{CC1}
V_{CC2}
180 Ω
2,2 nF
1
2
TR
TCA
10 nF
3
TCB
+30 V
100 nF
7
V_{CC3}
47 μF
4
DCS
10 nF
10
DCA
180 Ω
1 nF
8
FFM
FM oscillator
(Z_i = 75 Ω)
AM oscillator
(Z_i = 2 kΩ)
22 nF
11
FAM
SAA1057
6
OUT
10 kΩ (1)
TUNER
tuning voltage
18 kΩ (1)
100 nF (1)
5
IN
330 nF (1)
18
TEST
4 MHz
17
XTAL
27 pF
DLEN
CLB
DATA
V_{EE}
13
14
12
15
BUS
7Z83972.1

(1) Values depend on the tuner diode characteristics.

Fig. 6 Application example of the SAA1057 PLL frequency synthesizer module.

LED DISPLAY/INTERFACE CIRCUIT

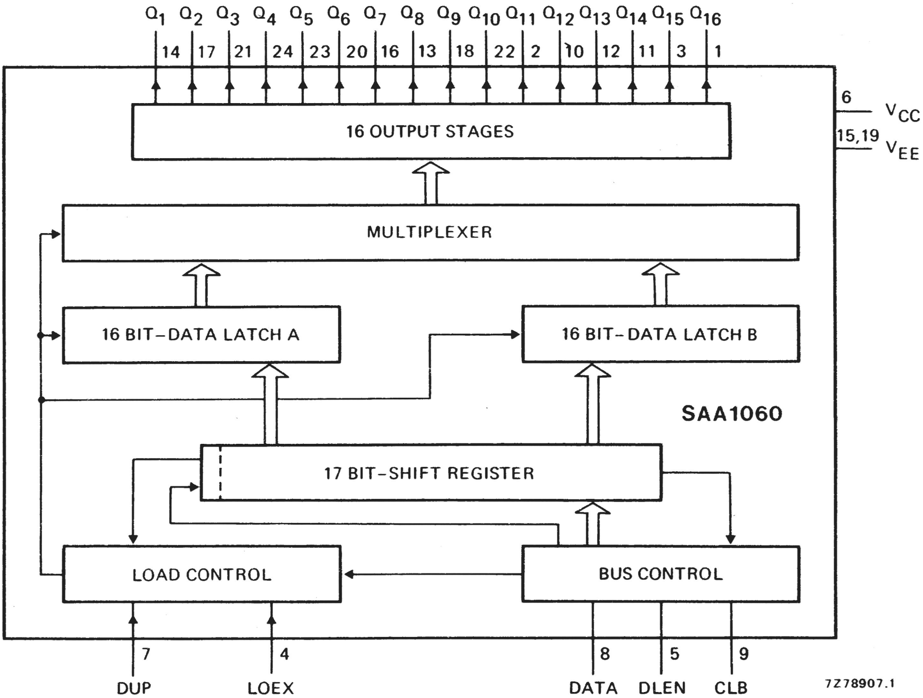

Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16
14 17 21 24 23 20 16 13 18 22 2 10 12 11 3 1
6
VCC
15,19
VEE
16 OUTPUT STAGES
MULTIPLEXER
16 BIT-DATA LATCH A
16 BIT-DATA LATCH B
SAA1060
17 BIT-SHIFT REGISTER
LOAD CONTROL
BUS CONTROL
7
4
8
5
9
DUP
LOEX
DATA
DLEN
CLB
7Z78907.1

Fig. 1 Block diagram.

Features

- Driving 7, 14, 16-segment displays.
- Driving linear displays, bar graph displays for analogue functions.
- Serial to parallel decoder.
- Bus control for the selection of 18-bit words.
- 2 x 16-bit latch.
- Duplex operation for two modes of output: static (16 bit) or dynamic (2 x 16 bit).
- Data transfer control.
- 2 outputs for higher output current (80 mA).

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4 to 6	V
Operating ambient temperature range	T_{amb}		−20 to + 80	°C
Maximum input frequency	f_I	typ.	50	kHz
Supply current	I_{CC}	typ.	60	mA
Output current	I_Q	<	40	mA
Output current (Q_8 and Q_{16} only)	I_Q	<	80	mA

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A).

GENERAL DESCRIPTION

The integrated circuit SAA1060 is primarily designed to drive the display unit of a digital tuning system. It can also be used as a 16-bit serial to parallel decoder. Since the device has no decoder (this is handled by a microcomputer), it has many applications:

- driving 7-segment displays
- driving 14-segment displays
- driving linear displays, e.g. pointer, bar graph
- static output of switch-functions
- digital to analogue converter, with external R-2R network
- extension of the number of outputs for microprocessors or microcomputers.

Data transmission is initiated by means of a burst of clock pulses (CLB), a data line enable signal (DLEN) and the data signal (DATA). The bus control circuit distinguishes between interference and valid data by checking word length (17 bits) and the leading zero. This allows different bus information to be supplied on the same bus lines for other circuits (e.g. SAA1056 with 16 bits).

The last bit (bit 17) of the data word contains the information which of the two internal latches will be loaded. The input LOEX determines if the latched data of selected latches is presented directly to the outputs, or synchronized with the data select signal DUP.

The output stages are n-p-n transistors with open collectors. The current capability is designed for the requirements of duplex operation. Two of the outputs (Q_8 and Q_{16}) are arranged for double current, so that 2 x 2 segments can be connected in parallel.

OPERATION DESCRIPTION

Data inputs (DLEN, DATA)

The SAA1060 processes serially the 18-bit data words synchronized with the clock burst (CLB) and applied to the data input DATA. A command will be accepted only when the data line enable input (DLEN) is HIGH (see Fig. 3).

16th bit 1st bit

load	P	O	N	M	L	K	J	I	H	G	F	E	D	C	B	A	
bit	Q_{16}	Q_{15}	Q_{14}	Q_{13}	Q_{12}	Q_{11}	Q_{10}	Q_9	Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	

7Z78909

leading zero

Fig. 2 Organization of a data word.

Condition for 17th bit:
0 = load data latch B
1 = load data latch A

The loading of the accepted information in one of the data latches is done by the 19th clock pulse, when DLEN is LOW.

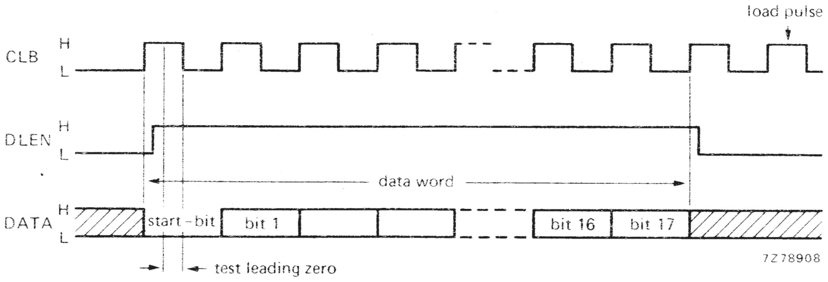


Fig. 3 Pulse diagram of the 16-bit data transmission.

Each data word must start with a leading zero. The SAA1060 checks the data word for the correct length (18 bits) and also for the leading zero.
The actual data is switched directly to the appropriate outputs. For switching on a segment, a '0' (LOW) is necessary at the appropriate data bit.

Data selection input (DUP)

The logic states at input DUP determine which of the two latch contents can be found on the output.

0 = latch A contents
1 = latch B contents

Load control input (LOEX)

Input LOEX determines the operation mode in which the device is able to work.

0 = duplex mode, i.e. output synchronized with the duplex signal
1 = d.c. mode, i.e. output direct from the by DUP selected data latch.

When operating in duplex mode at 50 Hz, the time between two data words to be transmitted must be > 21 ms.

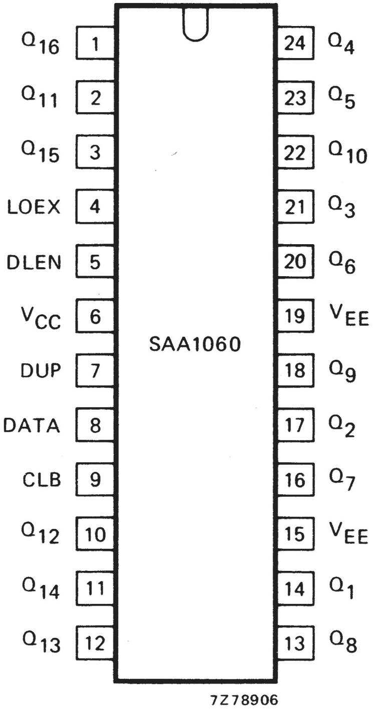

Q16
1
Q11
2
Q15
3
LOEX
4
DLEN
5
VCC
6
DUP
7
DATA
8
CLB
9
Q12
10
Q14
11
Q13
12
24
Q4
23
Q5
22
Q10
21
Q3
20
Q6
19
VEE
18
Q9
17
Q2
16
Q7
15
VEE
14
Q1
13
Q8
SAA1060
7Z78906

Fig. 4 Pinning diagram.

RATINGS ($V_{EE} = 0$)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{CC}	−0,3 to + 7	V
Total power dissipation	P_{tot}	max. 900	mW
Operating ambient temperature range	T_{amb}	−20 to + 80	°C
Storage temperature range	T_{stg}	−25 to + 125	°C

CHARACTERISTICS

V_{EE} = 0; T_{amb} = 25 °C; unless otherwise specified

	V_{CC} V	symbol	min.	typ.	max.		conditions
Supply voltage	–	V_{CC}	4	5	6	V	
Supply current	5	I_{CC}	–	60	–	mA	
Inputs DATA, CLB, DLEN, LOEX							
input voltage HIGH	5	V_{IH}	2	–	5	V	
input voltage LOW	5	V_{IL}	–	–	1	V	
input current LOW	5	$-I_{IL}$	–	–	20	µA	$V_I = 0$
maximum input frequency	5	f_I	–	50	–	kHz	
Input DUP							
input voltage HIGH	5	V_{IH}	0,8	–	12	V	
input voltage LOW	5	V_{IL}	–6	–	0,4	V	
input current HIGH	5	I_{IH}	0,01	–	12	mA	
maximum input frequency	5	f_I	–	50	–	kHz	
Outputs Q_1 to Q_7, Q_9 to Q_{15}							
output voltage HIGH	5	V_{QH}	–	–	16,8	V	$I_{QH} = 0$
output voltage LOW	5	V_{QL}	–	–	0,5	V	I_{QL} = 40 mA
output current LOW							
duplex mode	5	I_{QL}	–	–	60	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{QL}	–	20	40	mA	
Outputs Q_8 and Q_{16}							
output voltage HIGH	5	V_{QH}	–	–	16,8	V	$I_{QH} = 0$
output voltage LOW	5	V_{QL}	–	–	0,5	V	I_{QL} = 80 mA
output current LOW							
duplex mode	5	I_{QL}	–	–	120	mA	peak value at sinusoidal voltage
d.c. mode	5	I_{QL}	–	40	80	mA	

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

LCD DISPLAY/INTERFACE CIRCUIT

GENERAL DESCRIPTION

The SAA1062A is designed to drive a Liquid Crystal Display (LCD) of a digital tuning system. It contains a shift register with programmable length (18 or 21 bits), latches, both synchronized or static, exclusive-OR segment drivers (17 or 20 bits), an i.f. oscillator and a backplane driver for the LCD. The circuit is designed to be driven by a 3 bus structure from a microcomputer and can also be used as a programmable 17 or 20 bits serial-to-parallel decoder. It is also capable of storing 40 bits of information.

Features

- Driving 7 to 20-segment displays.
- Driving linear displays.
- Serial to parallel decoder of digital signals.
- Bus control for the selection of 18/21-bit words.
- 17/20-bit latch.
- A.C. segment drive.
- On-chip oscillator.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4,2 to 5,5	V
Operating ambient temperature range	T_{amb}		−20 to + 70	°C
Maximum input frequency	f_i	typ.	50	kHz
Supply current	I_{CC}	typ.	3,5	mA
Output current (Q_1 to Q_{20})	I_Q	>	60	μA

PACKAGE OUTLINES

SAA1062A : 28-lead DIL; plastic (SOT-117).
SAA1062AT: 28-lead mini-pack; plastic (SO-28; SOT-136A).

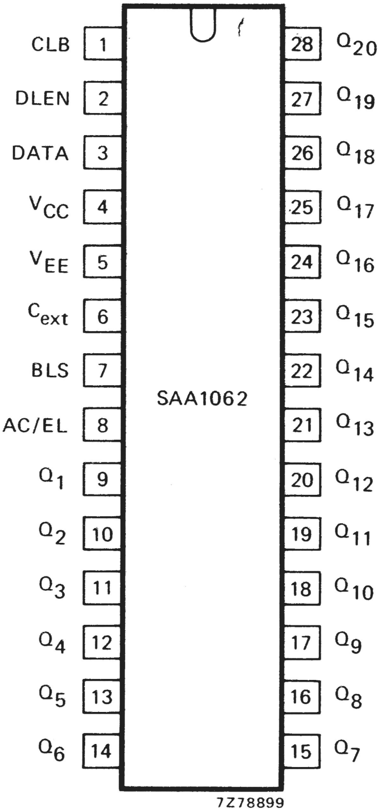

CLB
DLEN
DATA
V_{CC}
V_{EE}
C_{ext}
BLS
AC/EL
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
1
2
3
4
5
6
7
8
9
10
11
12
13
14
SAA1062
28
27
26
25
24
23
22
21
20
19
18
17
16
15
Q_{20}
Q_{19}
Q_{18}
Q_{17}
Q_{16}
Q_{15}
Q_{14}
Q_{13}
Q_{12}
Q_{11}
Q_{10}
Q_9
Q_8
Q_7
7Z78899

Fig. 1 Pinning diagram.

DEVELOPMENT SAMPLE DATA

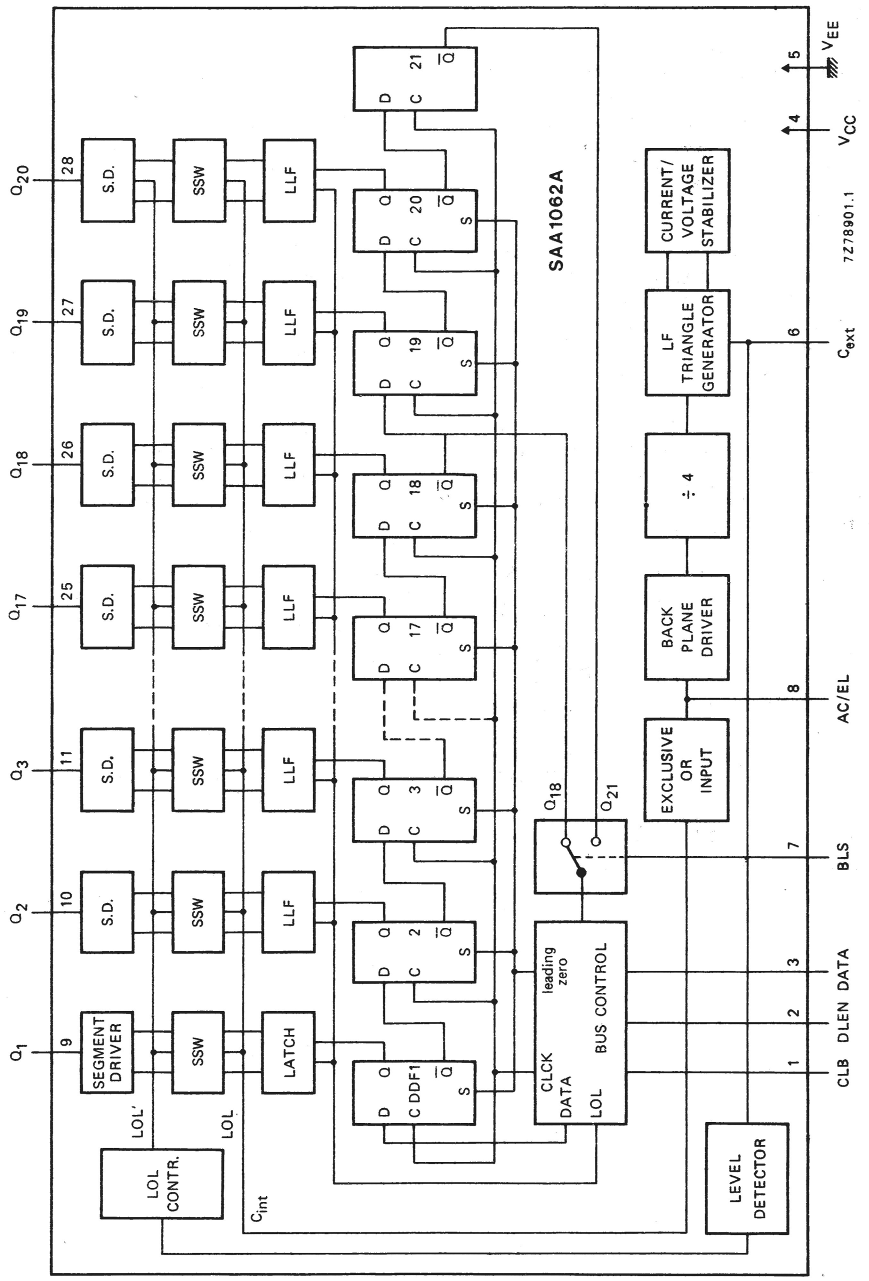

SAA1062A
Q1
Q2
Q3
Q17
Q18
Q19
Q20
9
10
11
25
26
27
28
SEGMENT DRIVER
S.D.
SSW
LATCH
LLF
D
C
Q
Q̄
S
DDF1
2
3
17
18
19
20
21
LOL'
LOL
LOL CONTR.
C_{int}
CLCK
DATA
LOL
leading zero
BUS CONTROL
Q18
Q21
EXCLUSIVE OR INPUT
BACK PLANE DRIVER
÷ 4
LF TRIANGLE GENERATOR
CURRENT/ VOLTAGE STABILIZER
LEVEL DETECTOR
1
2
3
7
8
6
4
5
CLB
DLEN
DATA
BLS
AC/EL
C_{ext}
V_{CC}
V_{EE}
7Z78901.1

Fig. 2 Block diagram.

OPERATION DESCRIPTION

The input information for this device consists of a data bus with 18 or 21 bits words, an external clock synchronized with the data bus and an enable signal. The organization of these signals is given in Fig. 3. These signals are handled by the BUS CONTROL circuit in which the decision is made whether these signals are valid for the device. It contains a leading zero detector (start condition of reception) and a data-length control. Leading zero is detected when the data signal is LOW and the DLEN signal is HIGH, during the first HIGH period of the clock signal. During the HIGH period of DLEN, the length control determines if the clock signal consists of the programmed number of pulses (18 or 21). This last function permits the user to supply other information on the same signal lines.

Furthermore the bus control prevents the device from accepting inferferences on the signal lines. While leading zero is detected, the shift register is set and for a proper leading zero the following data is shifted into this register. The Q_n position of the first bit of the register is shifted into the last bit, if the length of the data and the clock input are correct. Incorrect length of the information is detected by checking the value of the last bit of the programmed register. If the data transmission has been accepted properly, the bus control stage generates a valid pulse (LOL).
This pulse enables the load control circuit to load the contents of the register into the output latch immediately. On the first edge of the backplane driver signal "AC out/EL in" following on this "LOL" pulse, the new information of this latch is transferred to the output driver which also contains a latch. With this ability it is possible to load the device with 20 bits and also to transfer this data to the segment outputs. Furthermore, the SR can be reloaded by a second complete load procedure without a load enable clock pulse. This causes the SR to contain 20 bits and the output latches another 20 bits of information.
The output driver also contains an EXCLUSIVE-OR which is driven by the backplane driver signal and the latch output. The segment driver output signal is in phase with the output of the backplane driver when the input data is HIGH ("1") and 180° out-of-phase when the input data is LOW ("0").
In the static or slave mode, the backplane output can be used as input by connecting pin 6 to ground or V_{CC}. The IC now can operate as a static driver or as a synchronized slave.

The l.f. oscillator consists of a triangle generator of the I-2I principle. It only needs an external capacitor to fix the frequency. As both amplitude and current are temperature compensated, this frequency is more or less independent of pn temperature. An internal switching signal of this generator is divided by 4 to attain a symmetrical output for the backplane driver (pin 8) of nominal 60 Hz for an external capacitor of 22 nF.

The backplane driver is able to drive a 40 bits display.

The bit length of the shift register is programmed with BLS (Bit Length Selector) (pin 7). If BLS is kept LOW the DATA bit length is 20; for BLS open or HIGH a DATA bit length of 17 is selected.

DEVELOPMENT SAMPLE DATA

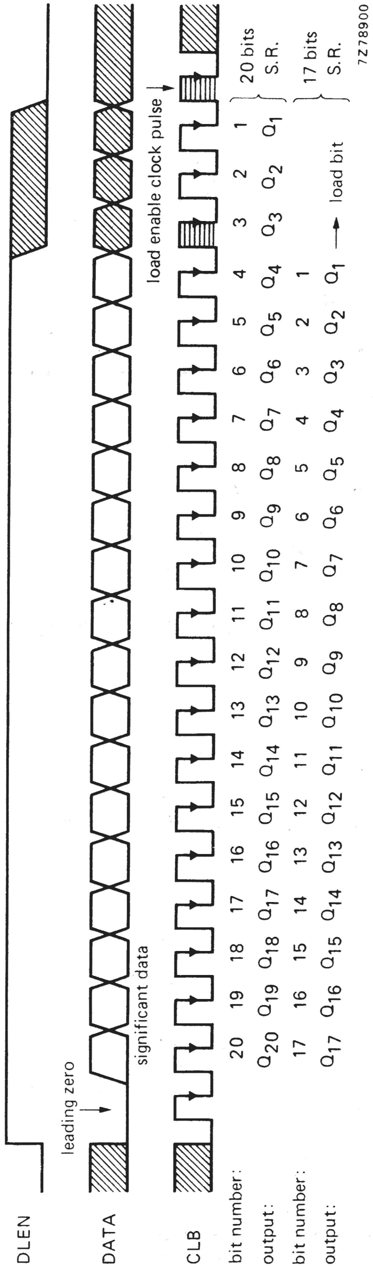

DLEN
DATA
CLB
bit number:
output:
bit number:
output:
leading zero
significant data
load enable clock pulse
20 bits S.R.
17 bits S.R.
load bit
20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Q20 Q19 Q18 Q17 Q16 Q15 Q14 Q13 Q12 Q11 Q10 Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1
17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Q17 Q16 Q15 Q14 Q13 Q12 Q11 Q10 Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1
7Z78900

Fig. 3 Organization of 18 and 21 bit words; DATA = LOW means segment ‘on’.

RATINGS ($V_{EE} = 0$)

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	6 V
Total power dissipation at T_{amb} = 100 °C derate linearly with 0,02 W/°C	P_{tot}	max.	500 mW
Operating ambient temperature range	T_{amb}		−25 to + 125 °C
Storage temperature range	T_{stg}		−55 to + 125 °C

CHARACTERISTICS

$V_{EE} = 0$; $V_{CC} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

	symbol	min.	typ.	max.		condition
Supply voltage	V_{CC}	4,2	5	5,5	V	
Supply current	I_{CC}	–	3,5	–	mA	
Inputs CLB, DLEN, DATA, BLS						
input voltage HIGH	V_{IH}	1,6	–	V_{CC}	V	
input voltage LOW	V_{IL}	−1	–	+ 0,8	V	
maximum input frequency	f_I	–	50	–	kHz	
Input C_{ext}						
input voltage HIGH	V_{IH}	4,6	–	–	V	static mode
input voltage LOW	V_{IL}	−0,1	–	0,4	V	sync. slave mode
input current HIGH	I_{IH}	–	–	180	μA	
input current LOW	I_{IL}	–	–	−40	μA	
Input AC/EL (in slave mode)						
input voltage HIGH	V_{IH}	2,7	–	V_{CC}	V	
input voltage LOW	V_{IL}	−0,4	–	2,3	V	
Output C_{ext} (oscillator mode)						
oscillator frequency	f_{osc}	120	240	360	Hz	C = 22 nF
Output stage backplane (AC/EL)						
output current sink/source	I_O	2,4	–	–	mA	
Output Q_1 to Q_{20}						
output current sink/source	I_O	60	–	–	μA	
d.c. rest voltage between pin 8 (AC/EL) and one of the segment drivers (see Fig. 4)						
segment 'on' situation		–	–	25	mV	
segment 'off' situation		–	–	25	mV	

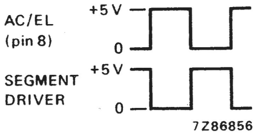


Fig. 4 AC/EL and segment driver pulses.
The d.c. voltage for segment 'on' is about 5 V.

FLUORESCENT DISPLAY/INTERFACE CIRCUIT

GENERAL DESCRIPTION

The SAA1063 is designed to drive the display unit of a digital tuning system. It contains a 17-bit shift register, latches, display multiplexers and output stages, capable of driving 4½ decades of a 7 segment fluorescent display in duplex mode. The decoding for the display is carried out in the data input (microcomputer).

Features

- Driving 4½ decades of a seven segment display in duplex mode.
- Microcomputer compatible.
- 17-bit shift register.
- D.C. and duplex operation.

QUICK REFERENCE DATA

Supply voltage range	V_{CC}		4 to 5,5	V
Operating ambient temperature range	T_{amb}		−20 to +80	°C
Maximum input frequency	f_i	min.	50	kHz
Supply current	I_{CC}	typ.	20	mA
Output current	I_Q	max.	1,5	mA
Maximum output voltage swing	V_{Qmax}	min.	34,5	V

PACKAGE OUTLINE

24-lead DIL; plastic (SOT-101A)

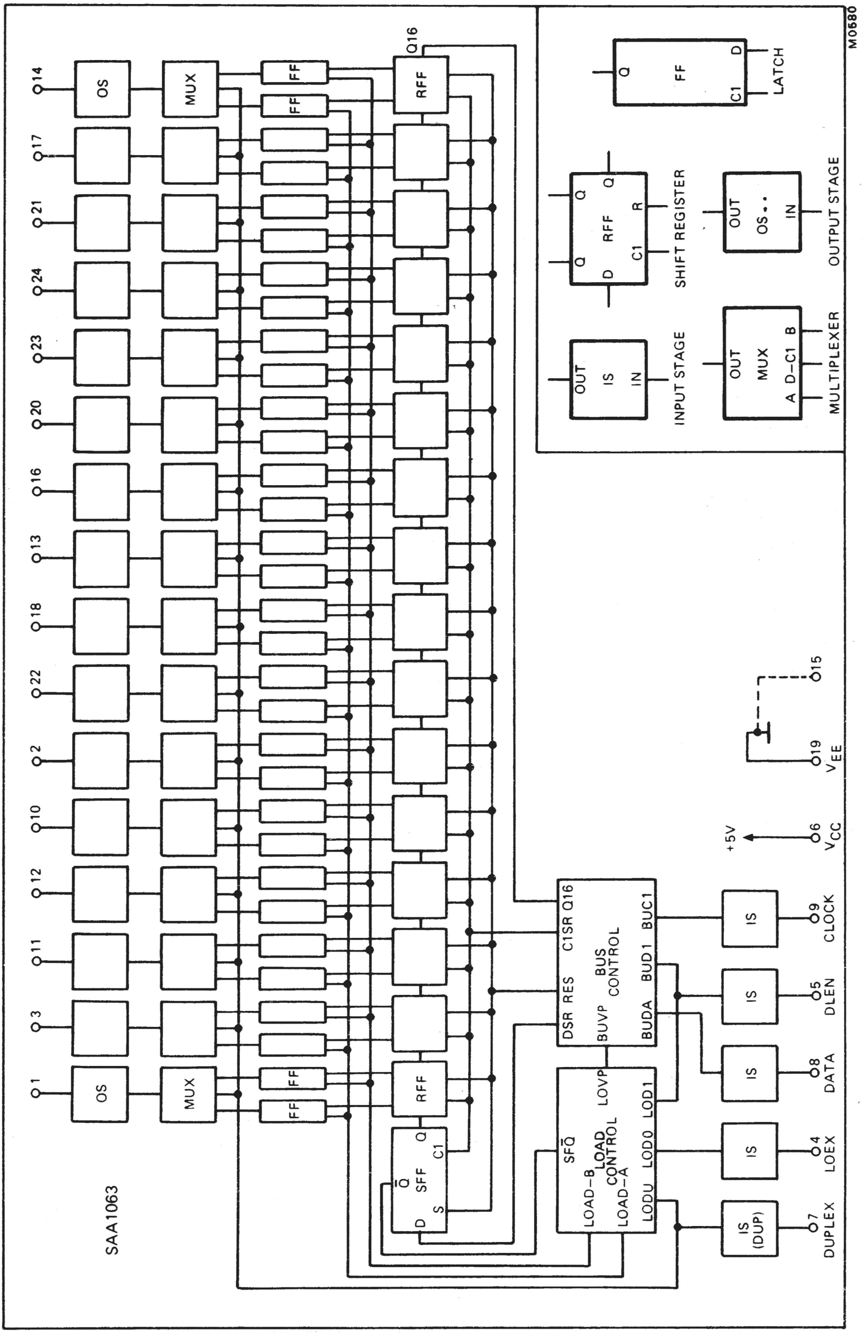

1
3
11
12
10
2
22
18
13
16
20
23
24
21
17
14
OS
MUX
FF
RFF
Q16
SFF
$\bar{Q}$
Q
C1
D
S
SAA1063
LOAD CONTROL
LOAD-B
LOAD-A
SF$\bar{Q}$
LOVP
LOD1
LOD0
LODU
BUS CONTROL
DSR
RES
C1SR
Q16
BUVP
BUDA
BUD1
BUC1
IS
IS (DUP)
9 CLOCK
5 DLEN
8 DATA
4 LOEX
7 DUPLEX
+5V
6 V_{CC}
19 V_{EE}
15
LATCH
SHIFT REGISTER
R
INPUT STAGE
OUT
IN
OUTPUT STAGE
MULTIPLEXER
A
B
D-C1
M0580

Fig. 1 Block diagram.
Insert indicates structure of logic elements.

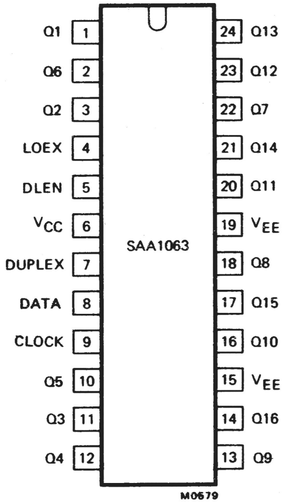

Q1
Q6
Q2
LOEX
DLEN
V_CC
DUPLEX
DATA
CLOCK
Q5
Q3
Q4
1
2
3
4
5
6
7
8
9
10
11
12
SAA1063
24
23
22
21
20
19
18
17
16
15
14
13
Q13
Q12
Q7
Q14
Q11
V_EE
Q8
Q15
Q10
V_EE
Q16
Q9
M0679

Fig. 2 Pinning diagram.

DEVELOPMENT SAMPLE DATA

PINNING

1.	Q1	segment drive outputs	13.	Q9	segment drive outputs
2.	Q6		14.	Q16	
3.	Q2		15.	V_{EE}	ground
4.	LOEX	mode selection	16.	Q10	segment drive outputs
5.	DLEN	bus enable	17.	Q15	
6.	V_{CC}	+5 V power supply	18.	Q8	
7.	DUPLEX	duplex input	19.	V_{EE}	ground
8.	DATA	data input	20.	Q11	segment drive outputs
9.	CLOCK	bus clock input	21.	Q14	
10.	Q5	segment drive outputs	22.	Q7	
11.	Q3		23.	Q12	
12.	Q4		24.	Q13	

OPERATION DESCRIPTION

The input information for this device consists of a data bus with 17 bit words, an external clock synchronized with the data bus and an enable signal. The data format of these signals is given in Fig. 3. These signals are handled by the BUS CONTROL circuit in which the decision is taken as to whether these signals are valid for this device. It contains a leading zero detector (start condition of reception) and a data-length control. Leading zero is detected when the data signal is LOW and the DLEN signal HIGH, during the first HIGH period of the clock signal. During the HIGH period of the DLEN signal, the length control determines if the clock signal consists of 18 pulses. This last function permits the user to supply other information on the same signal lines.

Furthermore the bus control prevents the device accepting interference on the signal lines. If leading zero is detected the shift register is reset and then the data is written into this register. The reset position of the first bit of the register is shifted into the last bit, if the length of the data and the clock input is correct. Incorrect length of the information is detected by checking the value of the last bit of the register. If the data transmission has been accepted properly, the bus control stage generates a valid pulse (LOVP). This pulse enables the load control circuit to load the contents of the register into one of the two latches. When the load bit of the data word is HIGH the register contents are loaded into latch A; when this load bit is LOW the register contents are loaded into latch B. When the data information is accepted this load bit is written into the first bit of the shift register.

In duplex mode the load pulse is synchronised by the duplex signal, to avoid current transients in the output stages during the loading of the latches. The duplex mode operates in one of two mode conditions. When LOEX (pin 4) is LOW the duplex mode condition is selected; when LOEX is HIGH the d.c. mode condition is selected. The output stages are switched to the contents of latch A and latch B respectively.

When the duplex input (pin 7) is LOW the contents of latch A can be found on the output, when this input is HIGH the contents of latch B are found on the output.

In the duplex mode condition the output stages are capable of driving 32 duplexed segments of a fluorescent display. However, in the d.c. mode condition the output stages can only drive 16 segments of the display and two SAA1063 devices are required to drive a 4½ decade display unit.

DEVELOPMENT SAMPLE DATA

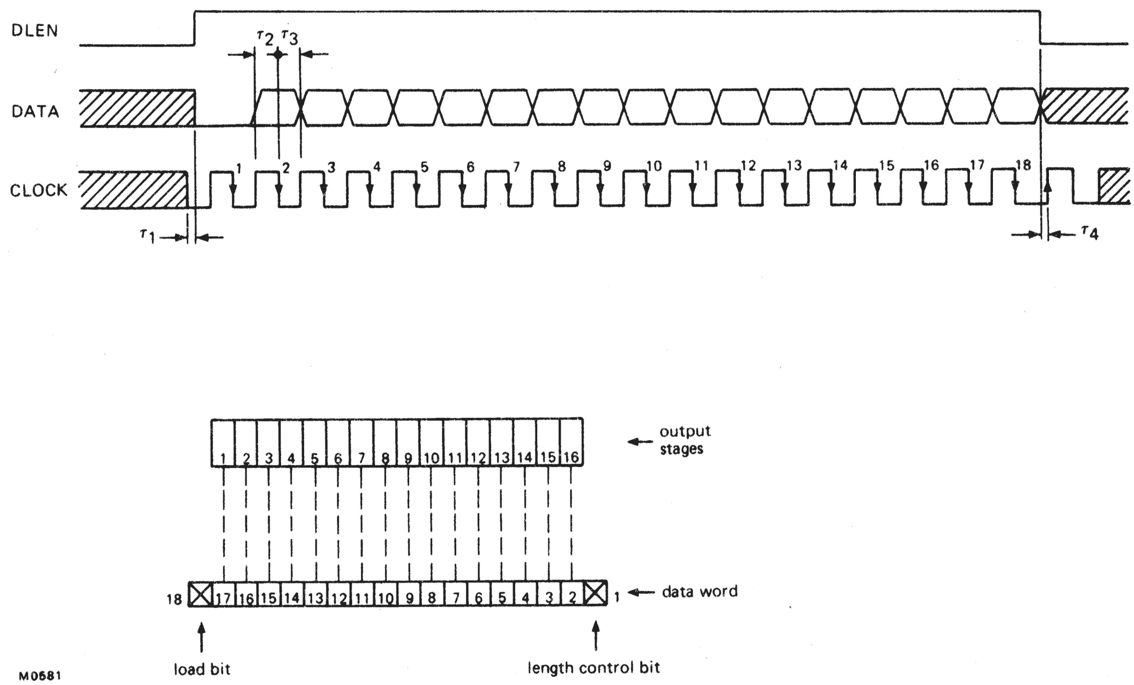

DLEN
DATA
CLOCK
τ_2 τ_3
τ_1
τ_4
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
output stages
18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
data word
load bit
length control bit
M0681

Fig. 3 Organisation of 18-bit data word.

Notes

1. The display segment is blanked by a HIGH data bit.
2. In duplex mode the period between the two data words must be greater than 21 ms.
3. Shaded timing periods are 'don't care' levels.
4. $\tau_1 > 4\ \mu s$ if a continuous clock is used. τ_2 and $\tau_3 > 4\ \mu s$. $\tau_4 > 2\ \mu s$.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{CC}	max.	6	V
Total power dissipation at T_{amb} = 80 °C	P_{tot}	max.	900	mW
Operating ambient temperature range	T_{amb}		−20 to +80	°C
Storage temperature range	T_{stg}		−55 to +125	°C

CHARACTERISTICS

V_{EE} = 0 V; V_{CC} = 5 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.		conditions
Supply voltage	V_{CC}	4	5	5,5	V	
Supply current	I_{CC}	–	20	–	mA	
Inputs LOEX, DLEN, DATA, CLOCK						
input voltage HIGH	V_{IH}	2	–	5	V	
input voltage LOW	V_{IL}	0	–	0,8	V	
input current	$-I_{IH}$	–	–	20	μA	(V_I = 0 V)
max. input frequency	f_i	50	–	–	kHz	
DUPLEX						
input voltage HIGH	V_{IH}	0,8	–	20	V	
input voltage LOW	V_{IL}	−6	–	0,4	V	
input current HIGH	I_{IH}	0,01	–	12	mA	
input frequency	f_i	–	50	–	Hz	
Outputs Q1 to Q16						
output voltage HIGH	$-V_{OH}$	30	–	–	V	$I_O < 0,7$ μA
output voltage LOW	V_{OL}	4,5	–	–	V	I_O = 1 mA
output current	I_{OL}	–	–	1,5	mA	

TUNER SWITCHING CIRCUIT

The SAA1300 is for switching on and off the supply lines of various circuit parts via an I^2C bus signal. Furthermore, it can be used to supply current for switching diodes in radio and television tuners. It contains 5 output stages, which are capable of supplying up to 100 mA in the ON state or sinking up to −100 μA in the OFF state.

Current limiting and short-circuit protection are included. The output stages are driven by a shift register/latch combination which is loaded via data from the I^2C bus. A power-on reset of the latches ensures the OFF state of the output stages (OUT 2 to OUT 5) without data reception from the I^2C bus. A subaddressing system allows the connection of up to three circuits on the same I^2C bus lines; one of the outputs (OUT 1, pin 7) can also be used as an input to select the device via a simple internal A/D converter.

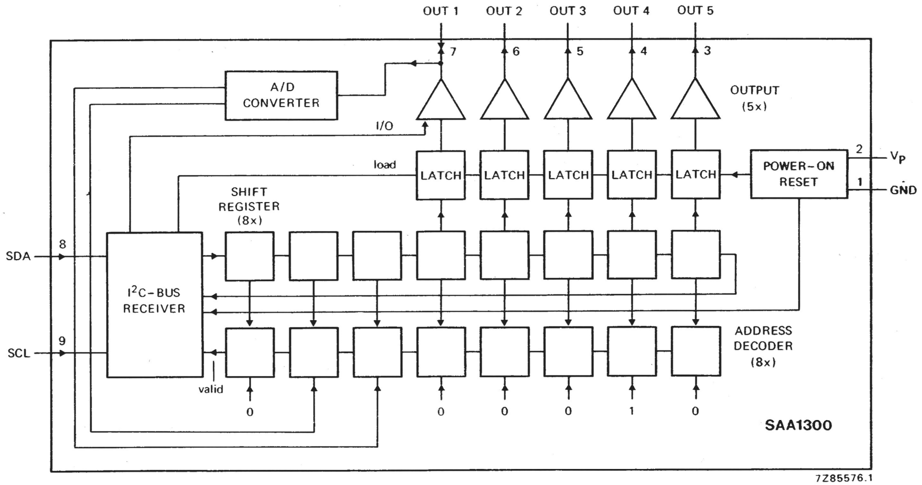

OUT 1
OUT 2
OUT 3
OUT 4
OUT 5
7
6
5
4
3
A/D CONVERTER
OUTPUT (5x)
I/O
load
LATCH
LATCH
LATCH
LATCH
LATCH
POWER–ON RESET
2
V_P
1
GND
SHIFT REGISTER (8x)
SDA
8
I^2C–BUS RECEIVER
SCL
9
valid
ADDRESS DECODER (8x)
0
0
0
0
1
0
SAA1300
7Z85576.1

Fig. 1 Block diagram.

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142B).

PINNING

pin no.	symbol	function
1	GND	ground
2	V_P	positive supply
3	OUT 5	outputs
4	OUT 4	
5	OUT 3	
6	OUT 2	
7	OUT 1	output and subaddressing input
8	SDA	serial data line } I^2C bus
9	SCL	serial clock line

I^2C BUS INFORMATION*

Address, first byte

0 1 0 0 0 A B 0 where,

A	B	function	condition
0	0	general address	OUT 1 = output
0	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,L}$ (LOW)
1	0	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,H}$ (HIGH)
1	1	OUT 1 = input	address accepted if $V_{OUT\,1} = V_{OUT\,M}$ (MEDIUM)

Data, second byte

OUT 5, OUT 4, OUT 3, OUT 2, OUT 1, X, X, X

The I/O output stage (OUT 1) is switched as an input stage after a power-on reset. It depends on the contents of the first data transmission whether the output stage is switched as an output or remains as an input.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	13,2	V
Input voltage range at SDA, SCL	V_I		−0,5 to + 13,7	V
Input voltage range at OUT 1	V_I		−0,5 to + 12,5	V
Output voltage range at OUT 1 to OUT 5	V_O		−0,5 to + 12,5	V
Input current at SDA, SCL	I_I	max.	20	mA
Input current at OUT 1	I_I	max.	20	mA
Total power dissipation	P_{tot}	max.	650	mW
Storage temperature range	T_{stg}		−40 to + 125	°C
Operating ambient temperature range	T_{amb}		−20 to + 80	°C

---

* Detailed information is given in a separate data sheet.

CHARACTERISTICS

V_P = 8 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 2)					
Supply voltage range	V_P	4	–	12	V
Supply current	I_P	–	10	–	mA
Power-on reset level output stage in "OFF" condition	V_{PR}	–	–	3,5	V
Maximum power dissipation*	P_{max}	–	650	–	mW
Inputs SDA, SCL (pins 8 and 9)					
Input voltage HIGH	V_{IH}	2,8	–	$V_P + 0,5$	V
Input voltage LOW	V_{IL}	0	–	1,8	V
Input current HIGH	$-I_{IH}$	–	–	50	μA
Input current LOW	I_{IH}	–	–	0,1	μA
Acknowledge sink current	I_{ACK}	–	–	2,5	mA
Maximum input frequency	$f_{i\,max}$	100	–	–	kHz
Outputs OUT 1 to OUT 5 (pins 3 to 7)					
Maximum output current; source : "ON"	I_{Oso}	+ 100	–	+ 150	mA
Output voltage HIGH at I_{Oso}	V_{OH}	–	–	$V_P - 2$	V
Output current; sink: "OFF"	I_{Osi}	–100	–300	–	μA
Output voltage LOW at I_{Osi}	V_{OL}	–	–	100	mV
Output voltage MEDIUM at I_O = 12,5 mA	V_{OM}	–	–	$V_P - 0,5$	V
OUT 1 used as subaddressing input					
Input voltage HIGH (code 1 0)	$V_{OUT\,1H}$	0,72 V_P	–	V_P	V
Input voltage MEDIUM (code 1 1)	$V_{OUT\,1M}$	0,39 V_P	–	0,61 V_P	V
Input voltage LOW (code 0 1)	$V_{OUT\,1L}$	0	–	0,28 V_P	V

---

* Outputs must not be driven simultaneously at maximum source current.

LOW-LEVEL AMPLIFIER

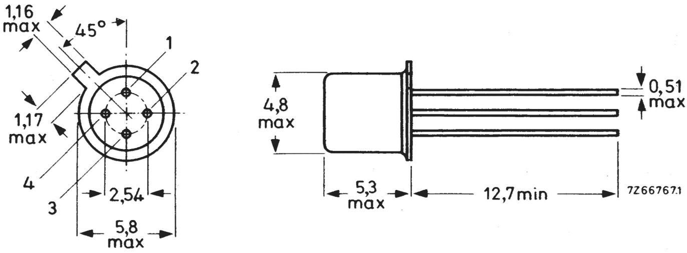
The TAA263 is a semiconductor integrated amplifier in a 4-lead TO-72 metal envelope. It comprises a three-stage, direct coupled low-level amplifier for use from d.c. up to frequencies of 600 kHz.

QUICK REFERENCE DATA				
Supply voltage	V_B	max.	8	V
Output voltage	V_{3-4}	max.	7	V
Output current	I_3	max.	25	mA
Transducer gain at P_o = 10 mW				
R_L = 150 Ω; f = 1 kHz	G_{tr}	typ.	77	dB
Operating ambient temperature	T_{amb}		−20 to +100	°C

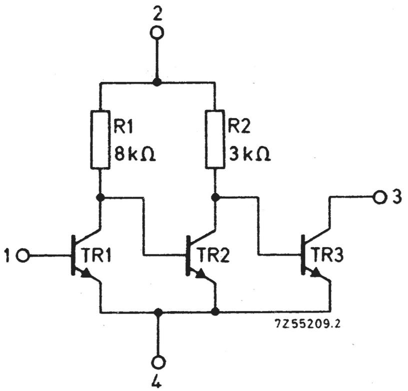
PACKAGE OUTLINE

Dimensions in mm

TO-72 (SOT-18/17)

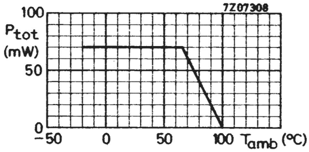

1,16 max
45°
1
2
1,17 max
4
3
2,54
5,8 max
4,8 max
0,51 max
5,3 max
12,7min
7Z66767.1

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages				
Supply voltage	V_B	max.	8	V
Output voltage	V_{3-4}	max.	7	V
Input voltage	$-V_{1-4}$	max.	5	V
Currents				
Output current	I_3	max.	25	mA
Input current	I_1	max.	10	mA
Power dissipation				
Total power dissipation up to T_{amb} = 65 °C	P_{tot}	max.	70	mW

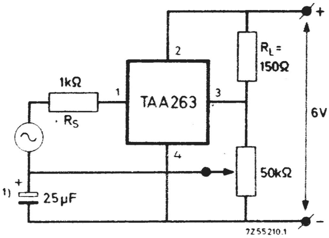


Temperatures			
Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature (see derating curve above)	T_{amb}	−20 to +100	°C

CHARACTERISTICS

T_{amb} = 25 °C

Test circuit:


1kΩ
R_S
1
TAA263
2
3
4
R_L = 150Ω
6V
50kΩ
+
1)
25μF
+
−
7Z55210.1

Currents				
Output current	I_3	typ.	12	mA
Total current drain (no signal)	I_2+I_3	<	16	mA
Over-all small signal current gain				
f = 1 kHz	$h_{f\ tot}$	typ.	5.10^5	
Transducer gain				
f = 1 kHz; P_o = 10 mW	G_{tr}	>	70	dB
		typ.	77	dB
Output power at f = 1 kHz; d_{tot} = 10%	P_o	>	10	mW
d_{tot} = 5%	P_o	>	8	mW
Noise figure				
f = 400 Hz to 6 kHz	F	typ.	5	dB
		<	10	dB
f = 450 kHz; Δf = 5 kHz	F	typ.	2.7	dB

---

[1] $Z \leqslant 10\ \Omega$ at f = 1 kHz

CHARACTERISTICS (continued) $T_{amb} = 25\ ^{o}C$

y parameters (point 4 common connection)

$V_B = 6\ V;\ I_3 = 3\ mA;\ V_{3-4} = 4.2\ V$

f = 1 kHz				
Input admittance	$y_i = g_i$	typ.	20	$\mu\Omega^{-1}$
Transfer admittance	$y_f = g_f$	typ.	11	Ω^{-1}
Output admittance	$y_o = g_o$	typ.	60	$\mu\Omega^{-1}$
f = 450 kHz				
Input conductance	g_i	typ.	15	$\mu\Omega^{-1}$
Input capacitance	C_i	typ.	14	pF
Transfer admittance	$\lvert y_f \rvert$	typ.	9.4	Ω^{-1}
Phase angle of transfer admittance	φ_f	typ.	125^o	
Output conductance	g_o	typ.	20	$\mu\Omega^{-1}$
Output capacitance	C_o	typ.	13	pF

INTEGRATED MOST AMPLIFIER

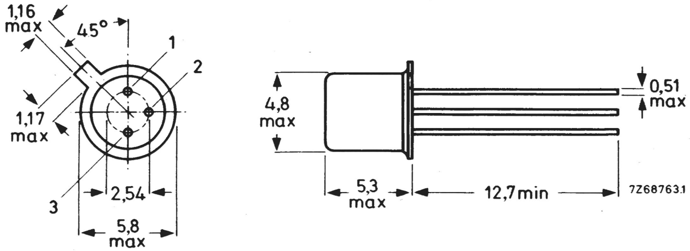
The TAA320 is a silicon monolithic integrated circuit, consisting of a MOS transistor and an n-p-n transistor in a TO-18 metal envelope.
The device is primarily intended for audio amplifiers with a very high input resistance (e.g. for crystal pick-ups).
Besides this application the TAA320 is also suitable for other applications where a high input resistance is required, like impedance converters, timing circuits, microphone-amplifiers, etc.

QUICK REFERENCE DATA				
Drain-source voltage (V_{GS} = 0)	$-V_{DSS}$	max.	20	V
Drain current	$-I_D$	max.	25	mA
Gate-source voltage $-I_D$ = 10 mA; $-V_{DS}$ = 10 V	$-V_{GS}$	typ.	11	V
Gate-source resistance $-V_{GS}$ up to 20 V; T_j up to 125 °C	r_{GS}	>	100	GΩ
Transfer admittance at f = 1 kHz $-I_D$ = 10 mA; $-V_{DS}$ = 10 V	$\|y_{fs}\|$	typ.	75	mΩ^{-1}

PACKAGE OUTLINE

Dimensions in mm

TO-18 (SOT-18/13)

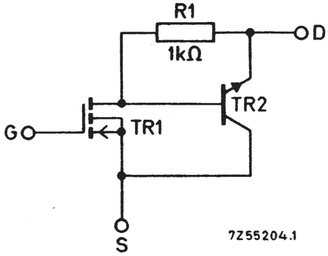


1 = drain
2 = gate
3 = source

Source connected to the case

Accessories supplied on request: 56246, 56263

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Drain-source voltage (V_{GS} = 0)	$-V_{DSS}$	max.	20	V
Gate-source voltage (I_D = 0)	$-V_{GSO}$	max.	20	V
Non repetitive peak gate-source voltage (t ≤ 10 ms)	$-V_{GSM}$	max.	100	V

Current

Drain current	$-I_D$	max.	25	mA

Power dissipation

Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	200	mW

Temperatures

Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature (see derating curve on page 8)	T_{amb}	−20 to +125	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	0.5	°C/mW

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain current				
$-V_{DS}$ = 20 V; V_{GS} = 0	$-I_{DSS}$	typ. <	5 1	nA μA
Gate-source voltage [1]				
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V	$-V_{GS}$	typ. 9 to	11 14	V V
Gate-source resistance				
$-V_{GS}$ up to 20 V; T_j up to 125 °C	r_{GS}	>	100	GΩ
Equivalent noise voltage				
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V B = 50 Hz to 15 kHz	v_n	typ.	25	μV
y parameters at f = 1 kHz				
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V				
Transfer admittance	$\lvert y_{fs} \rvert$	typ. 40 to	75 120	$m\Omega^{-1}$ $m\Omega^{-1}$
Input capacitance	C_{is}	typ.	8	pF
Feedback capacitance	$-C_{rs}$	typ.	1.5	pF
Output conductance	g_{os}	typ.	0.65	$m\Omega^{-1}$

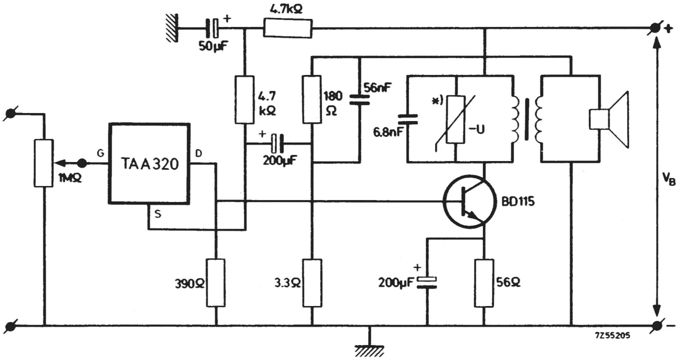
NOTE

To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the leads of the device have been short circuited by a clip. The clip has been arranged so that it need not be removed until the device has been mounted in the circuit.

---

1) $-V_{GS}$ decreases about 6 mV/°C with increasing ambient temperature at a constant $-I_D$.

APPLICATION INFORMATION 2 W audio amplifier with TAA320 and BD115



* The voltage dependent resistor (2322 552 03381) suppresses voltage transients that might otherwise exceed the safe operating limits of the BD115.

Supply voltage	V_B	=	100	V
Collector current of BD115	I_C	typ.	50	mA
Drain current of TAA320	$-I_D$	typ.	9.5	mA
Primary d.c. resistance of output transformer			140	Ω
Primary inductance of output transformer			2.7	H
A.C. collector load for BD115			1.8	kΩ

Performance at f = 1 kHz; feedback = 16 dB

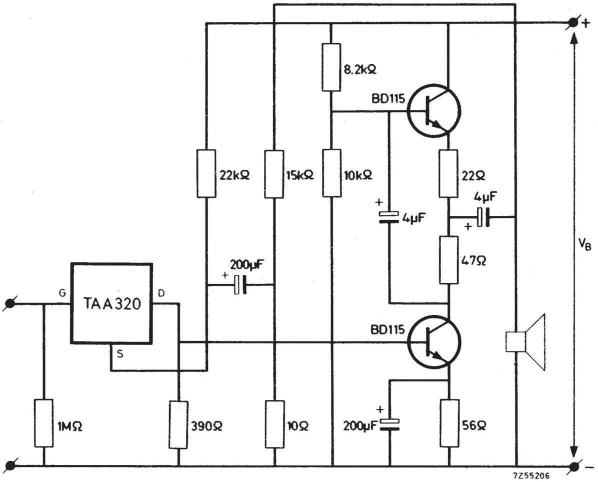
Output power at d_{tot} = 10% (on primary of the output transformer)	P_o	typ.	2.6	W
Input voltage for P_o = 50 mW	$V_{i(rms)}$	typ.	13.5	mV
Input voltage for P_o = 2 W	$V_{i(rms)}$	typ.	86	mV
Total distortion at P_o = 2 W	d_{tot}	typ.	3.6	%
Minimum frequency response (–3 dB)		60 Hz to	20	kHz
Signal-noise ratio at P_o = 2 W		typ.	73	dB

Mounting instruction for BD115

Proper continuous operation is ensured up to T_{amb} = 50 °C, provided the BD115 is directly mounted on a 1.5 mm blackened Al. heatsink of 30 cm^2 with a clamping washer of type 56218.
If the transistor is mounted on a heatsink with a mica washer, the heatsink should have an area of 50 cm^2.
Recommended diameter of hole in heatsink: 7.7 mm.

APPLICATION INFORMATION (continued)

4 W audio amplifier with TAA320 and 2 transistors of type BD115.



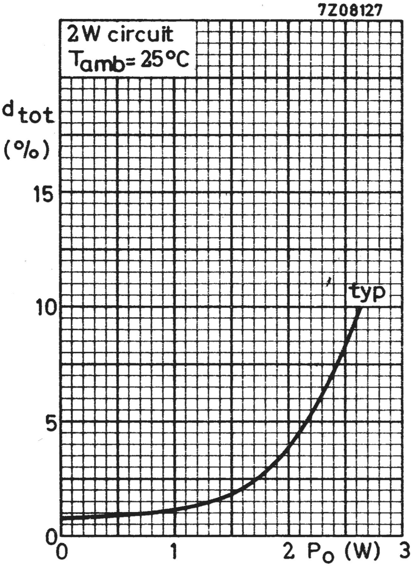
+
–
8.2kΩ
BD115
22kΩ
15kΩ
10kΩ
22Ω
4μF
4μF
47Ω
V_B
200μF
G
TAA320
D
S
BD115
1MΩ
390Ω
10Ω
200μF
56Ω
7Z55206

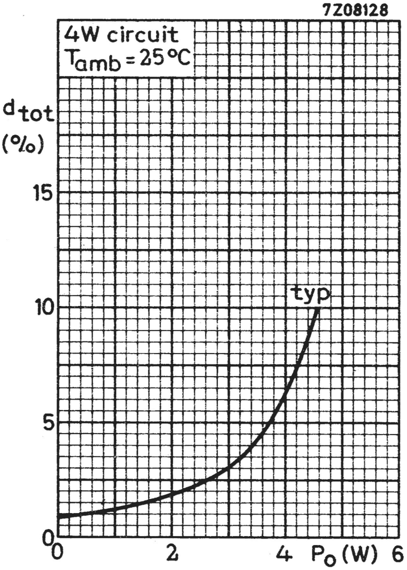
Supply voltage	V_B	=	200	V
Collector current of a BD115	I_C	typ.	52	mA
Drain current of TAA320	$-I_D$	typ.	8.6	mA

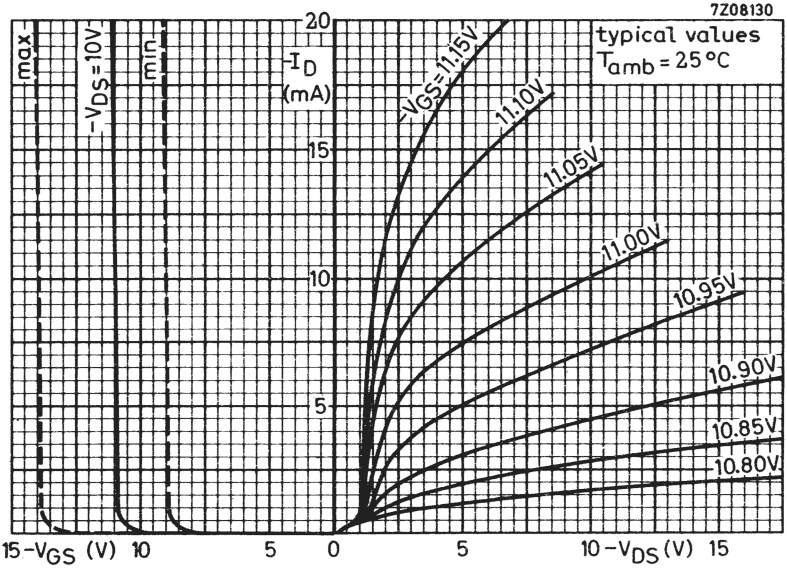
Performance at f = 1 kHz; feedback = 12 dB

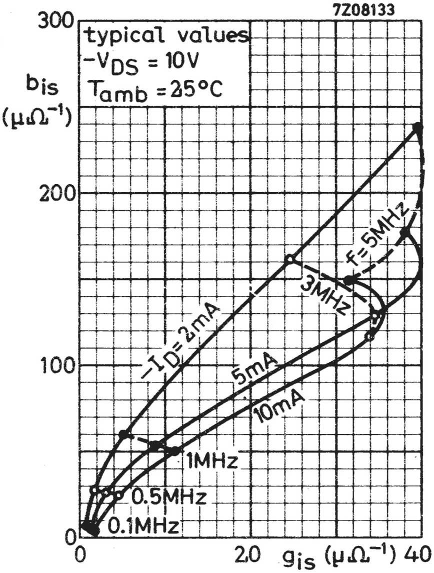
Output power at d_{tot} = 10%	P_o	typ.	4.5	W
Input voltage for P_o = 50 mW	$V_{i(rms)}$	typ.	7.5	mV
Input voltage for P_o = 4 W	$V_{i(rms)}$	typ.	67	mV
Total distortion at P_o = 4 W	d_{tot}	typ.	6	%
Minimum frequency response (–3 dB)		50 Hz to 20		kHz
Signal-noise ratio at P_o = 4 W		typ.	73	dB

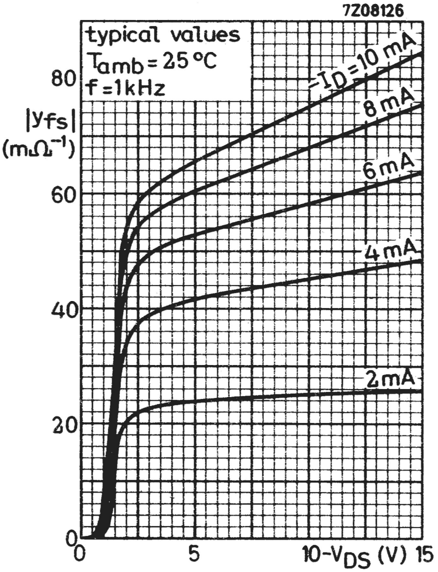
Mounting instruction for BD115 see page 4

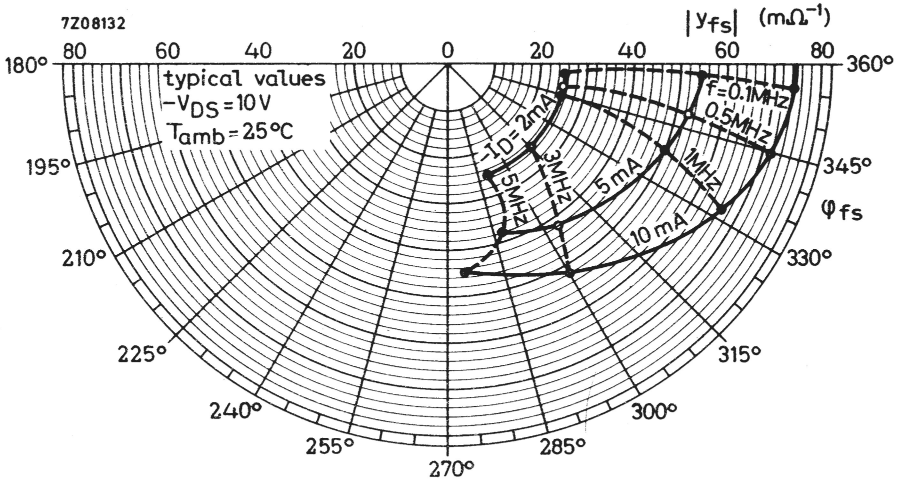

7Z08127
2W circuit
T_{amb}= 25°C
d_{tot} (%)
15
10
5
0
typ
0
1
2
3
P_o (W)

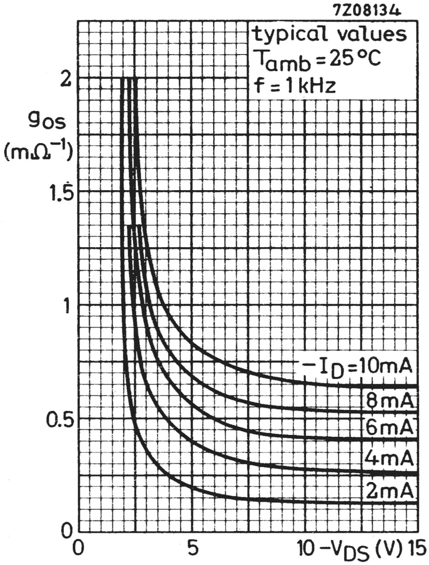

7Z08128
4W circuit
T_{amb} = 25°C
d_{tot} (%)
15
10
5
0
typ
0
2
4
6
P_o (W)

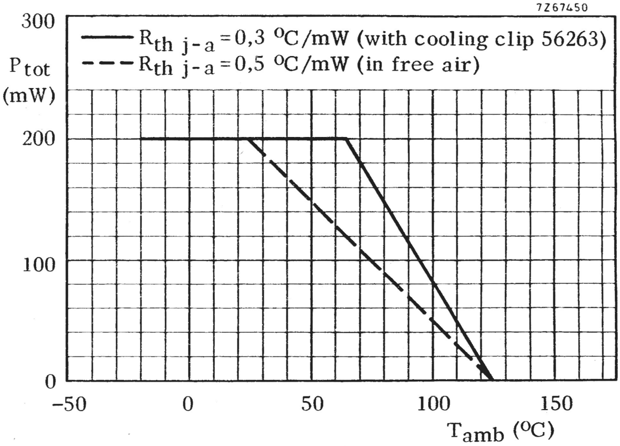

7Z08130
typical values
T_{amb} = 25°C
max
$-V_{DS}$ = 10V
min
$-I_D$ (mA)
20
15
10
5
$-V_{GS}$ = 11.15V
11.10V
11.05V
11.00V
10.95V
10.90V
10.85V
10.80V
15
$-V_{GS}$ (V)
10
5
0
5
10
$-V_{DS}$ (V)
15

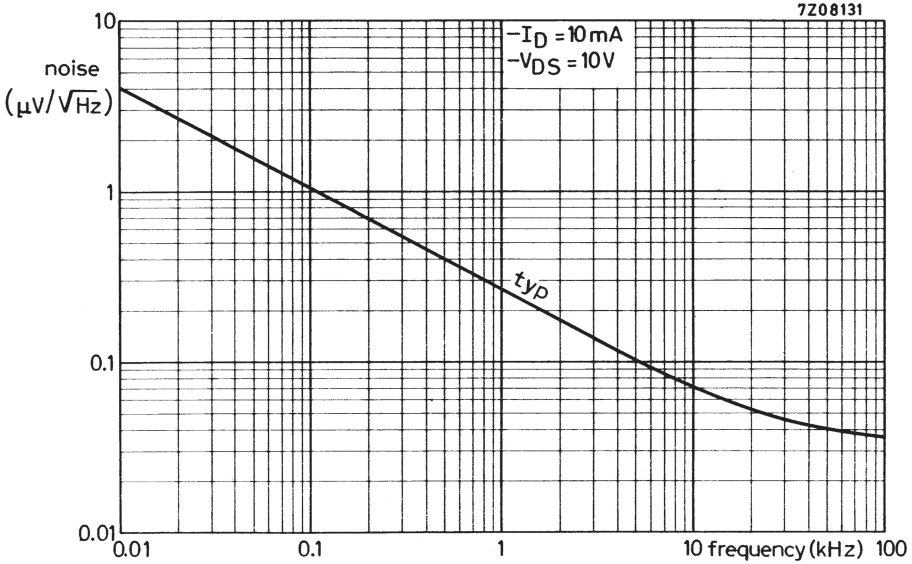

7Z08133
typical values
$-V_{DS}$ = 10V
T_{amb} = 25°C
b_{is} ($\mu\Omega^{-1}$)
300
200
100
0
0
2.0
g_{is} ($\mu\Omega^{-1}$)
40
$-I_D$ = 2mA
5mA
10mA
f = 5MHz
3MHz
1MHz
0.5MHz
0.1MHz


7Z08126
typical values
T_{amb} = 25 °C
f = 1kHz
$|y_{fs}|$ ($m\Omega^{-1}$)
80
60
40
20
0
0
5
10
$-V_{DS}$ (V)
15
$-I_D$ = 10 mA
8 mA
6 mA
4 mA
2 mA


7Z08132
$|y_{fs}|$ ($m\Omega^{-1}$)
80
60
40
20
0
20
40
60
80
180°
360°
typical values
$-V_{DS}$ = 10 V
T_{amb} = 25°C
195°
210°
225°
240°
255°
270°
285°
300°
315°
330°
345°
φ_{fs}
$-I_D$ = 2mA
5 mA
10 mA
f = 0.1MHz
0.5MHz
1MHz
3MHz
5MHz


7Z08134
typical values
T_{amb} = 25 °C
f = 1 kHz
g_{os}
(mΩ^{-1})
2
1.5
1
0.5
0
0
5
10
$-V_{DS}$ (V)
15
$-I_D$ = 10mA
8mA
6mA
4mA
2mA


7Z67450
$R_{th\ j-a}$ = 0,3 °C/mW (with cooling clip 56263)
$R_{th\ j-a}$ = 0,5 °C/mW (in free air)
300
P_{tot}
(mW)
200
100
0
−50
0
50
100
150
T_{amb} (°C)


7Z08131
noise (μV/√Hz)
10
1
0.1
0.01
−I_D = 10 mA
−V_DS = 10 V
typ
0.01
0.1
1
10
frequency (kHz)
100

INTEGRATED MOST LEVEL SENSOR

The TAA320A is a silicon monolithic integrated circuit, consisting of a p-channel enhancement type MOS transistor and an n-p-n transistor, in a TO-18 metal envelope. The device is intended for level sensors with a very high input resistance (e.g. timing circuits, thermostats, liquid level sensors, flame control circuits).

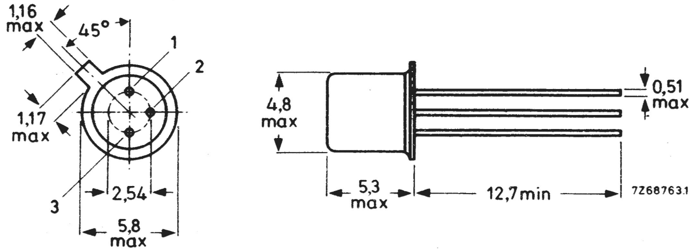
QUICK REFERENCE DATA

Drain-source voltage (V_{GS} = 0)		$-V_{DSS}$	max.	20	V
Drain current		$-I_D$	max.	60	mA
Gate-source voltage [1] $-I_D$ = 10 mA; $-V_{DS}$ = 10 V	group 1:	$-V_{GS}$	typ.	10, 6	V
				10, 0 to 11, 2	V
	group 2:	$-V_{GS}$	typ.	11, 3	V
				10, 7 to 11, 9	V
	group 3:	$-V_{GS}$	typ.	12, 0	V
				11, 4 to 12, 6	V
	group 4:	$-V_{GS}$	typ.	12, 7	V
				12, 1 to 13, 3	V
Gate cut-off current at T_{amb} = 25 °C $-V_{GS}$ = 20 V; I_D = 0		$-I_{GSO}$	typ.	1	pA
$-V_{GS}$ = 20 V; V_{DS} = 0		$-I_{GSS}$	typ.	1	pA

PACKAGE OUTLINE

Dimensions in mm

TO-18 (SOT-18/13)



1 = drain
2 = gate
3 = source

source connected to the case

Accessories supplied on request: 56246; 56263

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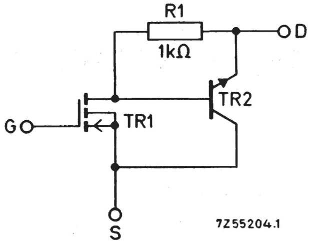
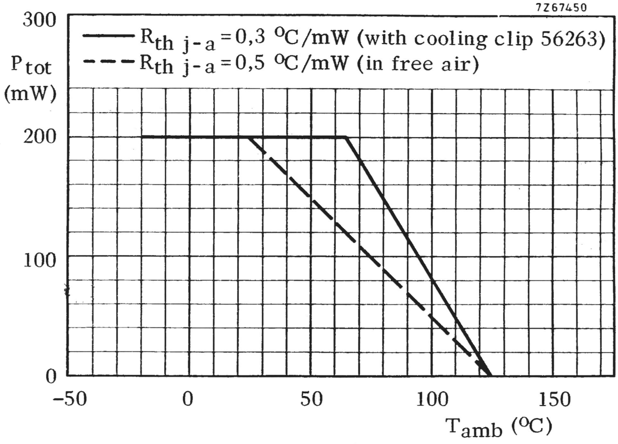
[1] For explanation of the group codefication see note b on page 3.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage (V_{GS} = 0)	$-V_{DSS}$	max.	20	V
Gate-source voltage (I_D = 0)	$-V_{GSO}$	max.	20	V
Non-repetitive peak gate-source voltage ($t \leq 10$ ms)	$\pm V_{GSM}$	max.	100	V
Current				
Drain current	$-I_D$	max.	60	mA
Peak drain current ($t <$ 200 ms; δ 0,001)	$-I_{DM}$	max.	100	mA
Temperatures				
Storage temperature	T_{stg}		−65 to +125	°C
Operating ambient temperature (see curve below)	T_{amb}		−20 to +125	°C



CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain current					
$-V_{DS}$ = 20 V; V_{GS} = 0		$-I_{DSS}$	typ. <	5 1	nA µA
Drain-source voltage [1]					
$-I_D$ = 10 mA; $-V_{GS}$ = 20 V		$-V_{DS}$	<	1	V
$-I_D$ = 60 mA; $-V_{GS}$ = 20 V		$-V_{DS}$	<	1,5	V
Gate-source voltage (see note b)					
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V	group 1:	$-V_{GS}$	typ. 10,0 to	10,6 11,2	V V
	group 2:	$-V_{GS}$	typ. 10,7 to	11,3 11,9	V V
	group 3:	$-V_{GS}$	typ. 11,4 to	12,0 12,6	V V
	group 4:	$-V_{GS}$	typ. 12,1 to	12,7 13,3	V V
Gate cut-off current					
$-V_{GS}$ = 20 V; I_D = 0		$-I_{GSO}$	typ.	1	pA [2]
$-V_{GS}$ = 20 V; V_{DS} = 0		$-I_{GSS}$	typ.	1	pA [2]

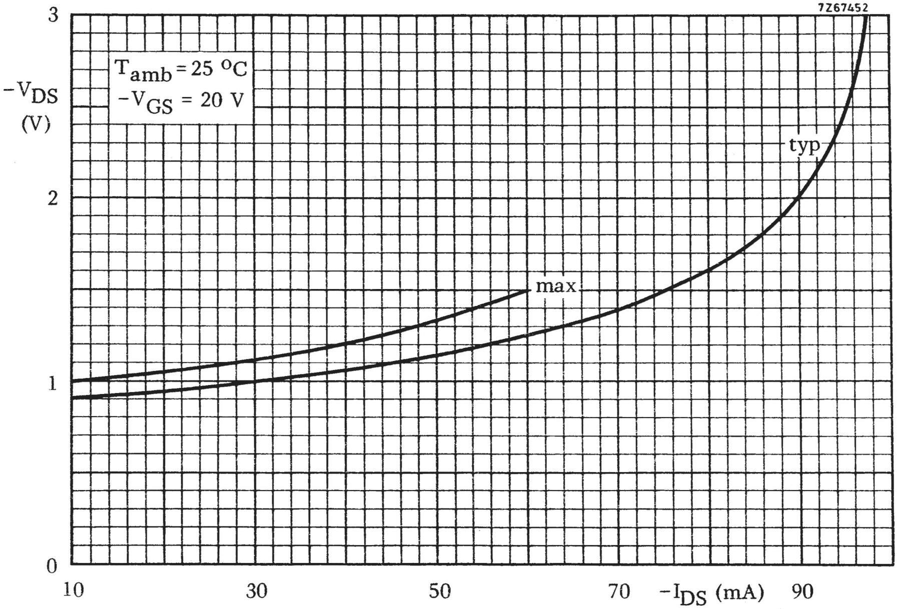
NOTES

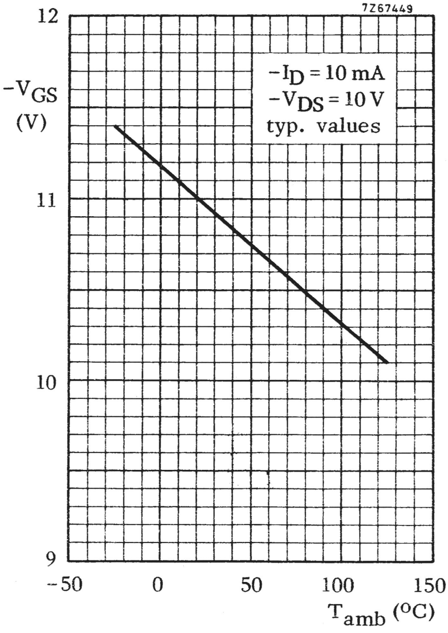
a. The leads are short-circuited by a clip to protect the oxide layer against damage due to accumulation (or build-up) of electrostatic charge on the high resistance gate electrode. The clip should not be removed until after the device is mounted.

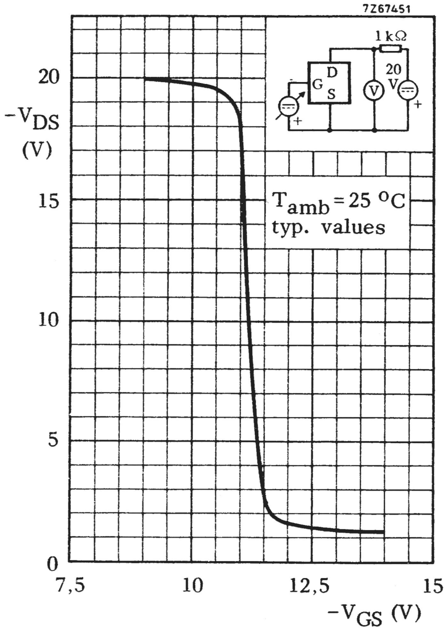
b. As a service to the customer the $-V_{GS}$ group to which a device belongs is identified by a numerical suffix (1, 2, 3 or 4), however, individual groups cannot be ordered separately.

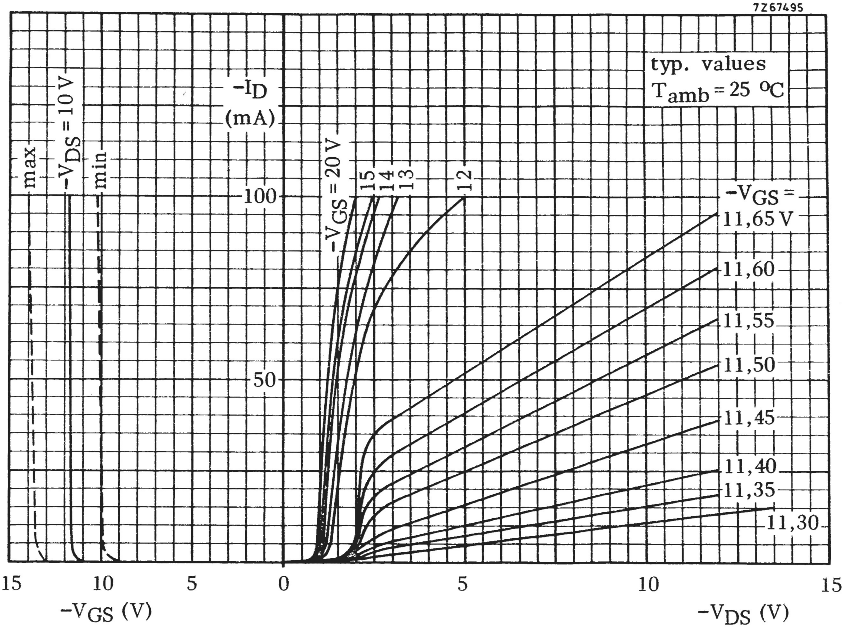
---

1. See also upper graph on page 4.
2. Being dependent on handling and ambient humidity, the quoted value applies only up to the time of shipping.
   Efficient drying treatment is advised before the device is mounted, provided the application requires this low current.


7Z67452
$T_{amb} = 25\ ^oC$
$-V_{GS} = 20\ V$
$-V_{DS}$ (V)
3
2
1
0
max
typ
10
30
50
70
$-I_{DS}$ (mA)
90


7Z67449
$-I_D = 10\ mA$
$-V_{DS} = 10\ V$
typ. values
$-V_{GS}$ (V)
12
11
10
9
-50
0
50
100
150
T_{amb} (°C)


7Z67451
1 kΩ
D
G
S
V
20 V
+
$T_{amb} = 25\ ^oC$
typ. values
$-V_{DS}$ (V)
20
15
10
5
0
7,5
10
12,5
15
$-V_{GS}$ (V)


7Z67495
typ. values
T_{amb} = 25 °C
$-I_D$ (mA)
100
50
max
$-V_{DS}$ = 10 V
min
$-V_{GS}$ = 20 V
15
14
13
12
$-V_{GS}$ =
11,65 V
11,60
11,55
11,50
11,45
11,40
11,35
11,30
15
10
5
0
5
10
15
$-V_{GS}$ (V)
$-V_{DS}$ (V)

INTEGRATED AM/FM RADIO RECEIVER CIRCUIT

The TBA570A is for use in small low-cost a.m. portable receivers as well as in high-quality battery or mains-fed a.m. and a.m./f.m. receivers. The IC incorporates: a.m. mixer, oscillator, i.f. amplifier, a.g.c. amplifier, a.m. detector and capacitor, f.m./i.f. limiting amplifier and stable base bias for f.m. front-end, and an audio preamplifier and driver.

The unique integrated audio part has an internally limited bandwidth (18 kHz) and negligible h.f. radiation back to the ferrite rod. This makes the TBA570A ideally suitable for small size a.m. receivers because print layout is not critical. The driver stage can directly drive complementary output stages (P_o = 6 W max.), or operate as a post amplifier (V_o = 500 mV).

In its standard applications, the TBA570A can replace the TBA570.

QUICK REFERENCE DATA

Applicable supply voltage range of receiver	V_S		2,7 to 18	V
Supply voltage range (pin 8)	V_P		3,6* to 5,4	V
Ambient temperature	T_{amb}		25	°C
Supply voltage (pin 8)	V_P	nom.	5,4	V
Total quiescent current except output stages, driver stage TR30 and f.m. front-end	I_{tot}	typ.	9	mA
A.M. performance (at pin 2)				
Sensitivity (V_o at pin 5; V_i at pin 2)				
for V_o = 30 mV	V_i		3,0 to 12	μV
range 1**	V_i		5,5 to 12	μV
range 2**	V_i		3,0 to 7	μV
R.F. input voltage				
for S/N = 26 dB	V_i	typ.	18	μV
for P_o = 50 mW (adjustable)	V_i	typ.	2	μV
A.G.C. range; change of r.f. input voltage for 10 dB expansion in audio range		typ.	65	dB
R.F. signal handling; d_{tot} = 10%; m = 0,8		typ.	150	mV
F.M. performance (at pin 2)				
R.F. input voltage; 3 dB before limiting	V_i	typ.	50	μV
Audio performance				
Output driver current (peak value)	I_{11M}	<	100	mA
Input impedance (at pin 12)	$\lvert Z_{12-16} \rvert$	typ.	100	kΩ

* Minimum supply voltage for guaranteed oscillator operation: V_P = 2,5 V.

** There are two ranges of sensitivity measured, and indicated by either '1' or '2' on the package. Ordering a specific range is not possible.

PACKAGE OUTLINES

TBA570A: 16-lead DIL; plastic (SOT-38).
TBA570AQ: 16-lead QIL; plastic (SOT-58).

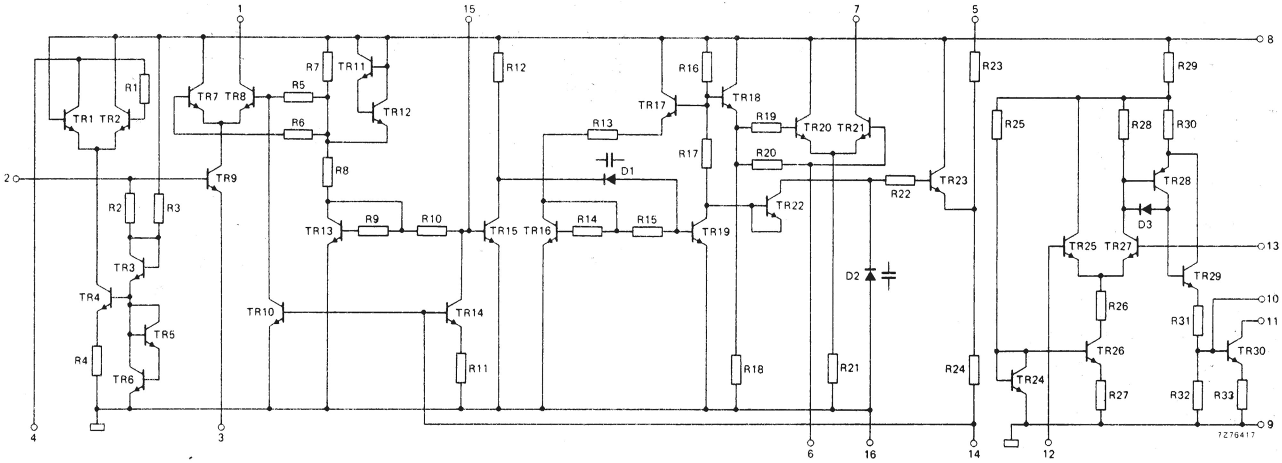

1
15
7
5
8
2
4
3
6
16
14
12
13
10
11
9
TR1 TR2
TR3
TR4
TR5
TR6
TR7 TR8
TR9
TR10
TR11
TR12
TR13
TR14
TR15 TR16
TR17
TR18
TR19
TR20 TR21
TR22
TR23
TR24
TR25 TR27
TR26
TR28
TR29
TR30
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
D1
D2
D3
7Z76417

Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_{8\text{-}16} = V_P$	max.	7	V
Voltage pin 11	$V_{11\text{-}9}$	max.	18	V
Current pin 11 (peak value)	I_{11M}	max.	100	mA
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 125		°C
Operating ambient temperature; $V_{8;\,4;\,7;\,1\text{-}16} = 7$ V; $I_{11M} = 100$ mA; see also derating curve Fig. 2	T_{amb}	−20 to + 85		°C

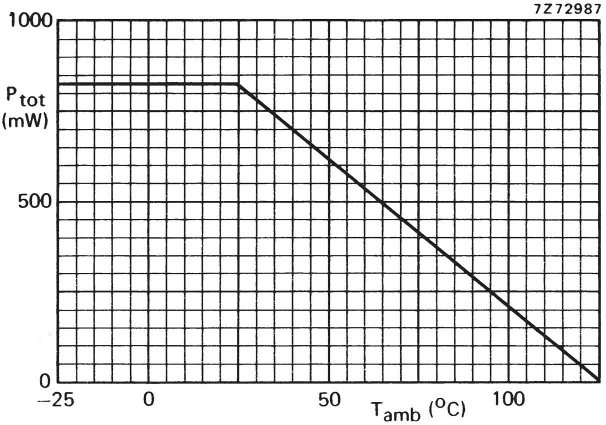


Fig. 2 Total power dissipation derating curve.

DESIGN DATA

Characteristics of integrated components are determined by process and layout data. Pins not under measuring conditions should not be connected.

Voltages with respect to pin 9 and 16 (tolerated minimum: 0 V)

Pins 1 and 7	$V_{1\text{-}9(16)}$ $V_{7\text{-}9(16)}$	max.	18	V
Pin 4	$V_{4\text{-}9(16)}$	V_P −0,5 to V_P +0,5		V
Pin 8	$V_P = V_{8\text{-}9(16)}$	max.	7	V
Pin 3	$V_{3\text{-}9(16)}$	max.	3	V
Pin 5	$V_{5\text{-}9(16)}$	max.	4	V
Pin 14	$V_{14\text{-}9(16)}$	max.	1	V

Currents (tolerated minimum: 0 mA)

Pins 2, 6, 12, 13 and 15	I_2; I_6; I_{12} I_{13}; I_{15}	max.	80	μA
Pin 10	I_{10}	max.	5	mA

D.C. CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$

Saturation voltage of driver stage $I_C = 50$ mA; $I_B = 2,5$ mA	$V_{11\text{-}16sat}$	typ. $<$	1,0 1,5	V V
Collector breakdown voltage of driver stage $I_C = 25$ mA; $R_{BE} = 7\ k\Omega$	$V_{11\text{-}16(BR)}$	$>$	18	V
D.C. current gain of driver stage $I_C = 50$ mA	h_{FE}	$>$	25	
Total quiescent current except driver stage collector current; f.m. front-end; discrete output stages				
$V_P = 5,4$ V	I_{tot}	typ.	9	mA
$V_P = 4,2$ V	I_{tot}	typ.	8	mA
Applicable supply voltage range of receiver	V_S		2,7 to 18	V*
Supply voltage range (pin 8)	V_P		3,6**to 5,4	V
Base bias voltage for f.m. front-end total external load current at pin 2: $-I_2 = 150\ \mu A$	$V_{2\text{-}16}$	typ.	1,2	V

A.C. CHARACTERISTICS

$T_{amb} = 25\ ^{o}C$; $V_P = 5,4$ V; I_E (TR9) = 1 mA; unless otherwise specified

			0,45	1	10,7	MHz
Input conductance at pin 2	g_{ie}	typ.	–	0,4	0,5	mA/V
Output conductance at pin 1	g_{oe}	typ.	6	–	90	μA/V
Input conductance at pin 15	g_{ie}	typ.	0,35	–	0,7	mA/V

---

* Adjustable by a dropping resistor in the V_S-line; see also maximum tolerated voltages for pins 1, 4, 7 and 8 in design data on the previous page.

** Minimum supply voltage for guaranteed oscillator operation: $V_P = 2,5$ V.

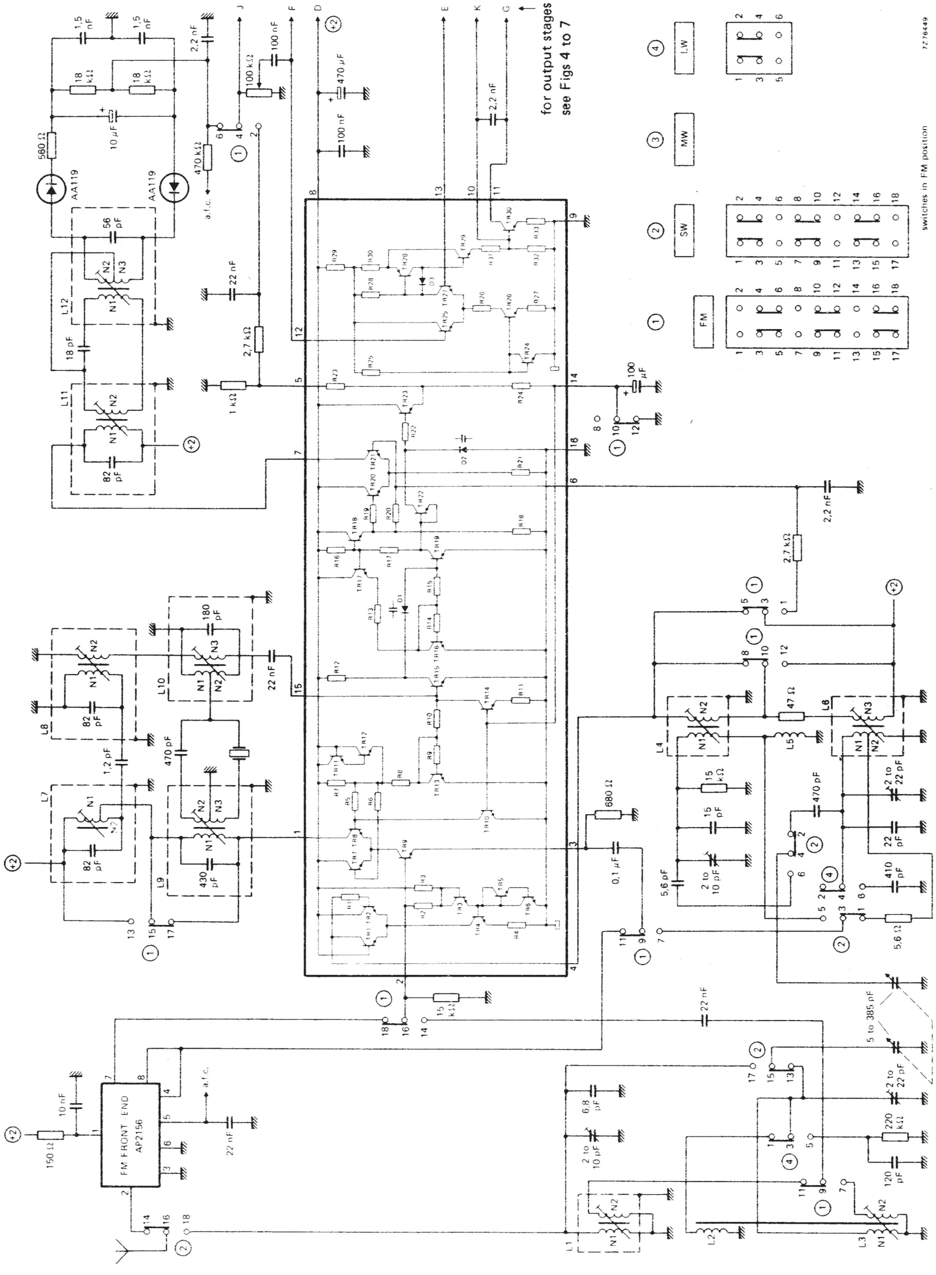

for output stages
see Figs 4 to 7
J
F
D
E
K
G
AA119
AA119
560 Ω
10 µF
18 kΩ
18 kΩ
1,5 nF
1,5 nF
2,2 nF
100 nF
100 kΩ
470 kΩ
a.f.c.
470 µF
100 nF
2,2 nF
56 pF
L12
L11
18 pF
82 pF
22 nF
2,7 kΩ
1 kΩ
100 µF
2,2 nF
2,7 kΩ
L8
L10
L7
L9
180 pF
22 nF
82 pF
1,2 pF
470 pF
82 pF
430 pF
680 Ω
0,1 µF
15 kΩ
22 nF
FM FRONT END
AP2156
150 Ω
10 nF
22 nF
a.f.c.
L4
L8
L5
47 Ω
15 kΩ
15 pF
2 to 10 pF
5,6 pF
470 pF
2 to 22 pF
22 pF
410 pF
5,6 Ω
5 to 385 pF
2 to 22 pF
6,8 pF
2 to 10 pF
220 kΩ
120 pF
L1
L2
L3
N1
N2
N3
FM
SW
MW
LW
switches in FM position
7Z76449

Fig. 3 H.F. part of a high performance f.m./a.m. (LW; MW; SW) receiver; for output stages see Figs 4, 5, 6 and 7.

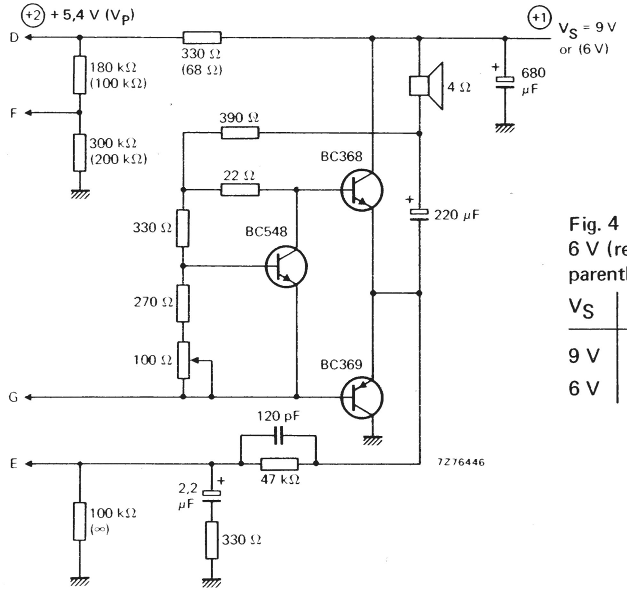

(+2) + 5,4 V (V$_P$)
D
F
G
E
180 kΩ
(100 kΩ)
300 kΩ
(200 kΩ)
330 Ω
(68 Ω)
390 Ω
22 Ω
330 Ω
270 Ω
100 Ω
BC548
BC368
BC369
(+1)
V$_S$ = 9 V
or (6 V)
4 Ω
680 μF
220 μF
120 pF
47 kΩ
2,2 μF
100 kΩ
(∞)
330 Ω
7Z76446

Fig. 4 Output stage for V_S = 9 V or 6 V (resistor values between parentheses); see also Fig. 3.

V_S	R_L	P_o at d_{tot} = 10%
9 V	4 Ω	1,8 W
6 V	4 Ω	0,6 W

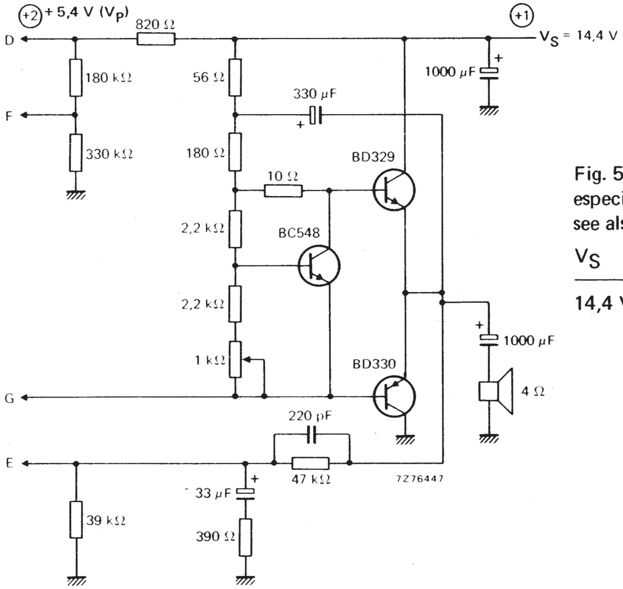

(+2) + 5,4 V (V$_P$)
820 Ω
D
F
G
E
180 kΩ
330 kΩ
56 Ω
180 Ω
10 Ω
2,2 kΩ
2,2 kΩ
1 kΩ
330 μF
BC548
BD329
BD330
(+1)
V$_S$ = 14,4 V
1000 μF
1000 μF
4 Ω
220 pF
47 kΩ
33 μF
390 Ω
39 kΩ
7Z76447

Fig. 5 Output stage for V_S = 14,4 V; especially used in car radios; see also Fig. 3.

V_S	R_L	P_o at d_{tot} = 10%
14,4 V	4 Ω	5,5 W

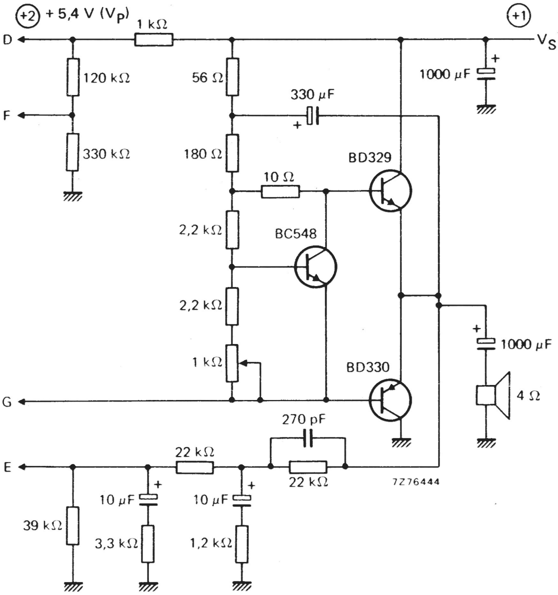

+2
+ 5,4 V (V_P)
1 kΩ
+1
V_S = 16 V
D
F
G
E
120 kΩ
330 kΩ
56 Ω
180 Ω
330 μF
1000 μF
BD329
10 Ω
2,2 kΩ
BC548
2,2 kΩ
1 kΩ
BD330
1000 μF
4 Ω
270 pF
22 kΩ
22 kΩ
10 μF
10 μF
39 kΩ
3,3 kΩ
1,2 kΩ
7Z76444

Fig. 6 Output stage for V_S = 16 V; see also Fig. 3.

V_S	R_L	P_o at d_{tot} = 10%
16 V	4 Ω	6,8 W

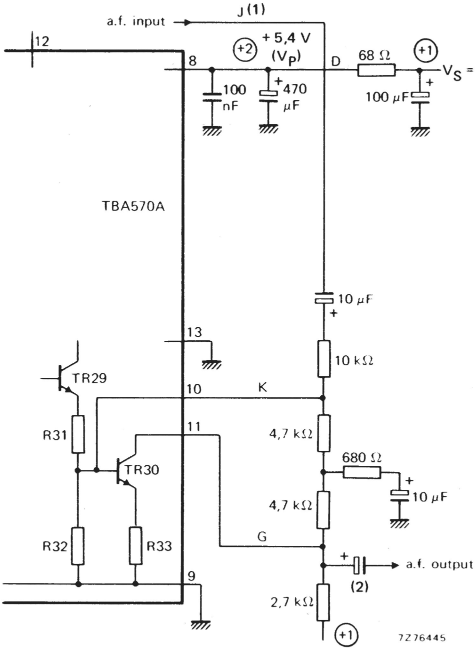

a.f. input
J (1)
12
8
+2
+ 5,4 V
(V_P)
D
68 Ω
+1
V_S = 6 V
100 nF
470 μF
100 μF
TBA570A
10 μF
13
10 kΩ
TR29
10
K
11
R31
4,7 kΩ
680 Ω
TR30
10 μF
4,7 kΩ
R32
R33
G
a.f. output
(2)
9
2,7 kΩ
+1
7Z76445

Fig. 7 Post amplifier for V_o = 500 mV and V_S = 6 V; see also Fig. 3.

(1) In circuit of Fig. 3 volume control resistance (100 kΩ) and capacitor (100 nF) on pin 12 should be omitted.

(2) Capacitor value depends on load.

COIL DATA (in circuit of Fig. 3)

High performance a.m./f.m. receiver (for portable and mains-fed applications)

A.M.—I.F. coils (f_o = 455 kHz)

I.F. bandpass filter:

L9
$N1 = 284{,}5\ \mu H$
$Q_o = 100$
$N1/N2 = 40$
$N2/N3 = 1$
$|Z_T| = 3\ k\Omega$

L10
$N1 = 680\ \mu H$
$Q_o = 100$
$N2/N1 = 74$
$(N2 + N1)/N3 = 10{,}7$

core material

L9, L10: 7 MN(C)
L7, L8, L11, L12: 119 AN(C)

F.M.—I.F. coils (f_o = 10,7 MHz)

Second i.f. bandpass filter:

L7
$N1 + N2 = 2{,}7\ \mu H$
$Q_o = 100$
$kQ_{L6\text{-}L7} = 1{,}2$
$N1/N2 = 1{,}75$

L8
$N1 = 2{,}7\ \mu H$
$Q_o = 90$
$N1/N2 = 5{,}5$

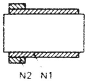
Ratio detector:

L11
$N1 = 2{,}7\ \mu H$
$Q_o = 85$
$kQ_{L11\text{-}L12} = 0{,}7$
$N1/N2 = 2{,}2$

L12
$N2 + N3 = 3{,}25\ \mu H$
$Q_o = 85$
$(N2 + N3)/N1 = 6$
$N2 = N3$

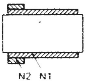
Low-cost 2-band a.m. portable receiver (see Fig. 8)

L1



N1 = 11
N2 = 2
wire: 1,1 mm dia.

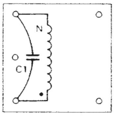
L2



N1 = 60
N2 = 4
wire: 20 x 0,03 mm

L1 and L2 on ferrite rod; 10 mm dia.; length = 10 cm

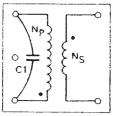
L3



$N = 284{,}5\ \mu H$; $f_m = 452$ kHz
$C1 = 430$ pF; $Q_o = 100$
wire: 0,1 mm dia.

core material: 7 MN(C)

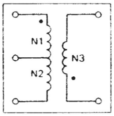
L4



$N_P = 284{,}5\ \mu H$; $f_m = 452$ kHz
$N_P/N_S = 16{,}7$; $Q_o = 100$
$C1 = 430$ pF
wire: 0,1 mm dia.

core material: 7 MN(C)

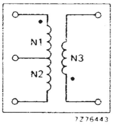
L5



$N1 + N2 = 127\ \mu H$; $f_m = 1$ MHz
$(N1 + N2)/N2 = 58$; $Q_o = 100$
$(N1 + N2)/N3 = 4{,}8$; $C_p = 200$ pF
wire: 0,1 mm dia.

core material: 7 BR

L6



$N1 + N2 = 13\ \mu H$; $f_m = 7$ MHz
$(N1 + N2)/N2 = 20$; $Q_o = 90$
$(N1 + N2)/N3 = 4$; $C_p = 40$ pF
wire: 0,1 mm dia.

core material: 119 AN(C)

Note

In the circuit of Fig. 8 for L3 and L4 a similar coil to L9 in the circuit of Fig. 3 can be used with the following exceptions:
L3: secondary windings N2 and N3 are not used.
L4: secondary windings N2 and N3 are connected in series.

When using a resistor between pins 2 and 15 (see dashed resistor in Fig. 8), signal handling is improved.

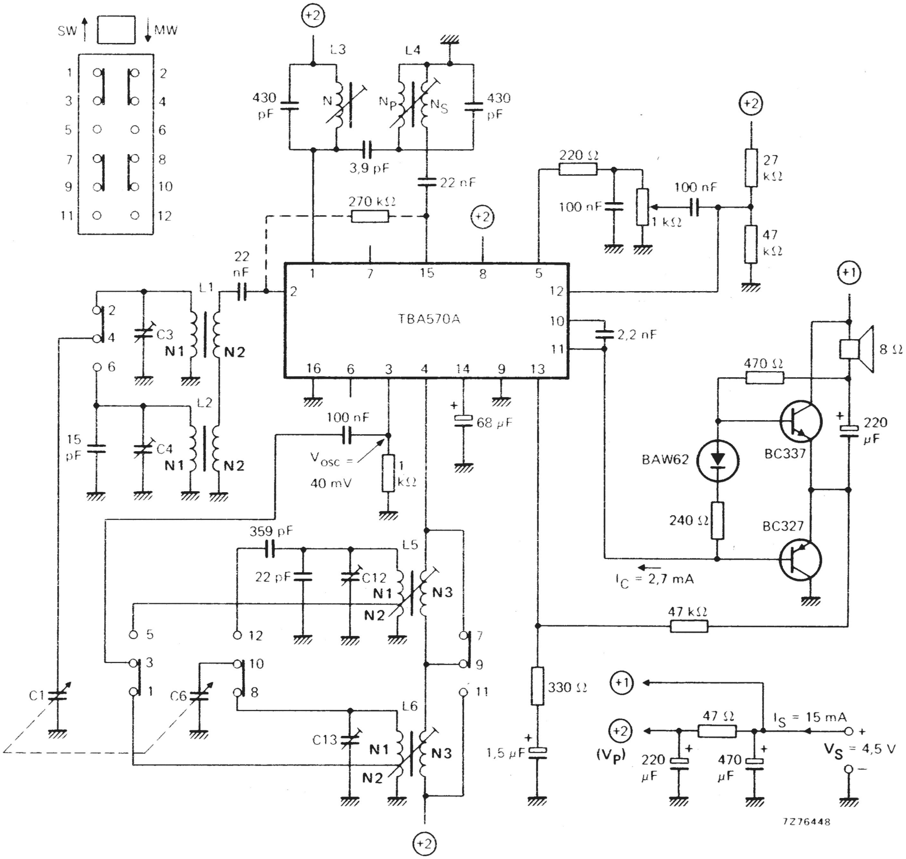

SW
MW
1 2
3 4
5 6
7 8
9 10
11 12
+2
L3
L4
430 pF
N
N_P
N_S
430 pF
3,9 pF
22 nF
270 kΩ
+2
220 Ω
100 nF
1 kΩ
100 nF
+2
27 kΩ
47 kΩ
22 nF
L1
TBA570A
1
7
15
8
5
2
12
10
11
16
6
3
4
14
9
13
2,2 nF
+1
8 Ω
470 Ω
C3
N1
N2
L2
15 pF
C4
N1
N2
100 nF
V_{osc} = 40 mV
1 kΩ
68 μF
220 μF
BAW62
BC337
240 Ω
BC327
I_C = 2,7 mA
359 pF
L5
22 pF
C12
N1
N2
N3
47 kΩ
5
12
7
3
10
9
1
8
11
C1
C6
L6
C13
N1
N2
N3
330 Ω
1,5 μF
+1
+2
(V_P)
47 Ω
I_S = 15 mA
V_S = 4,5 V
220 μF
470 μF
+2
7Z76448

Fig. 8 Low-cost 2-band (SW-MW) a.m. portable receiver; P_o = 250 mW; C1 and C6 maximum 385 pF.

APPLICATION INFORMATION

$T_{amb} = 25\ ^{o}C$

A.M. performance	$V_{8\text{-}16} = V_P$▲		5,4 V*	4,2 V**	
Sensitivity (V_o at pin 5; V_i at pin 2)					
$V_o = 30$ mV	V_i		3,0 to 12	–	μV
range 1	V_i		5,5 to 12	–	μV
range 2	V_i		3,0 to 7	–	μV
R.F. input voltage					
for S/N = 26 dB (notes 1 and 2)	V_i	typ.	18	10	μV
for $P_o = 50$ mW (adjustable); (notes 1,2 and 3)	V_i	typ.	2	2	μV
R.F. input voltage for 10 mV (a.f.) across volume control (notes 1 and 2)	V_i	typ.	2,7	4,5	μV
A.F. voltage across volume control at 100 μV (r.f.) input voltage (notes 1 and 2)	V_o	typ.	70	70	mV
Signal-to-noise ratio at 1 mV (r.f.) input voltage (notes 1 and 2)	S/N	typ.	46	47	dB
A.G.C. range (change in r.f. input voltage for 10 dB expansion in audio range); notes 1 and 2		typ.	60	60	dB
R.F. signal handling capability at 80% modulation; $d_{tot} < 10\%$ (note 1)	V_i	typ.	150	7	mV
Total harmonic distortion of h.f. part over most of a.g.c. range; m = 0,3; $f_m = 1$ kHz (note 4)	d_{tot}	typ.	1	1	%
I.F. selectivity	S_9	typ.	33	16	dB
I.F. bandwidth (3 dB)	B	typ.	5	5,5	kHz

Notes

1. a. A.F. signal: measured across volume control.
   b. R.F. signal: measured at pin 2 with the aerial circuit connected (source resistance about 1 kΩ).
   c. $f_o = 1$ MHz; $f_m = 400$ Hz.
2. m = 0,3.
3. A.M. sensitivity for $P_o = 50$ mW can be adjusted by means of the a.c. feedback network in the audio part e.g.: $V_i = 1,5$ μV for $P_o = 50$ mW (S/N ≈ 4 dB).
4. Distortion can be decreased to 0,7% by connecting a resistor of 270 kΩ between pins 2 and 15.

---

* See Figs 3, 4, 5, 6 and 7; high performance a.m./f.m. receiver.

** See Fig. 8; low-cost 2-band a.m. portable receiver.

▲ Minimum supply voltage for guaranteed oscillator operation: $V_P = 2,7$ V.

APPLICATION INFORMATION (continued)

T_{amb} = 25 °C; V_P = 5,4 V; measured in Fig. 3

F.M. performance

Sensitivity for an f.m. signal 3 dB before limiting			
at 75 Ω aerial input of f.m. front-end (note 1)	V_i	typ.	3,5 μV
at pin 2; first i.f. (notes 2 and 6)	V_i	typ.	50 μV
Sensitivity for 26 dB S/N ratio at 75 Ω aerial input of f.m. front-end (note 1)	V_i	typ.	2,5 μV
A.F. output voltage across volume control at an i.f. signal beyond limiting (note 2)	V_o	typ.	120 mV
Signal-to-noise ratio over most of signal range (note 2)	S/N	typ.	65 dB
A.M. suppression over most of signal range (note 3)		typ.	60 dB
I.F. selectivity (note 4)	S_{300}	typ.	43 dB
I.F. bandwidth (3 dB; note 4)	B	typ.	150 kHz
A.F. signal distortion 3 dB before i.f. limiting (note 5)	d_{tot}	typ.	0,8 %

Notes

1. Aerial e.m.f. (V_i) at f_o = 98 MHz; R_S = 50 Ω; Δf = ± 22,5 kHz; f_m = 1 kHz.
2. f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 1 kHz.
3. A.M. signal: m = 0,3; f_m = 1000 Hz.
   F.M. signal: f_o = 10,7 MHz; Δf = ± 75 kHz; f_m = 400 Hz.
   Carrier simultaneously modulated with a.m. and f.m.
4. Including ratio detector.
5. f_o = 98 MHz; Δf = ± 40 kHz; f_m = 1 kHz.
6. Pin 3 by-passed to ground with a capacitor of 220 nF.

APPLICATION INFORMATION (continued)

Audio performance

Distortion before clipping (note 1)	d_{tot}	typ.	0,5 %
Input impedance (note 2)	$\lvert Z_i \rvert$	typ.	90 kΩ
Noise output power; volume control at min. (note 3)	P_n	typ.	10 nW
Overall fidelity; flat within 3 dB (obtainable values)			35 Hz to 15 kHz
Open loop voltage gain	G_o	typ.	62 dB

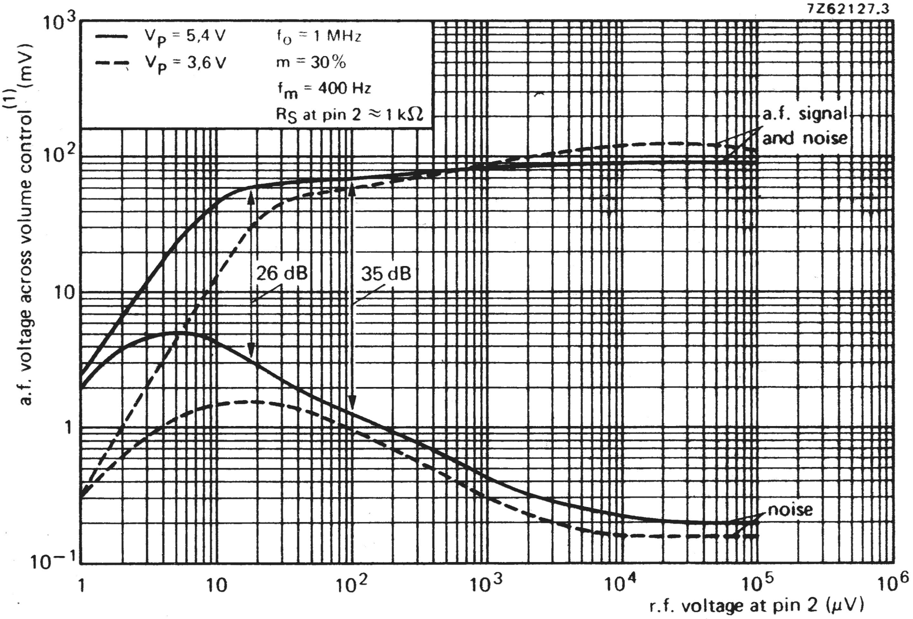
V_S	V	4,5	6	9	14,4	16
R_L	Ω	8	4	4	4	4
P_o at d_{tot} = 10%	W	0,22	0,6	1,8	5,5	6,8
P_o at onset of clipping; d_{tot} = 1%	W	0,15	0,4	1,2	4	4,8
V_i for d_{tot} = 10% (pin 12)	mV	14	16	25	50	45
V_i for P_o = 50 mW (pin 12)	mV	5,5	4,5	4	3,5	3,5
Output transistors		BC327 BC337	BC368 BC369	BC368 BC369	BD329 BD330	BD329 BD330
Circuit diagrams		Fig. 8	Fig. 4	Fig. 4	Fig. 5	Fig. 6

Post-amplifier (see Fig. 7)

Output voltage	500 mV
Audio gain (adjustable)	5
Distortion	0,2%

Notes

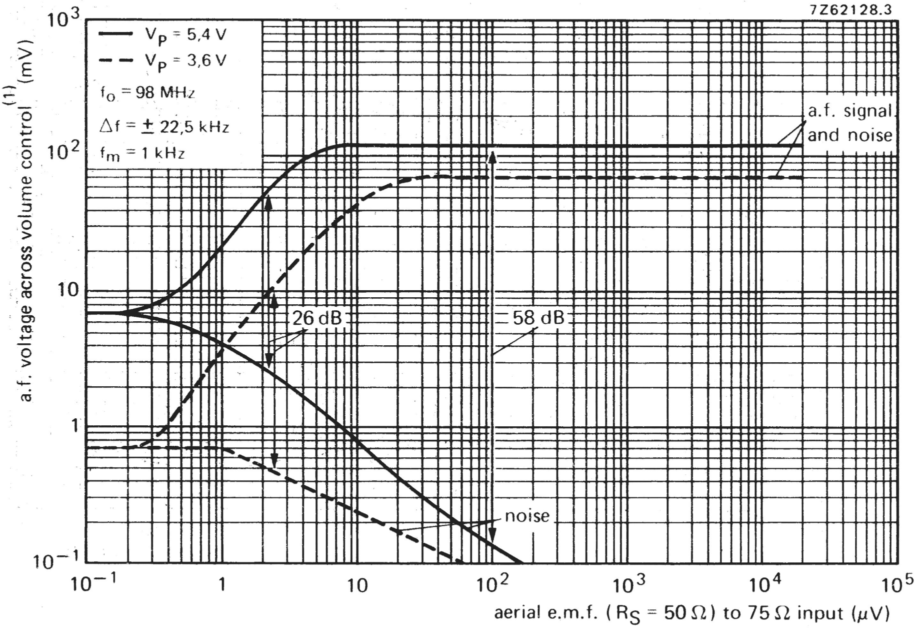
1. Measured at 1 kHz and a negative feedback of 16 dB.
2. At the maximum tolerated value of resistance-tap/bleeder at pin 12.
3. Measured at a bandwidth of 60 Hz to 15 kHz, pin 12 being connected via a capacitor of 32 μF to pin 9; R_L = 4 Ω.



(1) Slider at lower end.

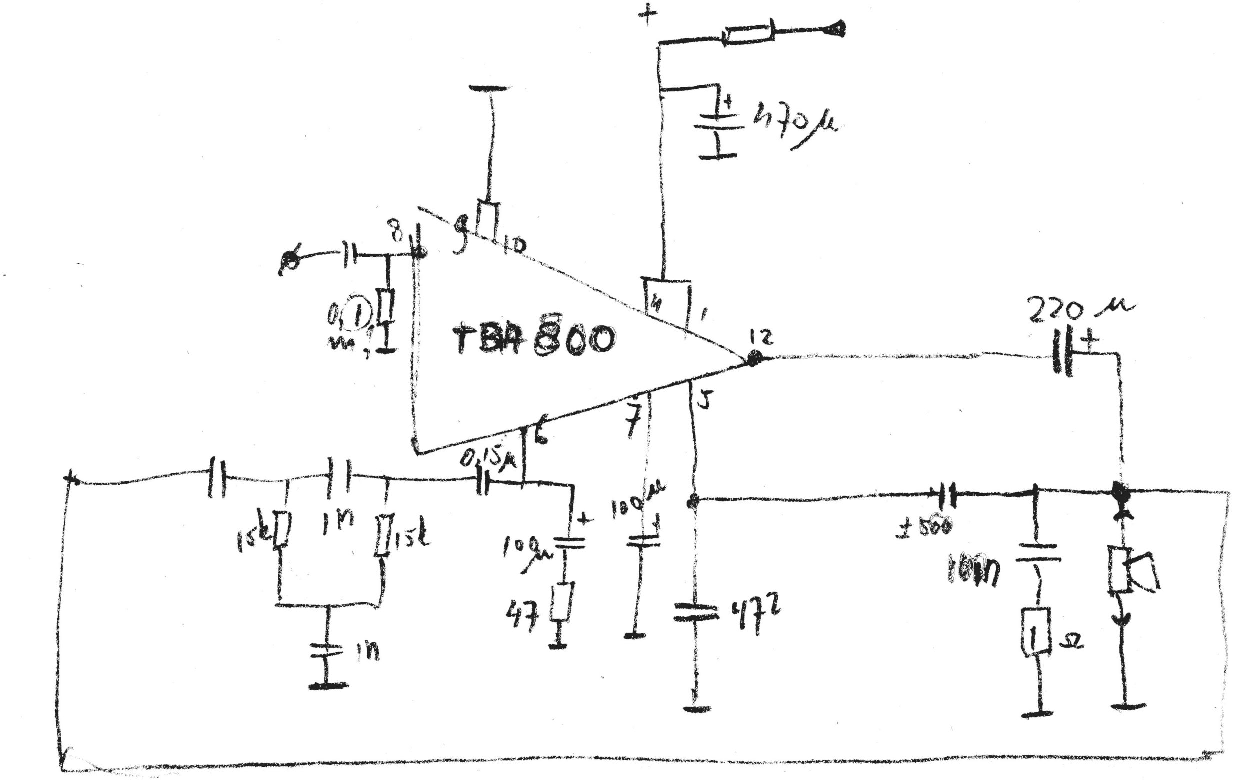
Fig. 9 Typical a.g.c. curves for a.m. reception (see Fig. 3); a.f. voltage across volume control as a function of r.f. voltage at pin 2.

APPLICATION INFORMATION (continued)



(1) Slider at lower end.

Fig. 10 Typical S/N curves for f.m. reception (see Fig. 3); a.f. voltage across volume control as a function of aerial e.m.f. from a source with R_S = 50 Ω to the 75 Ω input of the f.m. front-end.



+
470µ
TBA 800
8
9
10
4
1
12
5
7
6
0,1 M
220 µ
0,15µ
10µ
100µ
47
472
15k
1n
15k
1n
±500
100n
1 Ω

D.C. VOLUME AND BALANCE STEREO CONTROL CIRCUIT

The TCA730A is a monolithic integrated circuit for controlling volume and balance in stereo amplifiers by means of a d.c. voltage.
Features:

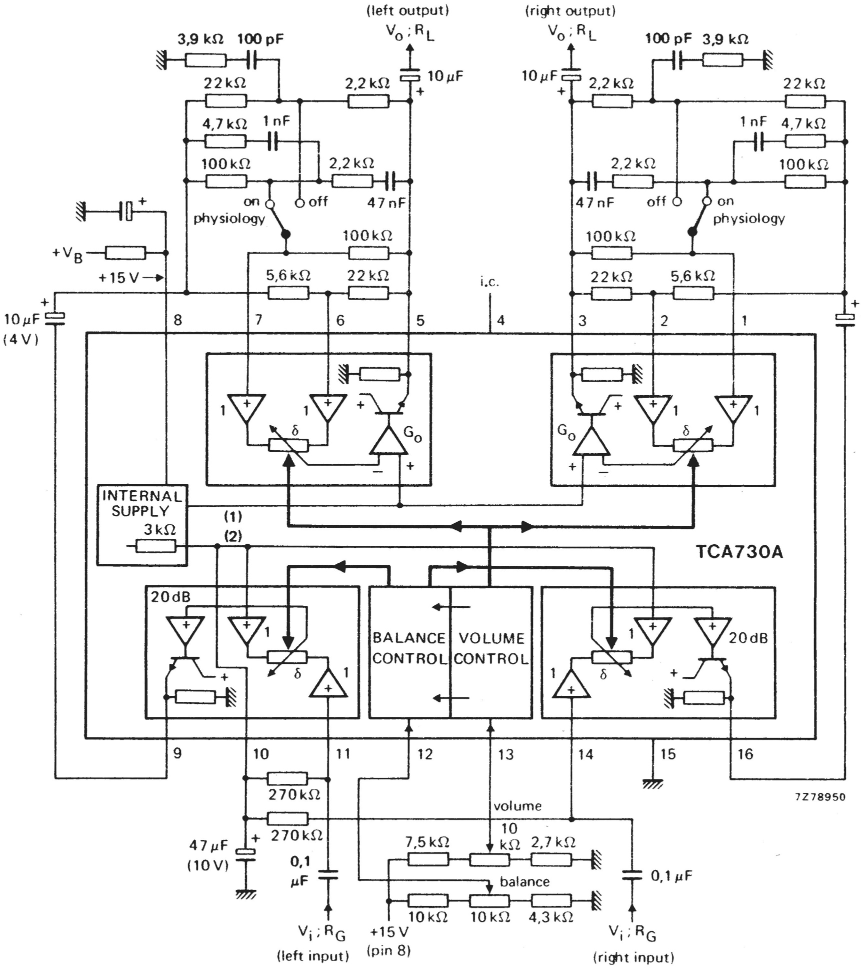
- physiological volume control
- balance control
- internal amplifier
- high-ohmic signals inputs
- internal supply voltage stabilization
- converter for the control voltage

QUICK REFERENCE DATA

Supply voltage (pin 8)	V_P	typ.	15	V
Supply current (pin 8)	I_P	typ.	35	mA
Input voltage range (r.m.s. value)	$V_{i(rms)}$		0,1 to 1,7	V
Nominal input voltage; m = 1 (r.m.s. value)	$V_{i(rms)}$	typ.	0,5	V
Input resistance	R_i	typ.	250	kΩ
Output voltage at nominal output power (r.m.s. value)	$V_{o(rms)}$	typ.	1	V
Volume control range	G_v		+20 to −80	dB
Channel balance	ΔG_v	typ.	1	dB
Balance control range	G_v		+5 to −7	dB
Total distortion at $V_{o(rms)}$ = 1 V	d_{tot}	typ.	0,1	%
Channel separation	α	typ.	55	dB
Signal-to-noise ratio	S/N	typ.	67	dB
Frequency response (−1 dB)			20 Hz to 20	kHz
Volume control voltage range	V_{13-15}		2 to 9,5	V
Balance control voltage range	V_{12-15}		2,5 to 9,0	V
Supply voltage range (pin 8)	V_P		13,5 to 16,5	V
Ambient temperature range	T_{amb}		−30 to +80	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).


(left output)
V_o ; R_L
(right output)
V_o ; R_L
3,9 kΩ
100 pF
22 kΩ
2,2 kΩ
10 μF
4,7 kΩ
1 nF
100 kΩ
2,2 kΩ
on
off
47 nF
physiology
100 kΩ
5,6 kΩ
22 kΩ
+V_B
+15 V
10 μF
(4 V)
i.c.
8
7
6
5
4
3
2
1
1
δ
G_o
INTERNAL SUPPLY
3 kΩ
(1)
(2)
TCA730A
20 dB
BALANCE CONTROL
VOLUME CONTROL
9
10
11
12
13
14
15
16
7Z78950
270 kΩ
270 kΩ
47 μF
(10 V)
0,1 μF
volume
7,5 kΩ
10 kΩ
2,7 kΩ
balance
10 kΩ
10 kΩ
4,3 kΩ
0,1 μF
V_i ; R_G
(left input)
+15 V
(pin 8)
V_i ; R_G
(right input)

(1) 6,6 V_{BE}; V_1 = 4,6 V
(2) 0,35 V_P + 0,65 V_{BE}; V_2 = 5,7 V.

Fig. 1 Block diagram with external circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	V_P	max.	18	V
Input voltages	$V_{11\text{-}15}; V_{14\text{-}15}$	min. max.	0 V_P	V V
Control voltages	$V_{12\text{-}15}; V_{13\text{-}15}$	min. max.	−5 12	V V
Total power dissipation	P_{tot}	max.	900	mW
Storage temperature range	T_{stg}		−55 to +150	°C
Operating ambient temperature range	T_{amb}		−30 to +80	°C

CHARACTERISTICS

$V_P = 15$ V; $T_{amb} = 25$ °C; measured in Fig. 1; balance control in mid-position ($V_{12\text{-}10} = 0$); physiology switch off; f = 1 kHz; $R_G = 22$ kΩ; $R_L = 5,6$ kΩ; unless otherwise specified.

Supply voltage range (pin 8)	V_P		13,5 to 16,5	V
Supply current	I_P	typ.	35 25 to 43	mA mA
Control range				
Voltage gain range	G_v		0 to 20	dB
Voltage gain at $V_{13\text{-}15} = 9,5$ V (0,63 V_P)	G_v	typ.	20 18 to 22	dB dB
Voltage attenuation range	G_v		0 to −80	dB
Voltage attenuation at $V_{13\text{-}15} = 3$ V (0,2 V_P)	G_v	> typ.	−75 −80	dB dB
Balance control range at $G_v = -10$ dB			+5 to −7	dB
Control inputs				
Recommended control voltage range				
volume	$V_{13\text{-}15}$		2 to 9,5	V
balance	$V_{12\text{-}15}$		2,5 to 9,0	V
Control voltage for $G_v = -10$ dB; $V_{12\text{-}10} = 0$	$V_{13\text{-}15}$		6,7 to 7,1	V*
Control voltage for balance 0 dB; $V_{13\text{-}15} = 6,9$ V	$V_{12\text{-}10}$	typ.	0 ± 0,2	V
Internal supply voltage (0,35 V_P + 0,65 V_{BE})	$V_{10\text{-}15}$	typ.	5,9 5,7 to 6,1	V V
Output resistance (pin 10)	R_{o10}	typ.	3	kΩ
Control current				
volume ($V_{13\text{-}15} = 6,9$ V)	I_{13}	typ. <	15 50	μA μA
balance ($V_{12\text{-}15} = 5,9$ V)	I_{12}	typ. <	8 25	μA μA
Input resistance				
pin 13 (volume)	R_{i13}	typ.	500	kΩ
pin 12 (balance)	R_{i12}	typ.	600	kΩ

* Typical value 6,9 V.

CHARACTERISTICS (continued)

Signal processing

Frequency response (−1 dB)	f		20 Hz to 20	kHz
Input resistance; $R_{11\text{-}10} = R_{14\text{-}10} = 270\ \text{k}\Omega$ (pins 11; 14)	$R_{i11;14}$	typ.	250	kΩ
Output resistance (pins 3; 5)	$R_{o3;5}$	typ.	10	Ω
Maximum input voltage; $V_{o(rms)} < 1$ V; $d_{tot} = 0{,}7$ % (r.m.s. value)	$V_{i(rms)}$	>	1,3	V
		typ.	1,7	V
Maximum output voltage; $V_{i(rms)} < 1$ V; $d_{tot} = 0{,}7$% (r.m.s. value)	$V_{o(rms)}$	>	1,8	V
		typ.	2,0	V
Nominal input voltage; m = 1 (r.m.s. value)	$V_{i(rms)}$	typ.	0,5	V
Nominal output voltage at nominal output power (r.m.s. value)	$V_{o(rms)}$	typ.	1	V
Total distortion				
$V_{o(rms)} = 1$ V; G_v = maximum	d_{tot}	typ.	0,07	%
		<	0,2	%
$V_{o(rms)} = 1$ V; $V_{i\ (rms)} = 1$ V	d_{tot}	typ.	0,2	%
$V_{o(rms)} = 50$ mV; $V_{i(rms)} = 150$ mV	d_{tot}	typ.	0,03	%
		<	0,1	%
$V_{o(rms)} = 50$ mV; $V_{i(rms)} = 1$ V	d_{tot}	typ.	0,2	%
Output noise voltage; f = 20 Hz to 20 kHz				
signal plus noise voltage (r.m.s. value)				
$G_v = -60$ dB	$V_{no(rms)}$	typ.	6	μV
$G_v = -10$ dB	$V_{no(rms)}$	typ.	15	μV
G_v = maximum (+20 dB)	$V_{no(rms)}$	typ.	100	μV
noise voltage; weighted conform DIN45405 (peak value)				
$G_v = -60$ dB	$V_{no(m)}$	typ.	15	μV
$G_v = -10$ dB	$V_{no(m)}$	typ.	35	μV
		<	80	μV
G_v = maximum (+20 dB)	$V_{no(m)}$	typ.	230	μV
		<	350	μV
Channel separation; $G_v = \pm 20$ dB; $V_i = V_o < 1$ V				
f = 250 Hz to 12,5 kHz	α	>	52	dB
		typ.	53	dB
f = 40 Hz to 16 kHz	α	>	46	dB
		typ.	50	dB
Channel balance				
$G_v = +15$ to -50 dB	ΔG_v	typ.	1	dB
		<	2	dB
$G_v < 50$ dB	ΔG_v	typ.	2	dB

Amplifier characteristics

Input resistance (pins 11 and 14)	$R_{i11;14}$	>	3	MΩ
D.C. output voltages				
(0,35 V_P – 1,35 V_{BE})	$V_{3\text{-}15}$; $V_{16\text{-}15}$	typ.	4,2	V
(6,6 V_{BE})	$V_{3\text{-}15}$; $V_{16\text{-}15}$	typ.	4,6	V
Quiescent input currents (pins 1,2,6,7,11,14)	I_1; I_2; I_6; I_7; I_{11}; I_{14}	typ. <	0,5 2	μA μA
Input resistance (pins 1,2,6 and 7) of physiology; without external circuitry	$R_{i1;2;6;7}$	>	1	MΩ
Internal load resistance at outputs (pins 3,5,9,16)	$R_{3\text{-}15}$; $R_{5\text{-}15}$; $R_{9\text{-}15}$; $R_{10\text{-}15}$	typ.	2	kΩ
Maximum gain; no load	$G_{3\text{-}1}$; $G_{3\text{-}2}$; $G_{5\text{-}6}$; $G_{5\text{-}7}$	> typ.	40 43	dB dB

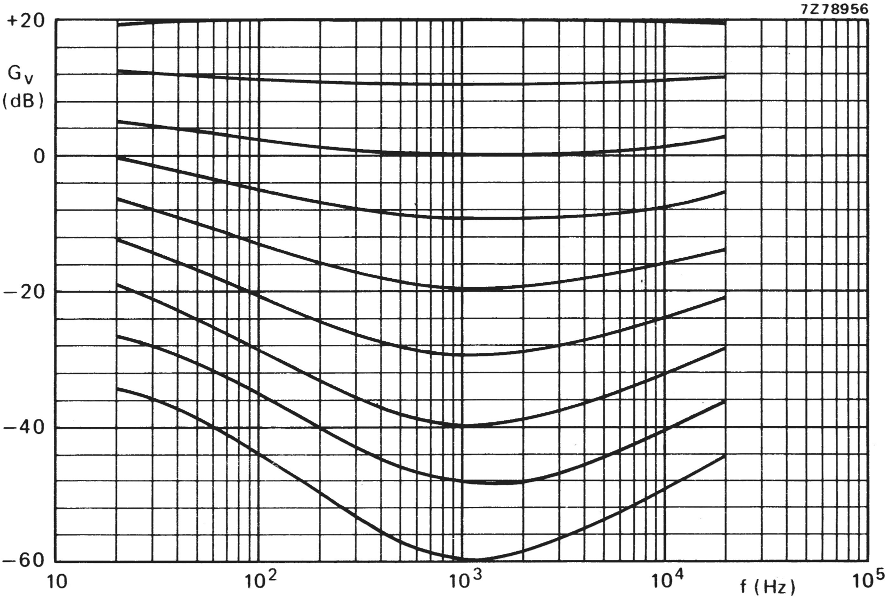


Fig. 2 Frequency response volume control with physiology.

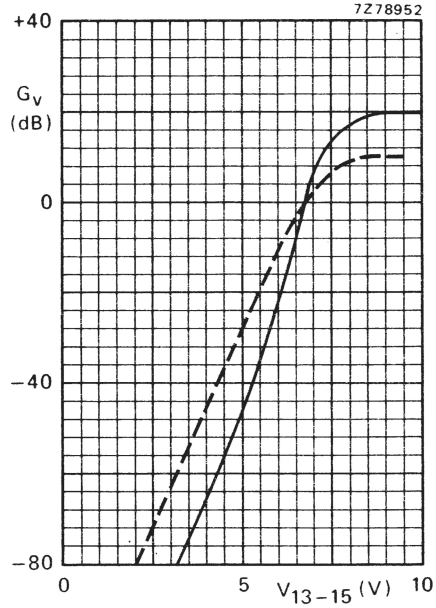
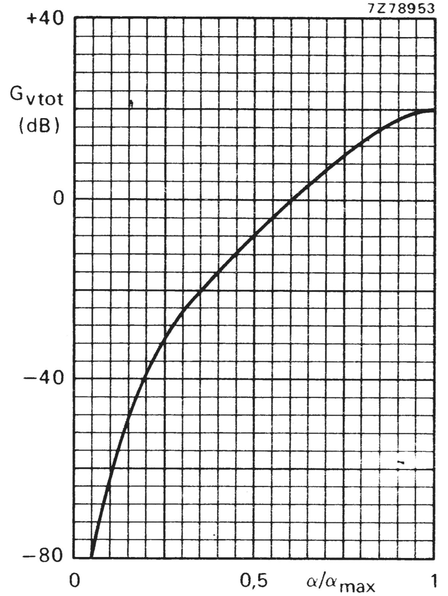


Fig. 3 Volume control curves; without physiology; balance = 0; $V_{12\text{-}10} = 0$.

—— $G_{v\,tot}$; $G_{v\,5\text{-}11}$; $G_{v\,3\text{-}14}$

- - - $G_{v\,9\text{-}11}$; $G_{v\,16\text{-}14}$



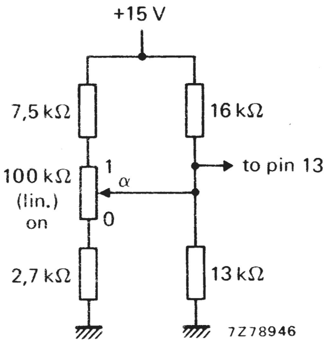

+15 V
7,5 kΩ
16 kΩ
100 kΩ
(lin.)
on
1
α
0
to pin 13
2,7 kΩ
13 kΩ
7Z78946

Fig. 4 Volume adjustment curve; balance = 0; $V_{12\text{-}10} = 0$.

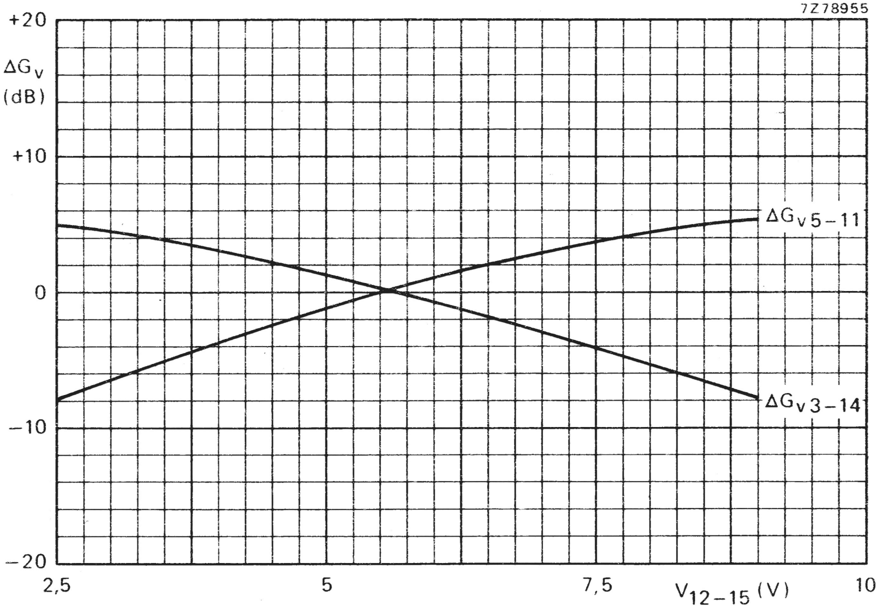


Fig. 5 Balance control curves; $G_{v\,tot} = -10$ dB ($V_{13\text{-}15} = 6,9$ V); for balance = 0.

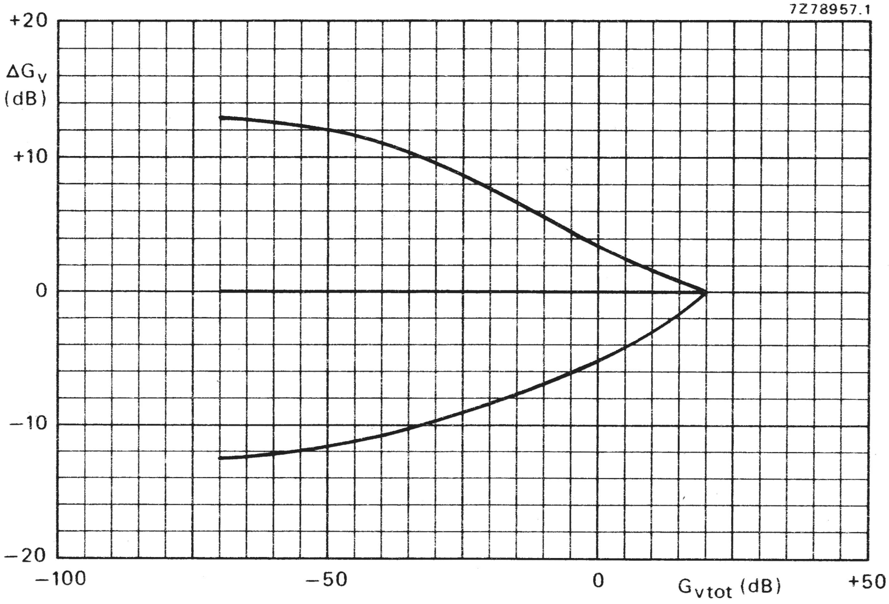
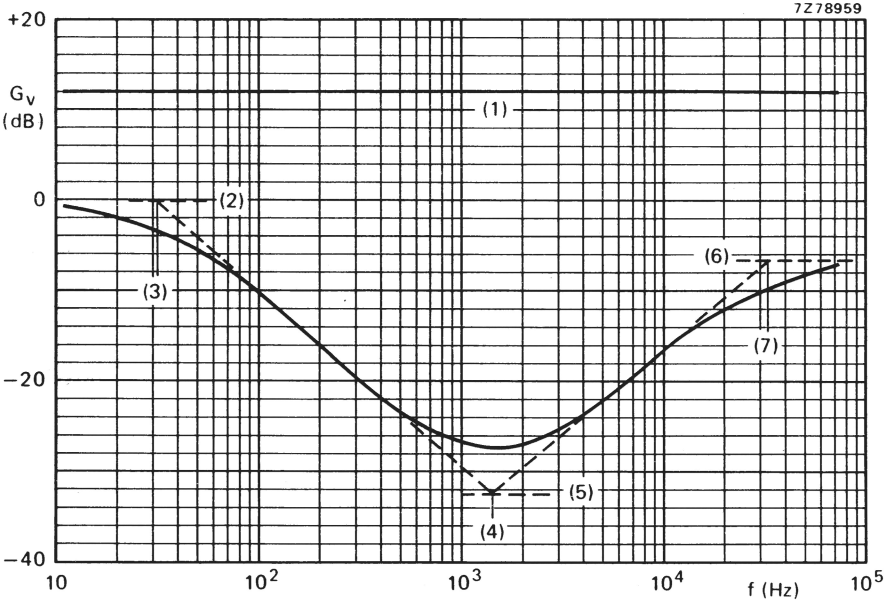


Fig. 6 Balance control range; $V_{12\text{-}15} = 2,5$ to $9,0$ V.



(1) $G_v = R2/R1$
(2) $G_v = R42/R31$
(3) $G_v = 1/2\pi \cdot R42 \cdot C42$
(4) $G_v = 1/2\pi \cdot R41 \cdot C31 = 1/2\pi \cdot R31 \cdot C31$
(5) $G_v \approx R41/R32$
(6) $G_v \approx R41/R32$
(7) $G_v = 1/2\pi \cdot R32 \cdot C31$

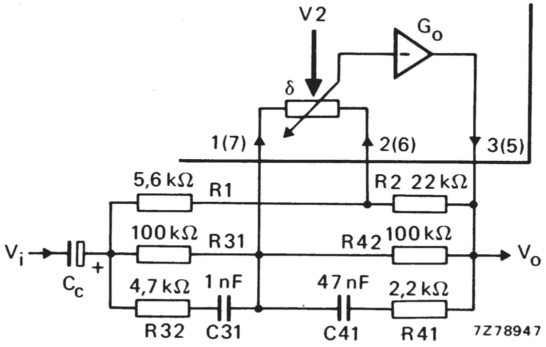

V2
G_o
δ
1(7)
2(6)
3(5)
5,6 kΩ
R1
R2 22 kΩ
100 kΩ
R31
R42
100 kΩ
V_i
+
C_c
V_o
4,7 kΩ
1 nF
47 nF
2,2 kΩ
R32
C31
C41
R41
7Z78947

Fig. 7 Frequency response of the physiology part.

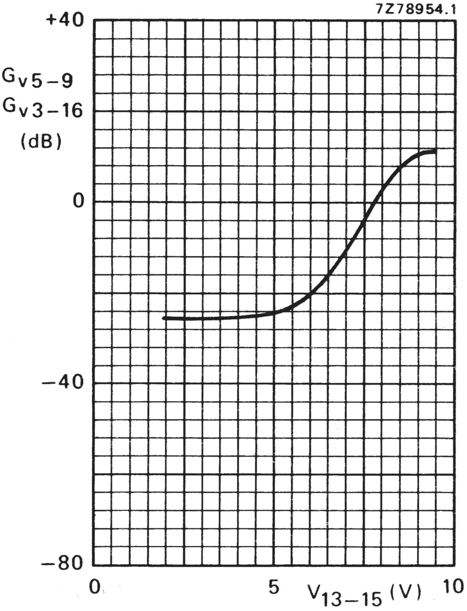


Fig. 8 Physiology control curve; f = 1 kHz; balance = 0; $V_{12\text{-}15} = 0$.

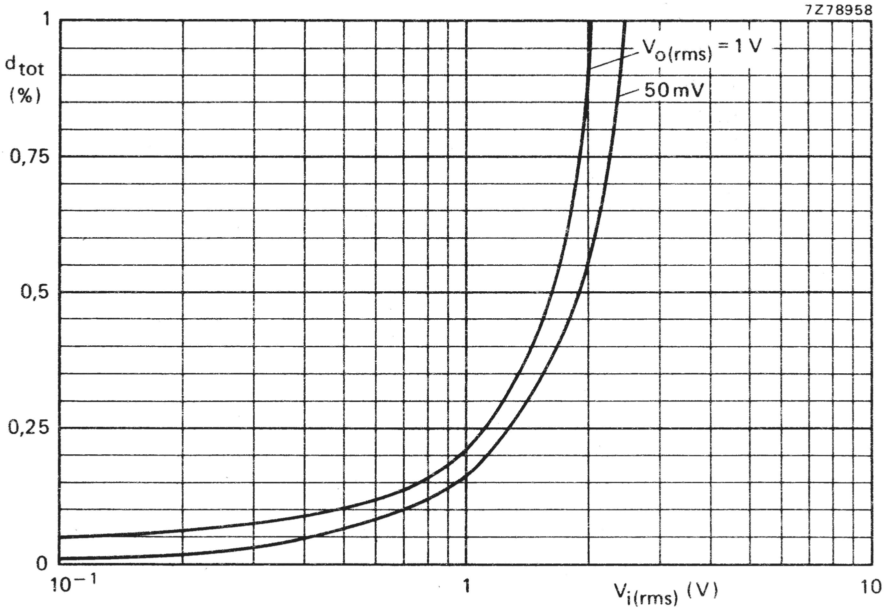


Fig. 9 Total distortion as a function of r.m.s. input voltage; f = 1 kHz; R_L = 5,6 kΩ.

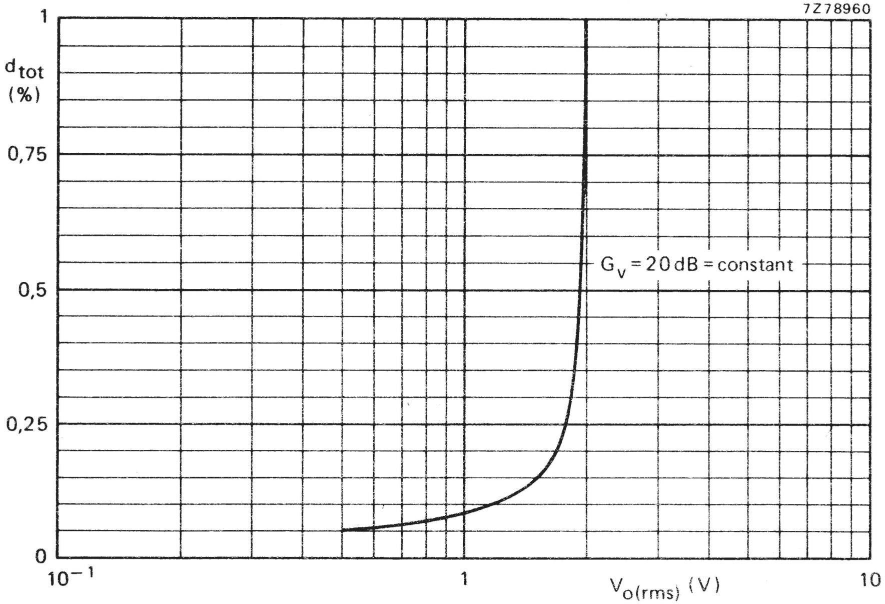


Fig. 10 Total distortion as a function of r.m.s. output voltage; f = 1 kHz; R_L = 5,6 kΩ.

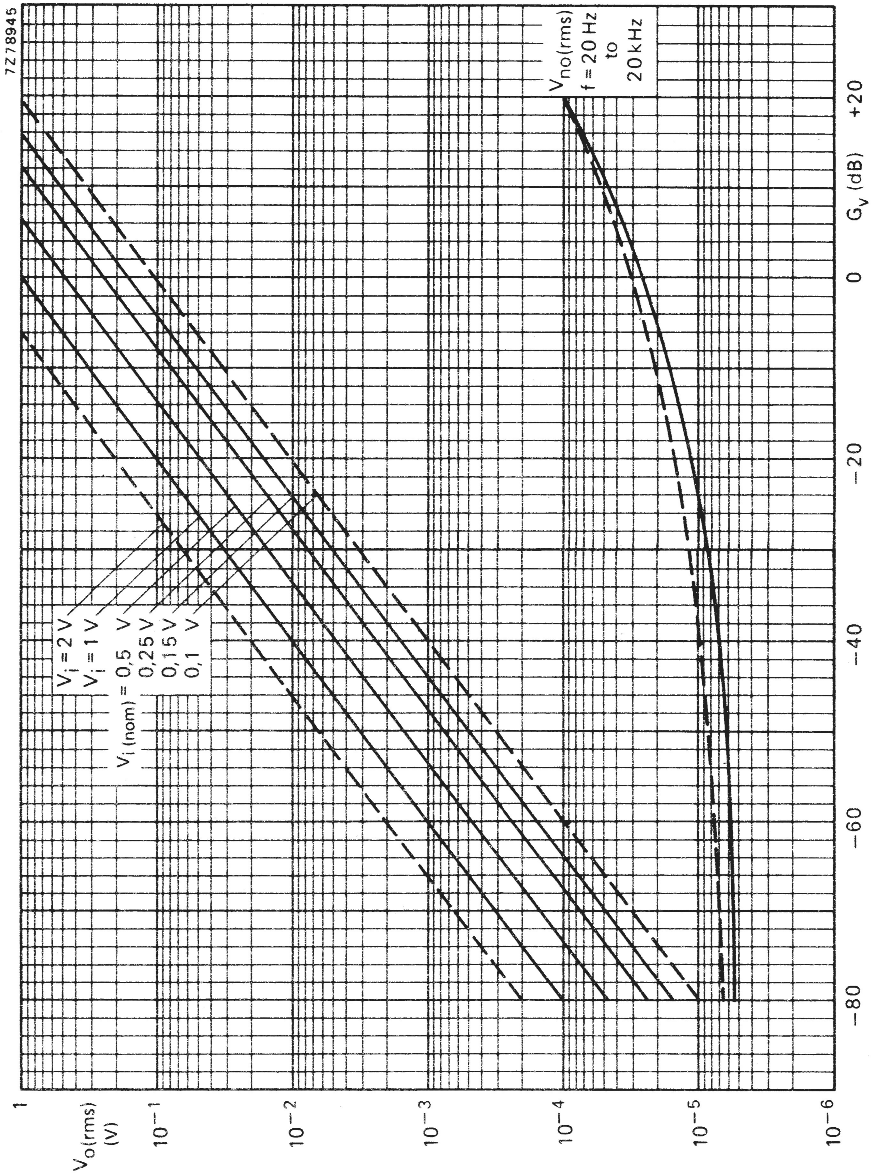
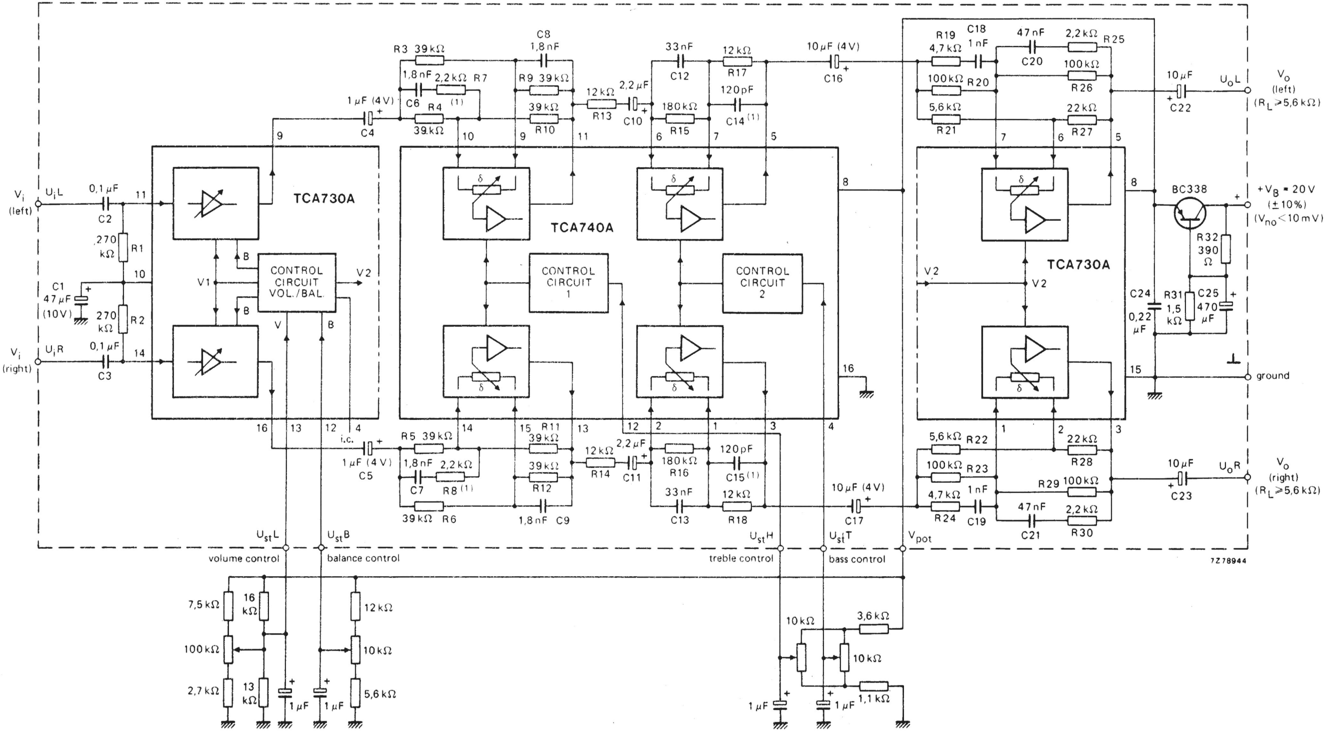


Fig. 11 The r.m.s. output voltage as a function of voltage gain; $P_{o(nom)}$ relative to $V_{o(rms)} = 1$ V.
—— without physiological volume control; ---- with physiological volume control.

APPLICATION INFORMATION


TCA730A
TCA740A
TCA730A
CONTROL CIRCUIT VOL./BAL.
CONTROL CIRCUIT 1
CONTROL CIRCUIT 2
V1
V2
B
V
V_i (left)
V_i (right)
U_iL
U_iR
C1 47 μF (10V)
C2 0,1 μF
C3 0,1 μF
R1 270 kΩ
R2 270 kΩ
C4 1 μF (4V)
C5 1 μF (4V)
i.c.
R3 39 kΩ
R4 39 kΩ
R5 39 kΩ
R6 39 kΩ
C6 1,8 nF
C7 1,8 nF
R7 2,2 kΩ (1)
R8 2,2 kΩ (1)
C8 1,8 nF
C9 1,8 nF
R9 39 kΩ
R10 39 kΩ
R11 39 kΩ
R12 39 kΩ
R13 12 kΩ
R14 12 kΩ
C10 2,2 μF
C11 2,2 μF
C12 33 nF
C13 33 nF
R15 180 kΩ
R16 180 kΩ
R17 12 kΩ
R18 12 kΩ
C14 120 pF (1)
C15 120 pF (1)
C16 10 μF (4V)
C17 10 μF (4V)
R19 4,7 kΩ
R24 4,7 kΩ
C18 1 nF
C19 1 nF
R20 100 kΩ
R23 100 kΩ
R21 5,6 kΩ
R22 5,6 kΩ
C20 47 nF
C21 47 nF
R25 2,2 kΩ
R30 2,2 kΩ
R26 100 kΩ
R29 100 kΩ
R27 22 kΩ
R28 22 kΩ
C22 10 μF
C23 10 μF
U_oL
U_oR
V_o (left) ($R_L \geqslant 5{,}6$ kΩ)
V_o (right) ($R_L \geqslant 5{,}6$ kΩ)
BC338
R32 390 Ω
R31 1,5 kΩ
C25 470 μF
C24 0,22 μF
$+V_B = 20$ V (± 10%) ($V_{no} < 10$ mV)
ground
$U_{st}L$
$U_{st}B$
$U_{st}H$
$U_{st}T$
V_{pot}
volume control
balance control
treble control
bass control
7,5 kΩ
16 kΩ
100 kΩ
2,7 kΩ
13 kΩ
1 μF
12 kΩ
10 kΩ
5,6 kΩ
3,6 kΩ
1,1 kΩ
7Z78944

(1) RC network for limiting treble boost (linear: $f_{-3\,dB} = 100$ kHz).

Fig. 12 Application diagram for TCA730A and TCA740A. For printed-circuit board see Fig. 13.

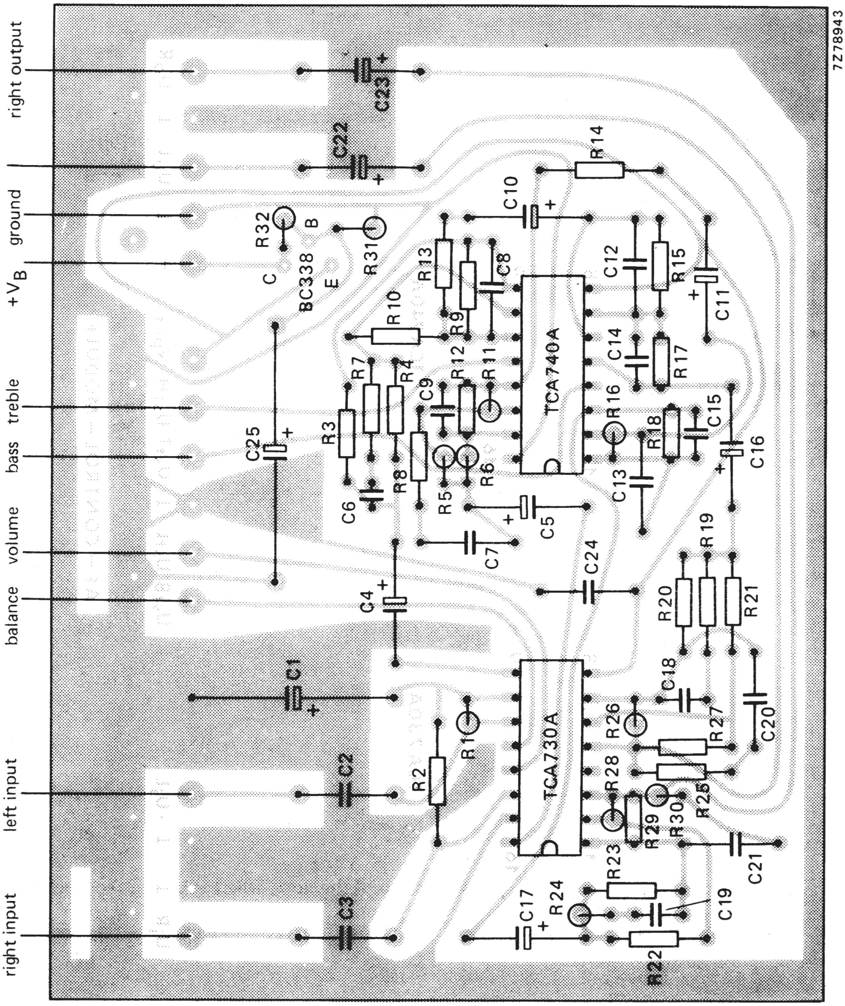
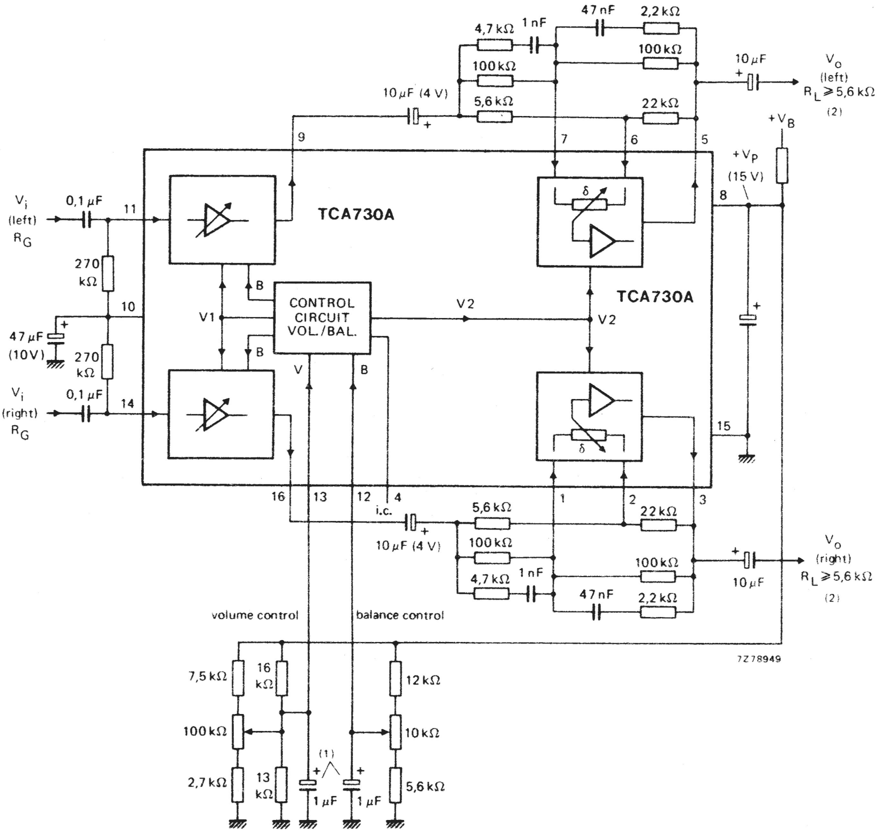

right output
left output
ground
+V_B
treble
bass
volume
balance
left input
right input
7Z78943
BC338
C
B
E
TCA740A
TCA730A
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32

Fig. 13 Printed-circuit board component side, showing component layout; for circuit diagram see Fig. 12.

APPLICATION INFORMATION (continued)



TCA730A
V1
V2
CONTROL CIRCUIT VOL./BAL.
V
B
Vi (left) RG
Vi (right) RG
0,1 µF
270 kΩ
47 µF (10V)
10 µF (4 V)
4,7 kΩ
1 nF
47 nF
2,2 kΩ
100 kΩ
5,6 kΩ
22 kΩ
10 µF
Vo (left) RL ≥ 5,6 kΩ (2)
Vo (right) RL ≥ 5,6 kΩ (2)
+VB
+VP (15 V)
δ
i.c.
volume control
balance control
7,5 kΩ
16 kΩ
13 kΩ
2,7 kΩ
12 kΩ
10 kΩ
1 µF
(1)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
7Z78949

(1) $C_{13\text{-}15} = C_{12\text{-}15} = 1\ \mu F$ are intended for suppression of the noise when adjusting the mechanical potentiometers.

(2) For rejecting noise, caused by switching on or off, corresponding muting switches can be used before or in the output power stage.

Fig. 14 Application example of TCA730A used for volume and balance control.

D.C. TREBLE AND BASS STEREO CONTROL CIRCUIT

The TCA740A is a monolithic integrated circuit for controlling treble and bass in stereo amplifiers by means of a d.c. voltage.
Features:

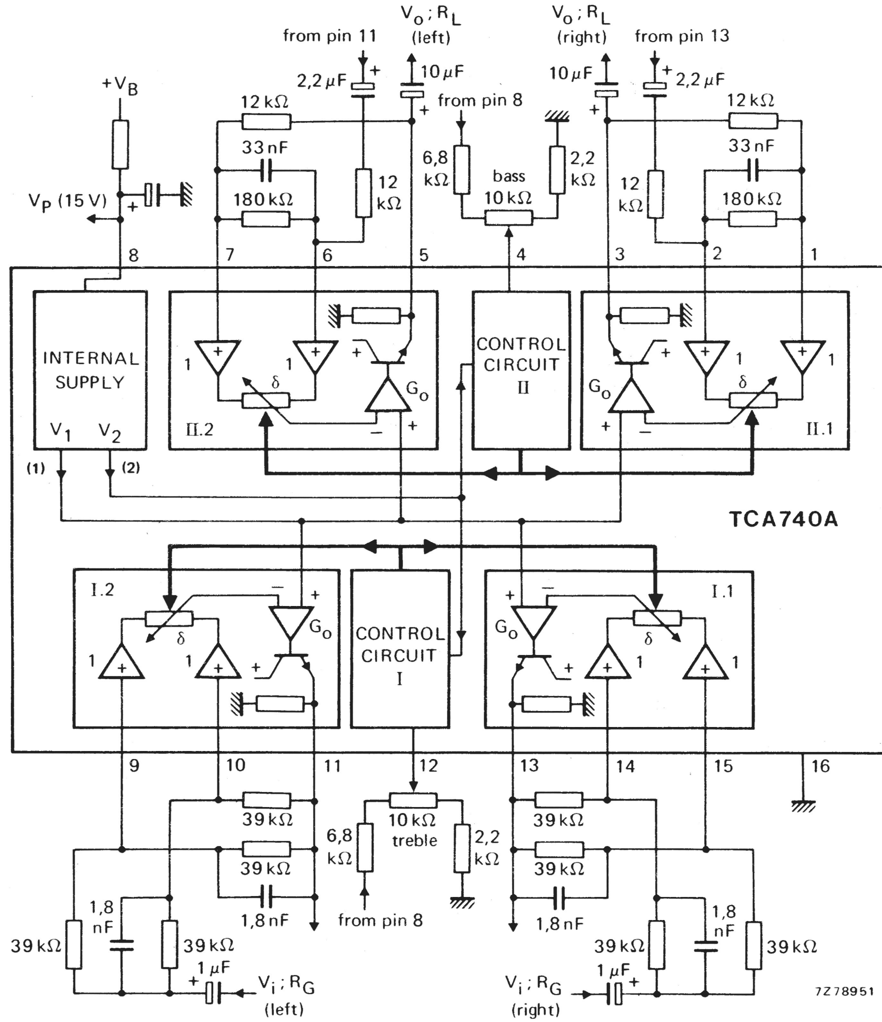
- two double potentiometer circuits
- feedback control
- internal amplifier
- high-ohmic signal inputs
- converter for the control voltages
- low-ohmic and short-circuit protected signal outputs

QUICK REFERENCE DATA

Supply voltage (pin 8)	V_P	typ.	15	V
Supply current (pin 8)	I_P	typ.	35	mA
Bass boost and cut at 40 Hz (ref. 1 kHz)		typ.	± 16	dB
Treble boost and cut at 16 kHz (ref. 1 kHz)		typ.	± 16	dB
Input/output voltage at d_{tot} = 0,7% (r.m.s. value)	$V_{i,o(rms)}$	typ.	2	V
Total distortion at $V_{o(rms)}$ = 1 V; linear frequency response	d_{tot}	typ.	0,1	%
Channel separation	α	typ.	70	dB
Output signal plus noise voltage (r.m.s. value)	$V_{no(rms)}$	typ.	45	μV
Frequency response (−1 dB)	f		20 Hz to 20	kHz
Treble/bass control voltage range	$V_{12\text{-}16}$; $V_{4\text{-}16}$		1,8 to 9,5	V
Supply voltage range (pin 8)	V_P		13,5 to 16,5	V
Ambient temperature range	T_{amb}		−30 to + 80	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).



V_o ; R_L (left)
V_o ; R_L (right)
from pin 11
from pin 13
from pin 8
$+V_B$
V_P (15 V)
2,2 μF
10 μF
12 kΩ
33 nF
180 kΩ
12 kΩ
6,8 kΩ
2,2 kΩ
bass 10 kΩ
1 2 3 4 5 6 7 8
INTERNAL SUPPLY
V_1
V_2
(1)
(2)
II.2
II.1
CONTROL CIRCUIT II
CONTROL CIRCUIT I
G_o
δ
TCA740A
I.2
I.1
9 10 11 12 13 14 15 16
39 kΩ
1,8 nF
10 kΩ treble
1 μF
V_i ; R_G (left)
V_i ; R_G (right)
7Z78951

(1) 6,6 V_{BE}; $V_1 = 4{,}6$ V

(2) 0,31 $V_P + 1{,}4\,V_{BE}$; $V_2 = 5{,}6$ V

Fig. 1 Block diagram with external circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	V_P	max.	18	V
Control voltages (pins 4 and 12)	$V_{4\text{-}16}$	max.	12	V
	$-V_{4\text{-}16}$	max.	5	V
	$V_{12\text{-}16}$	max.	12	V
	$-V_{12\text{-}16}$	max.	5	V
Total power dissipation	P_{tot}	max.	900	mW
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

V_P = 15 V; T_{amb} = 25 °C; measured in Fig. 1; in position 'linear' ($V_{4\text{-}16} = V_{12\text{-}16}$ = 5,6 V); R_G = 60 Ω; R_L = 5,6 kΩ; f = 1 kHz; unless otherwise specified

Supply voltage range (pin 8)	V_P		13,5 to 16,5	V
Supply current (pin 8)	I_P	typ.	34	mA
			25 to 45	mA

Signal processing

Voltage gain at linear frequency response	G_v	typ.	0	dB
Frequency response (−1 dB)	f		20 Hz to 20	kHz
Maximum gain variation at f = 1 kHz at maximum bass/treble boost or cut	ΔG_v	<	± 1,5	dB
Bass boost at 40 Hz (ref. 1 kHz) $V_{4\text{-}16}$ = 9,2 V		>	15	dB
		typ.	16	dB
Bass cut at 40 Hz (ref. 1 kHz) $V_{4\text{-}16}$ = 2 V		>	15	dB
		typ.	16	dB
Treble boost at 16 kHz (ref. 1 kHz) $V_{12\text{-}16}$ = 9,2 V		>	15	dB
		typ.	16	dB
Treble cut at 16 kHz (ref. 1 kHz) $V_{12\text{-}16}$ = 2 V		>	15	dB
		typ.	16	dB
Total distortion				
$V_{o(rms)}$ = 100 mV; f = 1 kHz	d_{tot}	typ.	0,03	%
$V_{o(rms)}$ = 100 mV; f = 40 Hz to 16 kHz	d_{tot}	typ.	0,1	%
$V_{o(rms)}$ = 1 V; f = 1 kHz	d_{tot}	typ.	0,07	%
		<	0,2	%
$V_{o(rms)}$ = 1 V; f = 40 Hz to 16 kHz	d_{tot}	typ.	0,2	%
Input/output voltage at d_{tot} = 0,7 % (r.m.s. value)	$V_{i(rms)} = V_{o(rms)}$	>	1,6	V
		typ.	2	V
Output signal plus noise voltage (r.m.s. value) f = 20 Hz to 20 kHz	$V_{no(rms)}$	typ.	40	μV
Output noise voltage; weighted conform DIN45405; peak value	$V_{no(m)}$	typ.	90	μV
		<	160	μV

CHARACTERISTICS (continued)

Channel separation				
f = 1 kHz	α	typ.	72	dB
f = 250 Hz to 12,5 kHz	α	typ.	68	dB
f = 40 Hz to 16 kHz	α	>	50	dB
		typ.	58	dB

Control voltages

Recommended control voltage range treble/bass	$V_{4\text{-}16} = V_{12\text{-}16}$	>	0	V
			2 to 9,2	V
		<	0,66 V_P	V
Control voltage at linear frequency response	$V_{4\text{-}16} = V_{12\text{-}16}$	typ.	5,6	V
			5,4 to 5,8	V
			(0,31 V_P to 1,4 V_{BE})	V
Quiescent input current $V_{4\text{-}16} = V_{12\text{-}16} = 2$ to 9,2 V	$I_4 = I_{12}$	typ.	6	µA
		<	25	µA
Input resistance (pins 4 and 12) $V_{4\text{-}16} = V_{12\text{-}16} = 5{,}6$ V	$R_{i4;12}$	typ.	800	kΩ

Amplifier characteristics

Quiescent input currents; $V_i = 4{,}6$ V (pins 1, 2, 6, 7, 9, 10, 14 and 15)	$I_1;I_2;I_6;I_7;I_9;I_{10};I_{14};I_{15}$	typ.	0,6	µA
		<	2	µA
Input resistance (pins 1,2,6,7,9,10,14 and 15)	$R_{i\,1;2;6;7;9;10;14;15}$	>	1	MΩ
Internal emitter resistance at outputs	$R_{3\text{-}16}$; $R_{5\text{-}16}$; $R_{11\text{-}16}$; $R_{13\text{-}16}$	typ.	2	kΩ
Output resistance (pins 3,5,11 and 13)	$R_{o\,3;5;11;13\text{-}16}$	typ.	10	Ω
Maximum gain; no load	G_v	>	40	dB
		typ.	43	dB
D.C. output voltages $V_{4\text{-}16} = V_{12\text{-}16} = 5{,}6$ V (pins 3,5,11 and 13)	$V_{3\text{-}16}$; $V_{5\text{-}16}$; $V_{11\text{-}16}$; $V_{13\text{-}16}$	typ.	4,6	V
			4,3 to 4,9	V
			(6,6 V_{BE})	V

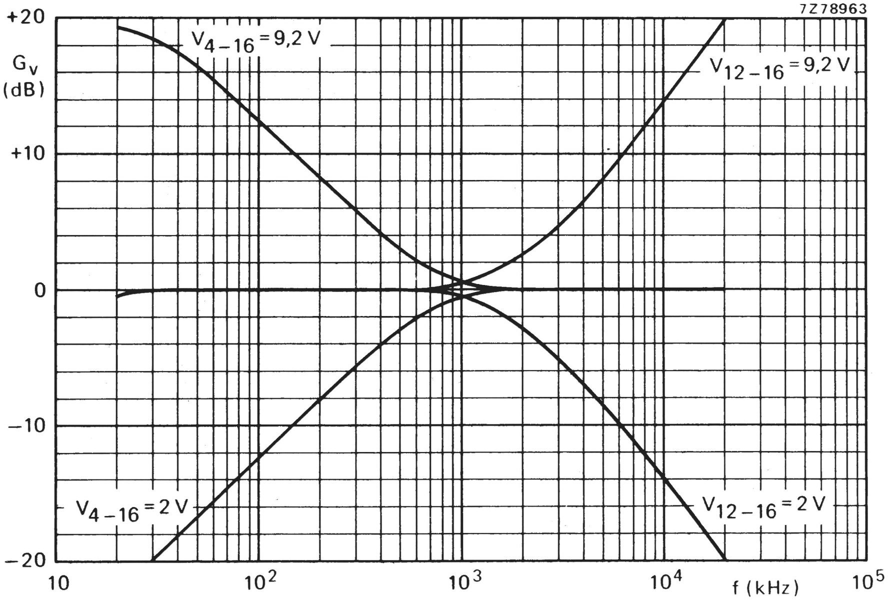


Fig. 2 Frequency response.

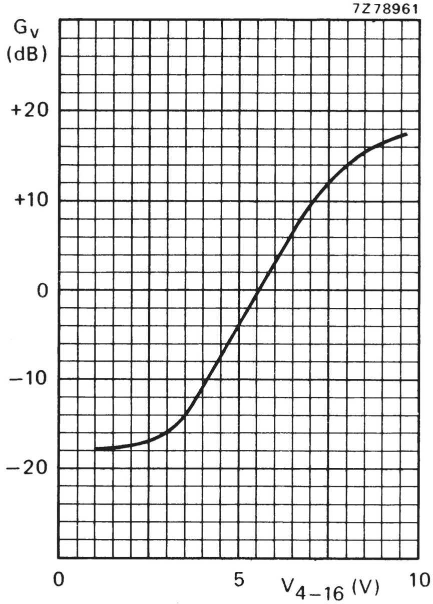


Fig. 3 Bass control curve at f = 40 Hz.

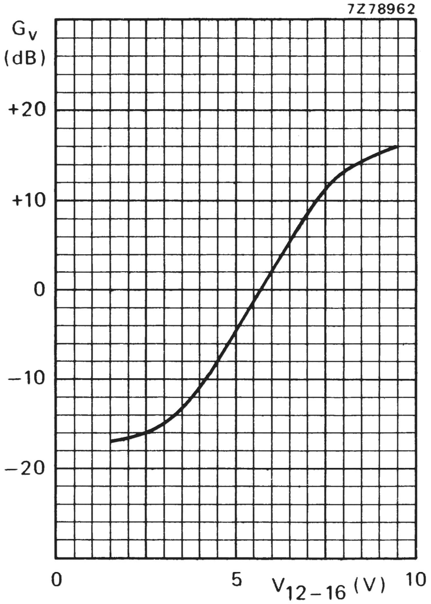


Fig. 4 Treble control curve at f = 16 kHz.

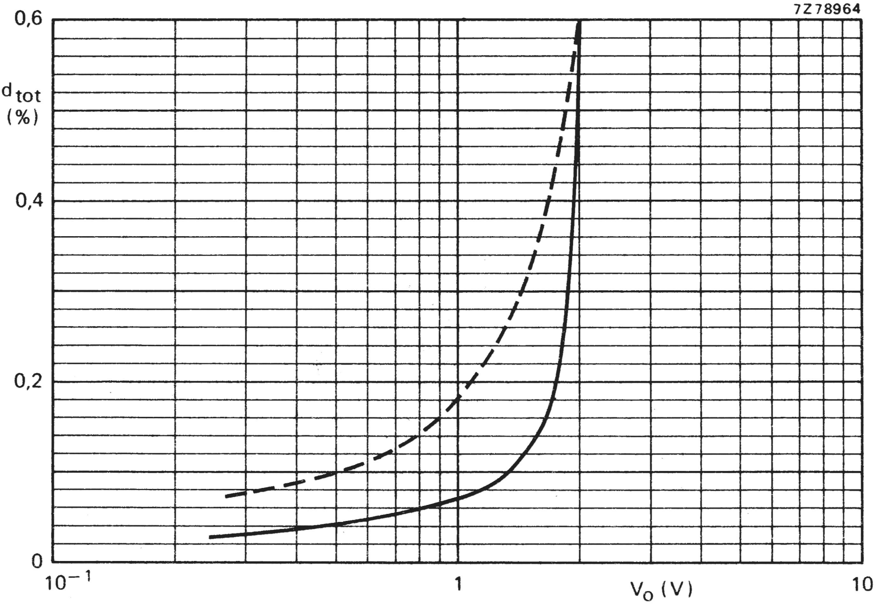
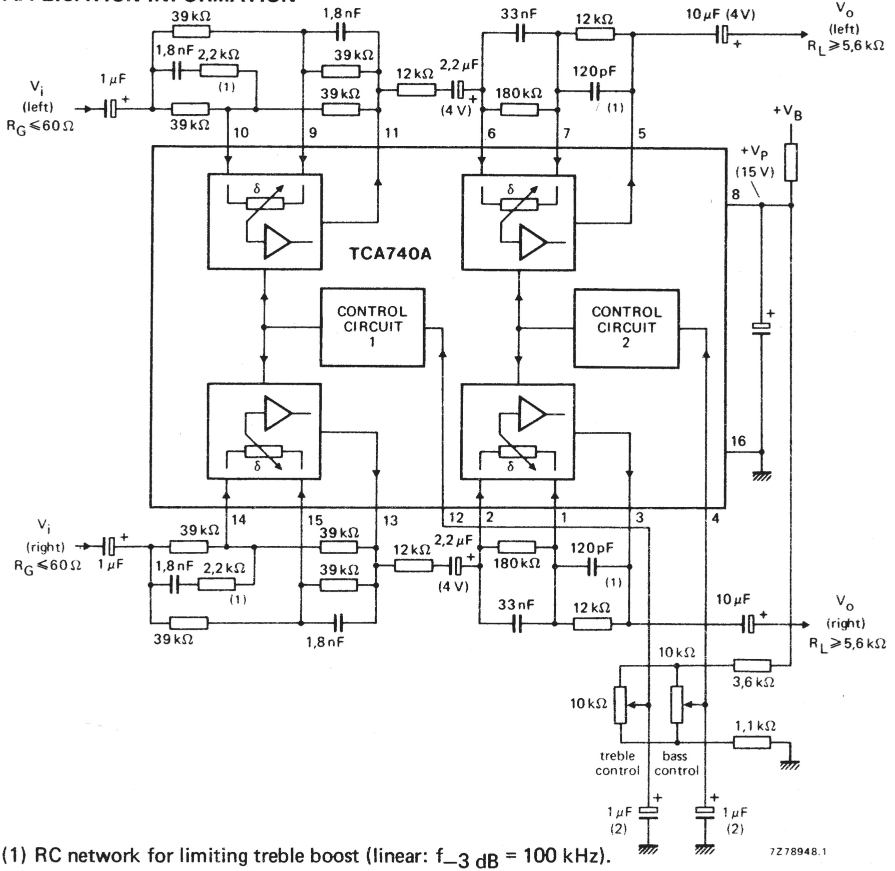


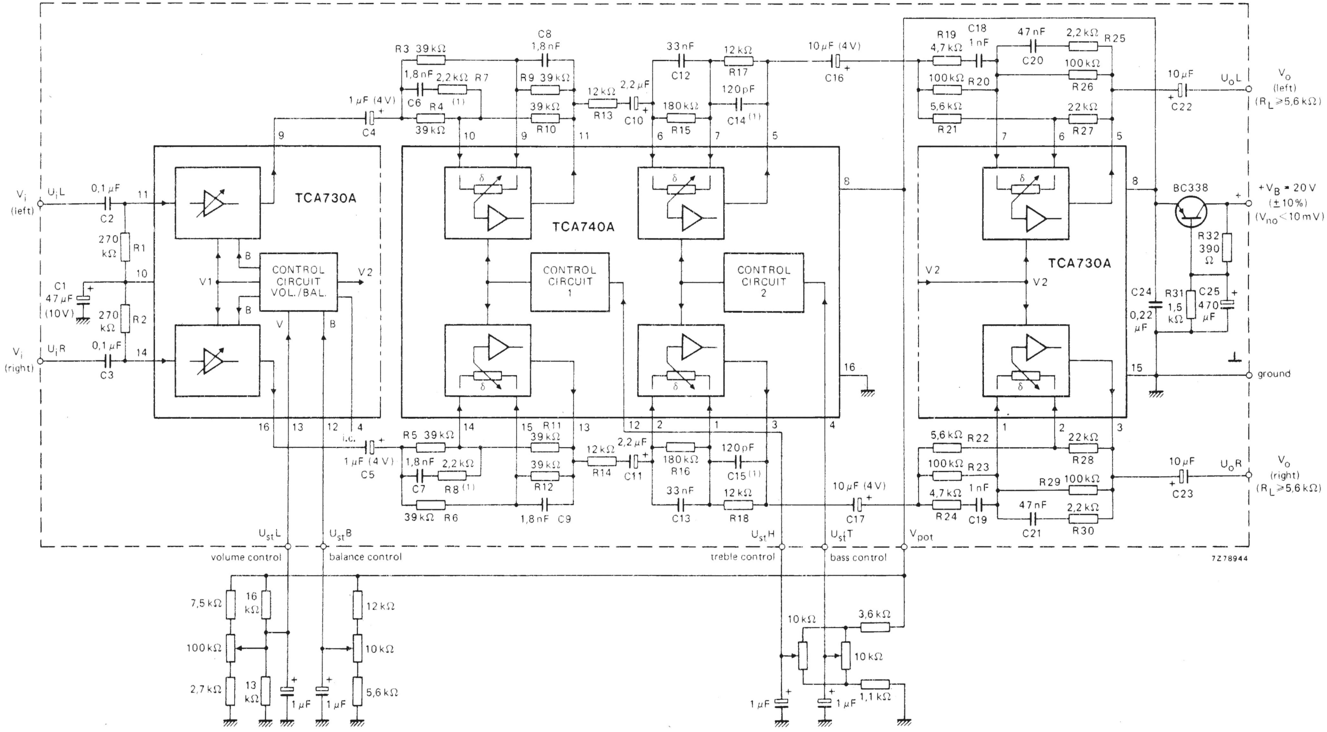
Fig. 5 Total distortion as a function of output voltage; $V_{4\text{-}16} = V_{12\text{-}16} = 5{,}6$ V (linear, $G_{v\,tot} = 1$); ——— f = 1 kHz; – – – f = 40 Hz to 16 kHz.

APPLICATION INFORMATION


39 kΩ
1,8 nF
33 nF
12 kΩ
10 μF (4 V)
V$_o$ (left) R$_L$ ≥ 5,6 kΩ
1,8 nF
2,2 kΩ
39 kΩ
12 kΩ
2,2 μF
120 pF
V$_i$ (left) R$_G$ ≤ 60 Ω
1 μF
(1)
39 kΩ
(4 V)
180 kΩ
(1)
+V$_B$
39 kΩ
10
9
11
6
7
5
+V$_P$ (15 V)
8
δ
TCA740A
CONTROL CIRCUIT 1
CONTROL CIRCUIT 2
16
14
15
13
12
2
1
3
4
V$_i$ (right) R$_G$ ≤ 60 Ω
39 kΩ
2,2 μF
180 kΩ
120 pF
1 μF
1,8 nF
2,2 kΩ
12 kΩ
(4 V)
(1)
(1)
33 nF
12 kΩ
10 μF
V$_o$ (right) R$_L$ ≥ 5,6 kΩ
39 kΩ
1,8 nF
10 kΩ
3,6 kΩ
10 kΩ
1,1 kΩ
treble control
bass control
1 μF (2)
1 μF (2)
7Z78948.1

(1) RC network for limiting treble boost (linear: $f_{-3\ dB} = 100$ kHz).
(2) Capacitors are intended for suppression of the noise when adjusting the mechanical potentiometers.

Fig. 6 Application example of TCA740A used for treble and bass control.


TCA730A
TCA740A
TCA730A
CONTROL CIRCUIT VOL./BAL.
CONTROL CIRCUIT 1
CONTROL CIRCUIT 2
BC338
V_i (left)
V_i (right)
U_iL
U_iR
V_o (left) ($R_L \geq 5,6\,k\Omega$)
V_o (right) ($R_L \geq 5,6\,k\Omega$)
U_oL
U_oR
$+V_B = 20\,V$ ($\pm 10\%$) ($V_{no} < 10\,mV$)
ground
$U_{st}L$
volume control
$U_{st}B$
balance control
$U_{st}H$
treble control
$U_{st}T$
bass control
V_{pot}
V1
V2
V
B
i.c.
C1 47 µF (10V)
C2 0,1 µF
C3 0,1 µF
R1 270 kΩ
R2 270 kΩ
C4 1 µF (4 V)
C5 1 µF (4 V)
R3 39 kΩ
R4 39 kΩ
R5 39 kΩ
R6 39 kΩ
C6 1,8 nF
R7 2,2 kΩ (1)
C7 1,8 nF
R8 2,2 kΩ (1)
C8 1,8 nF
C9 1,8 nF
R9 39 kΩ
R10 39 kΩ
R11 39 kΩ
R12 39 kΩ
R13 12 kΩ
R14 12 kΩ
C10 2,2 µF
C11 2,2 µF
C12 33 nF
C13 33 nF
R15 180 kΩ
R16 180 kΩ
R17 12 kΩ
R18 12 kΩ
C14 120 pF (1)
C15 120 pF (1)
C16 10 µF (4 V)
C17 10 µF (4 V)
R19 4,7 kΩ
C18 1 nF
R20 100 kΩ
R21 5,6 kΩ
R22 5,6 kΩ
R23 100 kΩ
R24 4,7 kΩ
C19 1 nF
C20 47 nF
C21 47 nF
R25 2,2 kΩ
R26 100 kΩ
R27 22 kΩ
R28 22 kΩ
R29 100 kΩ
R30 2,2 kΩ
C22 10 µF
C23 10 µF
C24 0,22 µF
R31 1,5 kΩ
C25 470 µF
R32 390 Ω
7,5 kΩ
16 kΩ
100 kΩ
2,7 kΩ
13 kΩ
1 µF
12 kΩ
10 kΩ
5,6 kΩ
10 kΩ
3,6 kΩ
10 kΩ
1,1 kΩ
δ
7Z78944

(1) RC network for limiting treble boost (linear: $f_{-3\,dB} = 100\,kHz$).

Fig. 7 Application diagram for TCA730A and TCA740A.
For printed-circuit board see Fig. 8.

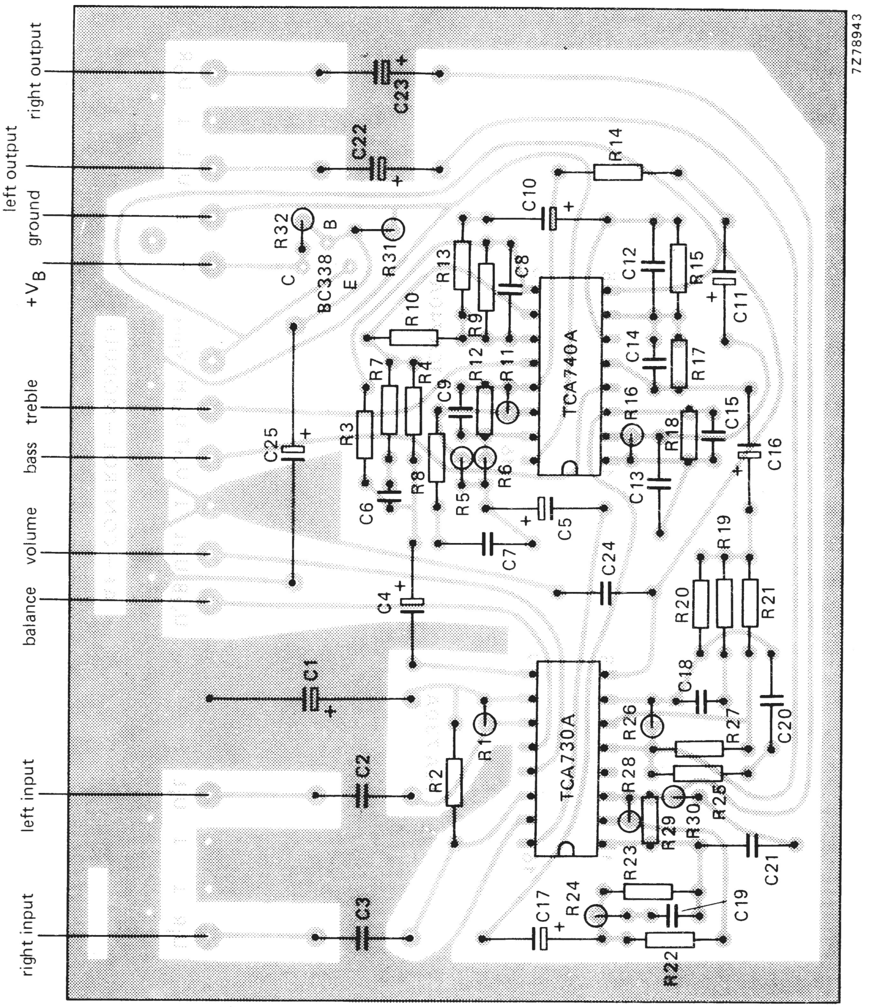

7Z78943
right output
left output
ground
+V_B
treble
bass
volume
balance
left input
right input
TCA740A
TCA730A
BC338
C
B
E
R32
R31
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
+

Fig. 8 Printed-circuit board component side, showing component layout; for circuit diagram see Fig. 7.

INTERFERENCE AND NOISE SUPPRESSION CIRCUIT FOR FM RECEIVERS

GENERAL DESCRIPTION

The TDA1001B is a monolithic integrated circuit for suppressing interference and noise in FM mono and stereo receivers.

Features

- Active low-pass and high-pass filters
- Interference pulse detector with adjustable and controllable response sensitivity
- Noise detector designed for FM i.f. amplifiers with ratio detectors or quadrature detectors
- Schmitt trigger for generating an interference suppression pulse
- Active pilot tone generation (19 kHz)
- Internal voltage stabilization

QUICK REFERENCE DATA

Supply voltage (pin 9)	V_P	typ.	12	V
Supply current (pin 9)	I_P	typ.	14	mA
A.F. input signal handling (pin 1) (peak-to-peak value)	$V_{i(p-p)}$	typ.	1	V
Input resistance (pin 1)	R_i	min.	35	kΩ
Voltage gain (V_{1-16}/V_{6-16})	G_v	typ.	0,5	dB
Total harmonic distortion	THD	typ.	0,25	%
Bandwidth	B	typ.	70	kHz
Suppression pulse threshold voltage (peak value); $R_{13} = 0$	$V_{i(tr)OM}$	typ.	19	mV
Suppression pulse duration	t_s	typ.	27	µs
Supply voltage range (pin 9)	V_P		7,5 to 16	V
Operating ambient temperature range	T_{amb}		−30 to +80	°C

PACKAGE OUTLINE

TDA1001B: 16-lead DIL; plastic (SOT-38).
TDA1001BT: 16-lead mini-pack; plastic (SO-16; SOT-109A).

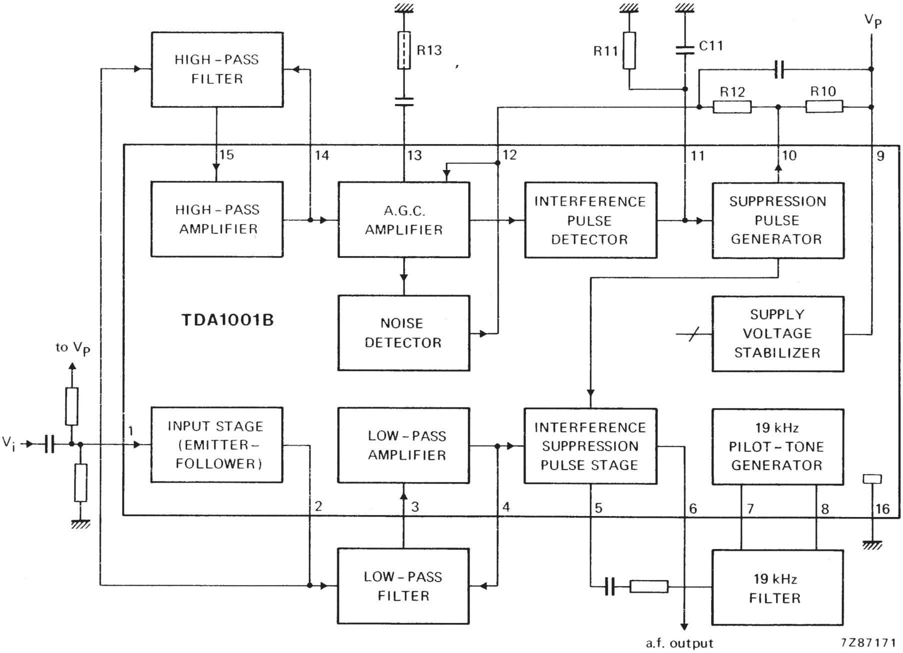

HIGH-PASS FILTER
R13
R11
C11
V_P
R12
R10
15
14
13
12
11
10
9
HIGH-PASS AMPLIFIER
A.G.C. AMPLIFIER
INTERFERENCE PULSE DETECTOR
SUPPRESSION PULSE GENERATOR
TDA1001B
NOISE DETECTOR
SUPPLY VOLTAGE STABILIZER
to V_P
V_i
1
INPUT STAGE (EMITTER-FOLLOWER)
LOW-PASS AMPLIFIER
INTERFERENCE SUPPRESSION PULSE STAGE
19 kHz PILOT-TONE GENERATOR
2
3
4
5
6
7
8
16
LOW-PASS FILTER
19 kHz FILTER
a.f. output
7Z87171

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	V_P	max.	18 V
Input voltage (pin 1)	$V_{1\text{-}16}$	max.	V_P V
Output current (pin 6)	I_6	max.	1 mA
	$-I_6$	max.	15 mA
Total power dissipation	see derating curves Fig. 2		
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−30 to +80 °C

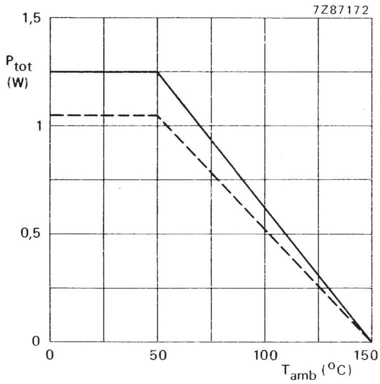


Fig. 2 Power derating curves.

——— in plastic DIL (SOT-38) package (TDA1001B)

– – – – in plastic mini-pack (SO-16; SOT-109A) package (TDA1001BT); mounted on a ceramic substrate of 50 x 15 x 0,7 mm.

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Input stage					
Input impedance (pin 1) f = 40 kHz	$\|Z_{i1}\|$	–	45	–	kΩ
Input resistance (pin 1) with pin 2 not connected	R_{i1}	–	600	–	kΩ
Input bias current (pin 1) $V_{1\text{-}16}$ = 4,8 V	I_{i1}	–	6	15	μA
Output resistance (pin 2) unloaded	R_{o2}		low-ohmic		
Internal emitter resistance	$R_{2\text{-}16}$	–	5,6	–	kΩ
Low-pass amplifier					
Input resistance (pin 3)	R_{i3}	10	–	–	MΩ
Input bias current (pin 3)	I_{i3}	–	–	7	μA
Output resistance (pin 4)	R_{o4}	–	–	5	Ω
Voltage gain (V_4/V_3)	$G_{v4/3}$	–	1,1	–	
Suppression pulse stage					
Input offset current at pin 5 during the suppression time t_s	I_{io5}	–	50	200	nA
Output stage					
Output resistance (pin 6)	R_{o6}		low-ohmic		
Internal emitter resistance	$R_{6\text{-}16}$	–	6	–	kΩ
Current gain (I_5/I_6)	$G_{i5/6}$	–	85	–	dB
Pilot tone generation (19 kHz)					
Input impedance (pin 8)	$\|Z_{i8}\|$	–	–	1	Ω
Output impedance (pin 7) pin 8 open	$\|Z_{o7}\|$	150	–	–	kΩ
Output bias current (pin 7)	I_{o7}	0,7	1	1,3	mA
Current gain (I_7/I_8)	$G_{i7/8}$	–	3	–	
High-pass amplifier					
Input resistance (pin 15)	R_{i15}	10	–	–	MΩ
Input bias current (pin 15)	I_{i15}	–	–	7	μA
Output resistance (pin 14)	R_{o14}	–	–	5	Ω
Voltage gain ($V_{14/15}$)	$G_{v14/15}$	–	1,4	–	

parameter	symbol	min.	typ.	max.	unit
A.G.C. amplifier; interference and noise detectors					
Internal resistance (pins 13 and 14)	$R_{13\text{-}14}$	1,5	2,0	2,5	kΩ
Operational threshold voltage (uncontrolled); peak value (pin 14)					
of the interference pulse detector	$\pm V_{14int\,m}$	–	15	–	mV
of the noise detector	$\pm V_{14n\,m}$	–	6,5	–	mV
Output voltage (peak value; pin 11)	$V_{11\text{-}16M}$	5,2	5,8	6,4	V
Output control current (pin 12) (peak value)	I_{12M}	150	200	250	μA
Output bias current (pin 12)	I_{o12}	–	2,5	6	μA
Input threshold voltage for onset of control (pin 12)	$V_{12\text{-}9}$	360	425	500	mV
($V_{i(tr)O}$ + 3 dB)	or:	–	$0{,}66V_{BE}$	–	mV
Suppression pulse generation (Schmitt trigger)					
Switching threshold (pin 11)					
1: gate disabled	$V_{11\text{-}16}$	–	3,2	–	V
2: gate enabled	$V_{11\text{-}16}$	–	2,0	–	V
Switching hysteresis	$\Delta V_{11\text{-}16}$	–	1,2	–	V
Input offset current (pin 11)	I_{io11}	–	–	100	nA
Output current (pin 10) gate disabled; peak value	I_{o10M}	0,6	1	1,4	mA
Reverse output current (pin 10)	I_{R10}	–	–	2	μA
Sensitivity (pin 10)	$V_{10\text{-}16}$	2,5	–	–	V

DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION

V_P = 12 V; T_{amb} = 25 °C; f = 1 kHz; measured in Fig. 4; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 9)	V_P	7,5	12	16	V
Quiescent supply current (pin 9)	I_P	10	14	18	mA
Signal path					
D.C. input voltage (pin 1)	$V_{1\text{-}16}$	–	4,5	–	V
Input impedance (pin 1); f = 40 kHz	$\lvert Z_{i1}\rvert$	35	–	–	kΩ
D.C. output voltage (pin 6)	$V_{6\text{-}16}$	2,4	2,8	–	V
Output resistance (pin 6)	R_{o6}		low-ohmic		
Voltage gain (V_6/V_1)	$G_{v6/1}$	0	0,5	1	dB
–3 dB point of low-pass filter	$f_{(-3dB)}$	–	70	–	kHz
Sensitivity for THD < 0,5% (peak-to-peak value)	$V_{i(p\text{-}p)}$	1,2	1,8	–	V
Residual interference pulse after suppression (see Fig. 3); pin 7 to ground; $V_{i(tr)M}$ = 100 mV; (peak-to-peak value)	$V_{6\text{-}16(p\text{-}p)}$	–	–	3	mV
Interference suppression at R13 = 0; notes 5 and 6; $V_{i(rms)}$ = 30 mV; f = 19 kHz (sinewave); $V_{i(tr)M}$ = 60 mV; f_r = 400 Hz	α_{int}	20	30	–	dB
Interference processing					
Input signal at pin 1; output signal at pin 10					
Suppression pulse threshold voltage; control function OFF (pin 9 connected to pin 12); r.m.s. value; note 1					
measured with sinewave input signal f = 120 kHz; $-V_{10\text{-}9} > 1$ V at R13 = 0 Ω	$V_{i(tr)rms}$	8	11	14	mV
at R13 = 2,7 kΩ	$V_{i(tr)rms}$	18	28,5	40	mV
voltage difference for safe triggering/ non-triggering (r.m.s. value)	$\Delta V_{i(rms)}$	–	1	–	mV
measured with interference pulses f = 400 Hz (see Fig. 3); peak value at R13 = 0 Ω	$V_{i(tr)M}$	–	19	–	mV
at R13 = 2,7 kΩ	$V_{i(tr)M}$	–	45	–	mV
Suppression pulse duration (note 2)	t_s	24	27	30	μs

parameters	symbol	min.	typ.	max.	unit
Noise threshold feedback control (notes 1 and 3)					
Noise input voltage (r.m.s. value) f = 120 kHz sinewave					
for $V_{12\text{-}9}$ = 300 mV					
at R13 = 0 Ω	$V_{ni(rms)}$	2,3	3,3	4,3	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	8,2	–	mV
for $V_{12\text{-}9}$ = 425 mV ($V_{i(tr)O}$ + 3 dB)					
at R13 = 0 Ω	$V_{ni(rms)}$	–	7,3	–	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	16,5	–	mV
for $V_{12\text{-}9}$ = 560 mV ($V_{i(tr)O}$ + 20 dB)					
at R13 = 0 Ω	$V_{ni(rms)}$	33	45	57	mV
at R13 = 2,7 kΩ	$V_{ni(rms)}$	–	107	–	mV
Amplification control voltage by interference intensity (note 4) $V_{i(rms)}$ = 50 mV; f = 19 kHz; $V_{i(tr)M}$ = 300 mV; r.m.s. value					
at repetition frequency f_r = 1 kHz	$V_{o6(rms)}$	49	–	56	mV
at repetition frequency f_r = 16 kHz	$V_{o6(rms)}$	45	–	65	mV

DEVELOPMENT SAMPLE DATA

Notes to application information

1. The interference suppression and noise feedback control thresholds can be determined by R13 or a capacitive voltage divider at the input of the high-pass filter and they are defined by the following formulae:
   $V_{i(tr)} = (1 + R13/R_S) \times V_{i(tr)O}$ in which $R_S = 2\ k\Omega$;
   $V_{ni} = (1 + R13/R_S) \times V_{niO}$ in which $R_S = 2\ k\Omega$.
2. The suppression pulse duration is determined by C11 = 2,2 nF and R11 = 6,8 kΩ.
3. The characteristic of the noise feedback control is determined by R12 (and R10).
4. The feedback control of the interference suppression threshold at higher repetition frequencies is determined by R10 (and R12).
5. The 19 kHz generator can be adjusted with $R_{7\text{-}16}$ (and $R_{7\text{-}8}$). Adjustment is not required if components with small tolerances are used e.g. $\Delta R < 1\%$ and $\Delta C < 2\%$.
6. Measuring conditions:
   The peak output noise voltage ($V_{no\ m}$, CCITT filter) shall be measured at the output with a de-emphazing time T = 50 μs (R = 5 kΩ, C = 10 nF); the reference value of 0 dB is $V_{o\ int}$ with the 19 kHz generator short-circuited (pin 7 grounded).

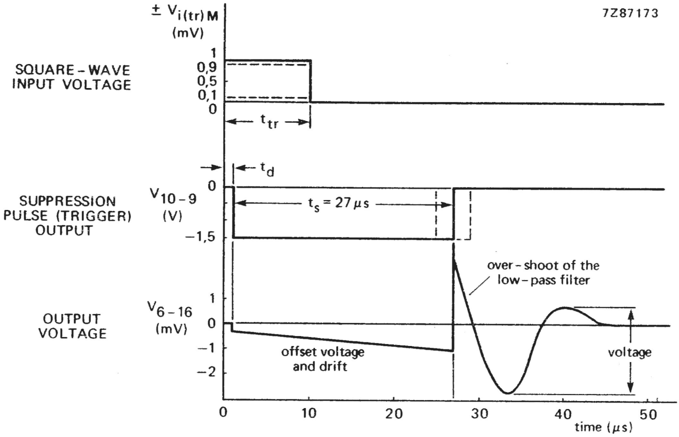


Fig. 3 Measuring signal for interference suppression; at the input (pin 1) a square-wave is applied with a duration of t_{tr} = 10 μs and with rise and fall times $t_r = t_f$ = 10 ns.

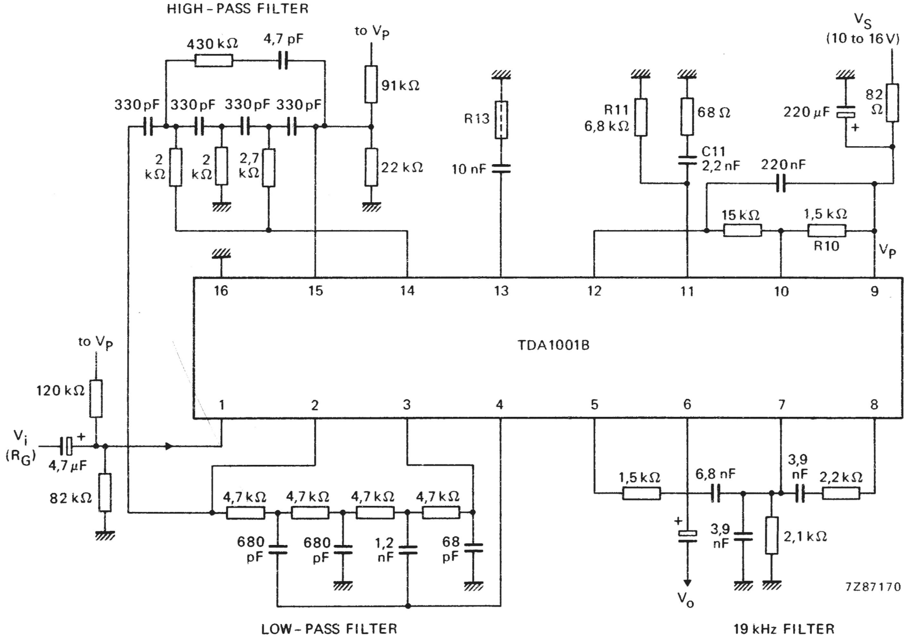

HIGH-PASS FILTER
430 kΩ
4,7 pF
to V_P
91 kΩ
22 kΩ
330 pF
330 pF
330 pF
330 pF
2 kΩ
2 kΩ
2,7 kΩ
R13
10 nF
R11 6,8 kΩ
68 Ω
C11 2,2 nF
220 nF
V_S (10 to 16 V)
82 Ω
220 µF
+
15 kΩ
1,5 kΩ
R10
V_P
16
15
14
13
12
11
10
9
TDA1001B
1
2
3
4
5
6
7
8
to V_P
120 kΩ
V_i (R_G)
+
4,7 µF
82 kΩ
4,7 kΩ
4,7 kΩ
4,7 kΩ
4,7 kΩ
680 pF
680 pF
1,2 nF
68 pF
LOW-PASS FILTER
1,5 kΩ
6,8 nF
3,9 nF
2,2 kΩ
+
3,9 nF
2,1 kΩ
V_o
7Z87170
19 kHz FILTER

Fig. 4 Application circuit diagram.

DEVELOPMENT SAMPLE DATA

RECORDING AND PLAYBACK AMPLIFIER

This integrated circuit incorporates all amplifier circuits necessary for the record/playback functions, with the exception of the audio power output amplifier. It comprises:
- a preamplifier for microphone or playback,
- a recording amplifier with automatic level control,
- a dynamic limiter with a short limiting time.

Compared to its predecessor TDA1002, this type features an improved automatic level control circuit; the control range has been enlarged from 40 to 55 dB and the spread in control characteristic has been reduced to less than 2 dB.

QUICK REFERENCE DATA

Supply voltage range	V_P		4 to 12	V
Operating ambient temperature	T_{amb}		−25 to + 125	°C
Total quiescent current (V_P = 9 V)	I_{tot}	typ.	15	mA
Preamplifier				
Input impedance (pin 1)	$\lvert Z_i \rvert$	typ.	16	kΩ
Open loop gain	G_o	typ.	70	dB
Clipping level (pin 4); V_P = 9 V; r.m.s. value	$V_{4\text{-}5(rms)}$	typ.	2	V
Equivalent noise input voltage R_S = 500 Ω; B = 300 Hz to 15 kHz	$V_{n(rms)}$	<	0,75	μV
Recording amplifier				
Input impedance (pin 8)	$\lvert Z_i \rvert$	typ.	40	kΩ
Open loop gain	G_o	typ.	80	dB
Clipping level (pin 9); V_P = 9 V; r.m.s. value	$V_{9\text{-}10(rms)}$	typ.	2	V
Automatic Level Control (A.L.C.)				
Input impedance (pin 6)				
at low signal level at pin 8	$\lvert Z_i \rvert$	typ.	250	kΩ
at high signal level pin 8	$\lvert Z_i \rvert$	typ.	25	Ω
Control voltage				
$V_{4\text{-}5}$ = 10 mV; f = 1 kHz; V_P = 9 V	$V_{9\text{-}10}$	typ.	250	mV
$V_{4\text{-}5}$ = 1000 mV; f = 1 kHz; V_P = 9 V	$V_{9\text{-}10}$	typ.	750	mV
Limiting time (Fig. 12)	t_l	typ.	10	ms
Level setting time (Fig. 12)	t_s	typ.	4	s
Recovery time (Fig. 13)	t_r	typ.	35	s

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

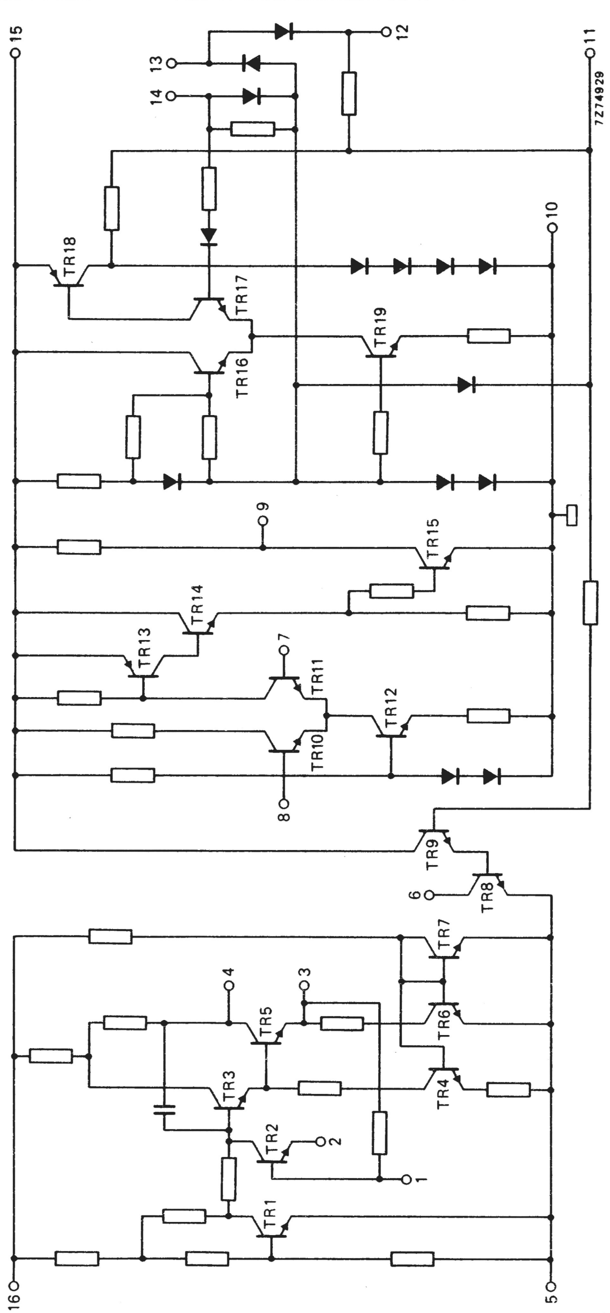

15
13
14
12
11
7Z74929
10
TR18
TR17
TR16
TR19
9
TR15
TR14
TR13
7
TR11
TR12
TR10
8
TR9
6
TR8
TR7
4
3
TR5
TR6
TR3
TR4
TR2
2
1
TR1
16
5

Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage preamplifier	$V_{16\text{-}5}$	max.	12 V
Supply voltage recording amplifier	$V_{15\text{-}10}$	max.	12 V
Total power dissipation			see derating curve Fig. 2
Storage temperature	T_{stg}		−65 to + 125 °C
Operating ambient temperature	T_{amb}		−25 to + 125 °C

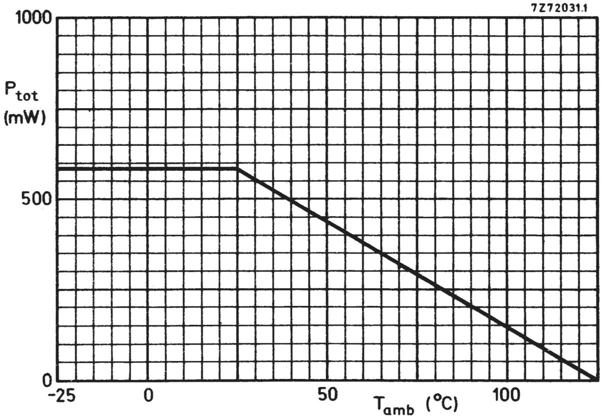


Fig. 2 Power dissipation derating curve.

D.C. CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

Supply voltage recording amplifier	$V_{15\text{-}10}$		4 to 12 V
Supply voltage preamplifier	$V_{16\text{-}5}$		4 to 12 V
Quiescent current rec. amplifier; V_P = 9 V	I_{15}	typ.	10 mA
Quiescent current preamplifier; V_P = 9 V	I_{16}	typ.	5 mA
Output voltage recording amplifier	$V_{9\text{-}10}$	typ.	½ V_P V
Output voltage preamplifier	$V_{4\text{-}5}$	typ.	½ V_P−0,35 V

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 9 V unless otherwise specified.

Preamplifier (note 1)			recording	playback	
Open loop voltage gain	G_o	typ.	70	70	dB
Closed loop voltage gain at f = 1 kHz	G_c	typ.	38	45	dB
Output voltage (clipping level); r.m.s. value	$V_{4\text{-}5(rms)}$	typ.	2	2	V
Equivalent noise input voltage; r.m.s. value (note 2)	V_n	<	0,75	0,75	µV
Input impedance (pin 1)	$\|Z_i\|$	typ.	16	16	kΩ
Total harmonic distortion					
f = 1 kHz; $V_{4\text{-}5}$ = 150 mV	d_t	typ.	–	0,12	%
f = 1 kHz; $V_{4\text{-}5}$ = 500 mV	d_t	<	0,2	–	
Amplitude response		flat: 20 Hz to 20 kHz		see Fig. 7	

Recording amplifier (Fig. 9)

with A.L.C.; unless otherwise specified.

Open loop gain	G_o	typ.	80	dB
Closed loop voltage gain at f = 1 kHz (note 3)	G_c	typ.	49	dB
Output voltage (clipping level); r.m.s. value	$V_{9\text{-}10(rms)}$	typ.	2	V
Input impedance pin 8	$\|Z_i\|$	typ.	40	kΩ
Input impedance pin 6				
low signal levels	$\|Z_i\|$	typ.	250	kΩ
high signal levels	$\|Z_i\|$	typ.	25	Ω
Total harmonic distortion		see Fig. 11		
Amplitude response (note 3)		see Fig. 10		

Automatic level control (see Fig. 8)

$V_{4\text{-}5}$ = 10 mV; f = 1 kHz	$V_{9\text{-}10}$	typ.	250	mV
$V_{4\text{-}5}$ = 100 mV; f = 1 kHz	$V_{9\text{-}10}$	typ.	450	mV
$V_{4\text{-}5}$ = 1000 mV; f = 1 kHz	$V_{9\text{-}10}$	typ.	750	mV
$V_{4\text{-}5}$ = 2000 mV; f = 1 kHz	$V_{9\text{-}10}$	typ.	880	mV
Limiting time (see Fig. 12)	t_l	typ.	10	ms
Level setting time (see Fig. 12)	t_s	typ.	4	s
Recovery time (see Fig. 13)	t_r	typ.	35	s

Notes

1. For recording see Fig. 3; for playback see Fig. 5.
2. R_S = 500 Ω; bandwidth = 300 Hz to 15 kHz.
3. Pin 6 not connected to pin 8.

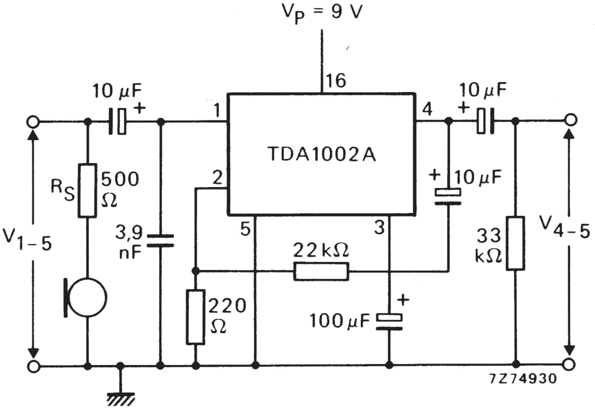

V_P = 9 V
16
10 µF
1
2
5
3
4
TDA1002A
R_S
500 Ω
3,9 nF
220 Ω
22 kΩ
100 µF
10 µF
10 µF
33 kΩ
V_{1-5}
V_{4-5}
7Z74930

Fig. 3 Preamplifier used as microphone amplifier.

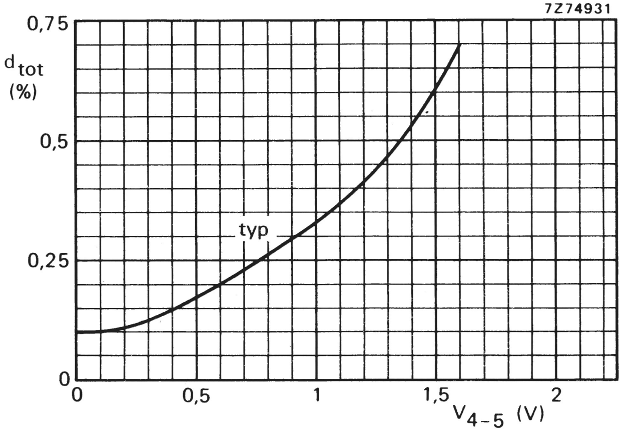
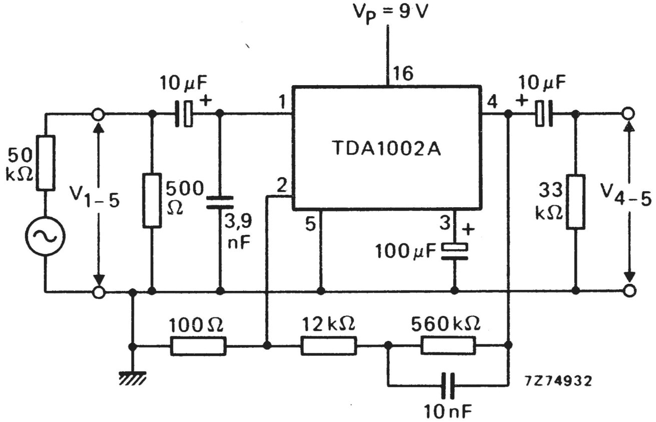


Fig. 4 Total harmonic distortion of preamplifier used for recording.



V_P = 9 V
16
10 μF
+
1
4
TDA1002A
50 kΩ
V1-5
500 Ω
3,9 nF
2
5
3
+
100 μF
33 kΩ
V4-5
100 Ω
12 kΩ
560 kΩ
10 nF
7Z74932

Fig. 5 Preamplifier used for playback.

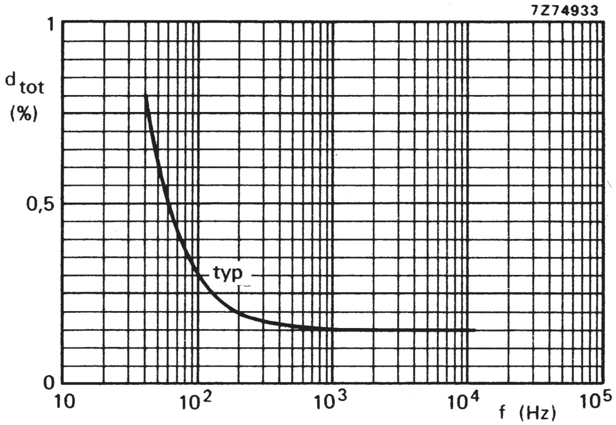


Fig. 6 Total harmonic distortion of preamplifier used for playback at V_{4-5} = 150 mV.

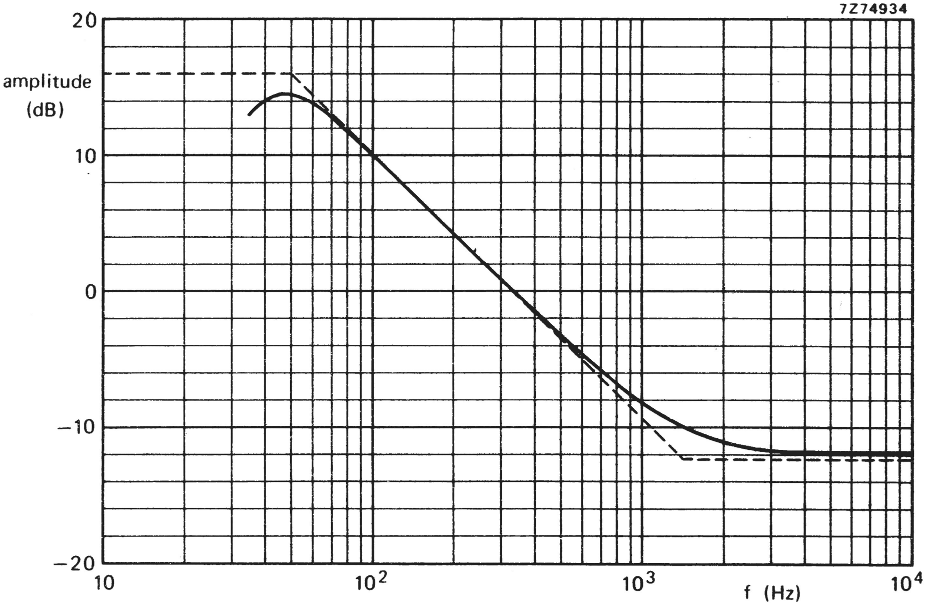


Fig. 7 Amplitude response of preamplifier used for playback; typical values. 0 dB = input voltage of 0,3 mV at f = 333 Hz. Dotted line according to DIN 45513.

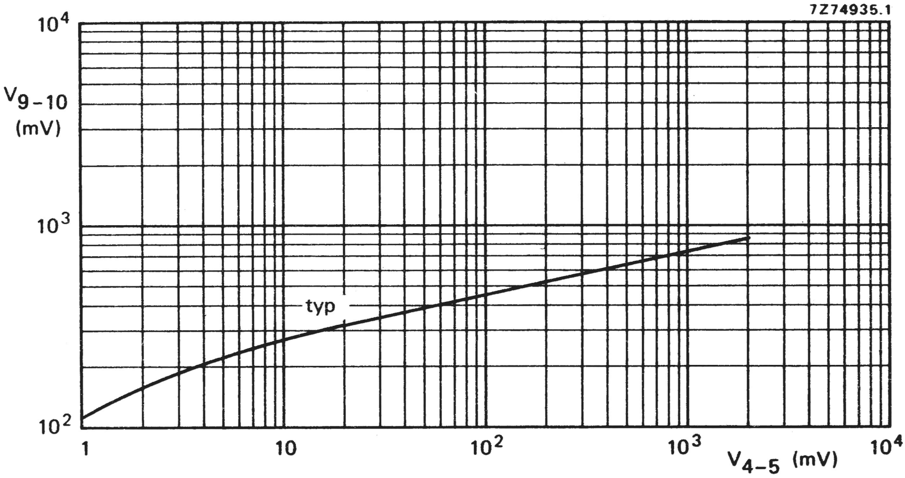


Fig. 8 Automatic level control; for circuitry see Fig. 9; f = 1 kHz.

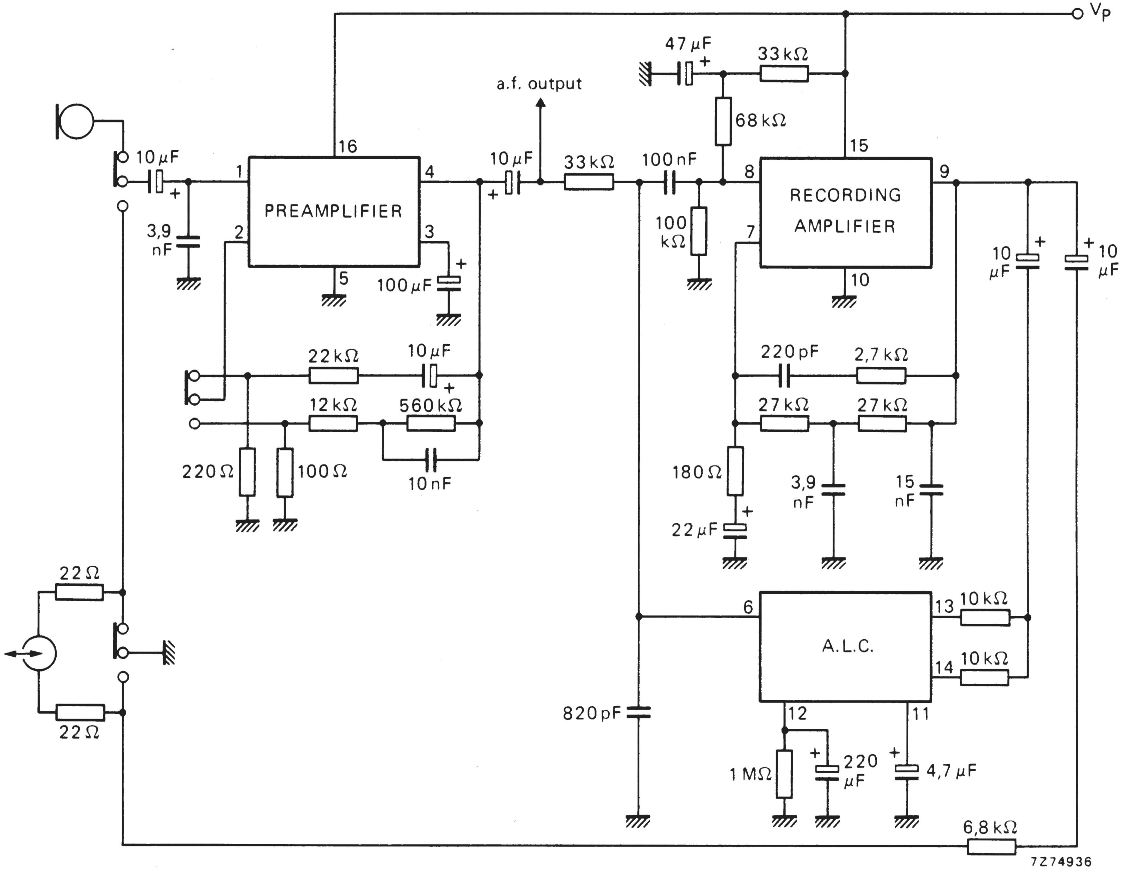

V_P
47 μF
33 kΩ
68 kΩ
a.f. output
10 μF
1
16
PREAMPLIFIER
4
2
3
5
3,9 nF
100 μF
10 μF
33 kΩ
100 nF
100 kΩ
15
8
9
RECORDING AMPLIFIER
7
10
10 μF
10 μF
22 kΩ
10 μF
12 kΩ
560 kΩ
220 Ω
100 Ω
10 nF
220 pF
2,7 kΩ
27 kΩ
27 kΩ
180 Ω
3,9 nF
15 nF
22 μF
22 Ω
22 Ω
6
A.L.C.
13
10 kΩ
14
10 kΩ
12
11
820 pF
1 MΩ
220 μF
4,7 μF
6,8 kΩ
7Z74936

Fig. 9 Application of TDA1002A (recording position).

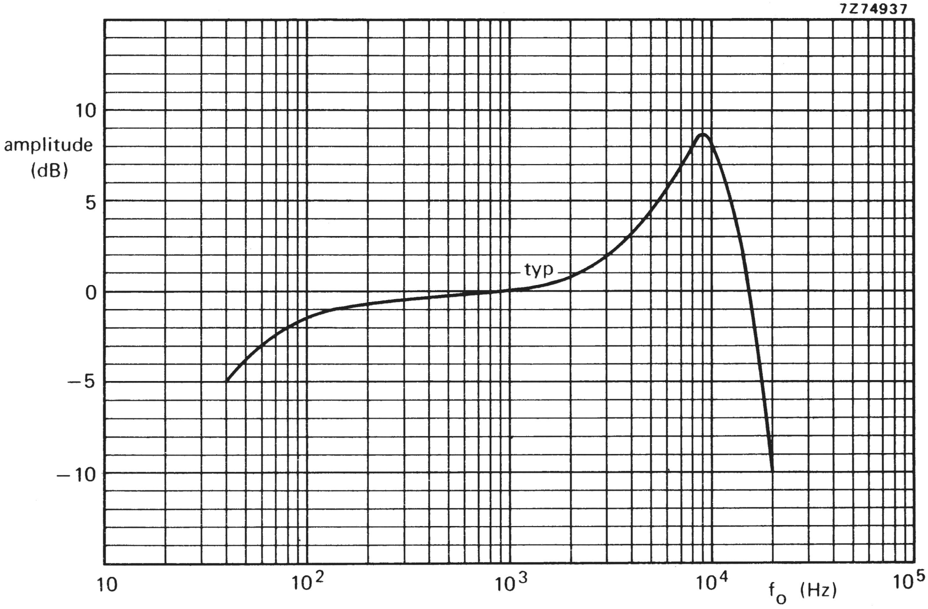


Fig. 10 Amplitude response of recording amplifier (A.L.C. not connected).

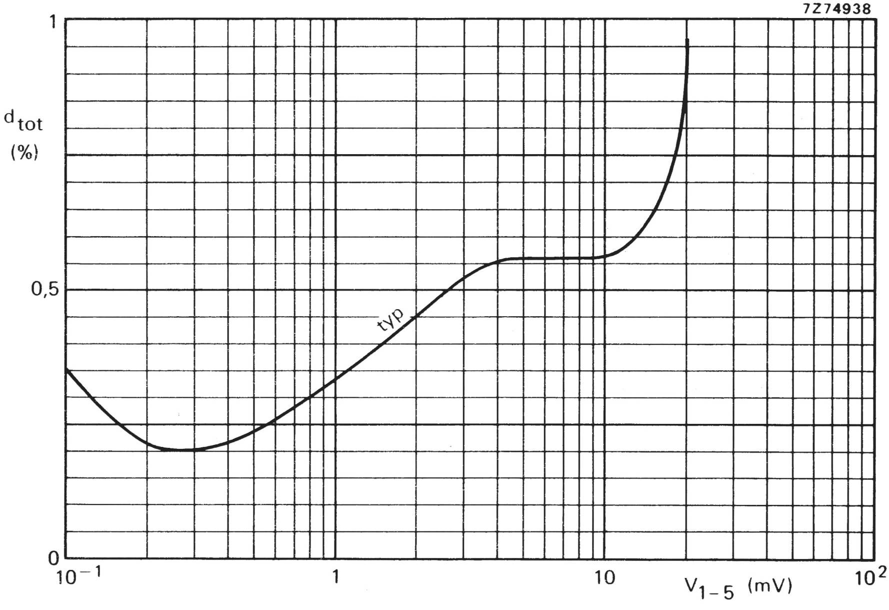
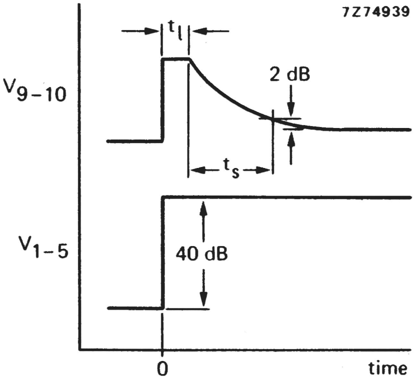


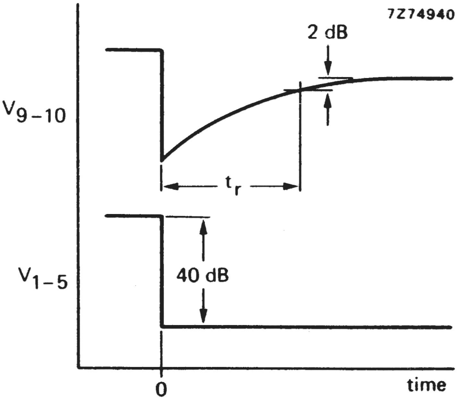
Fig. 11 Total harmonic distortion recording amplifier with A.L.C.; f = 1 kHz.

TIMING DIAGRAMS


7Z74939
t_l
2 dB
V_{9-10}
t_s
V_{1-5}
40 dB
0
time

t_l = limiting time.
t_s = level setting time.

Fig. 12 Output response at input level jumps.


7Z74940
2 dB
V_{9-10}
t_r
V_{1-5}
40 dB
0
time

t_r = recovery time.

Fig. 13 Output response at input level jumps.

FREQUENCY MULTIPLEX PLL STEREO DECODER

The TDA1005A is a high quality PLL stereo decoder based on the frequency-division multiplex (f.d.m.) principle, performing:

- excellent ACI (Adjacent Channel Interference) and SCA (Storecast) rejection
- very low BFC (Beat-Frequency Components) distortion in the higher frequency region

The circuit incorporates the following features:

- with simplified peripheral circuitry the circuit can perform as a time-division multiplex (t.d.m.) decoder, for use in economic medium and low-class apparatus
- for car radios: operation at a supply voltage of 8 V
- extra pin for smooth mono/stereo take-over without "clicks"
- automatic mono/stereo switching (minimum switching level is 16 mV), controlled by both pilot signal and field strength level
- low distortion in the loop resonance frequency region (≈ 300 Hz; THD = 0,2% typ.)
- external adjustment for obtaining optimum channel separation in the complete receiver
- internal amplification: t.d.m., 7 dB; f.d.m., 10 dB
- driver for stereo indicator lamp
- externally switchable: VCO-off or mono condition
- guaranteed VCO capture range (> 3,5% or 2,7 kHz)

QUICK REFERENCE DATA

Supply voltage range	$V_{8\text{-}16}$		8 to 18		V
Supply voltage	$V_{8\text{-}16}$	typ.	15		V
Ambient temperature	T_{amb}	typ.	25		°C
Measured at $V_{i(p\text{-}p)} = 1$ V (MUX signal with 8% pilot)			t.d.m.	f.d.m.	
Channel separation at f = 1 kHz	α	typ.	50	55	dB
Carrier suppression					
at f = 19 kHz	α_{19}	typ.	36	36	dB
at f = 38 kHz	α_{38}	typ.	45	40	dB
at f = 76 kHz	α_{76}	typ.	80	75	dB
ACI rejection at f = 114 kHz	α_{114}	typ.	52	70	dB
SCA rejection at f = 67 kHz	α_{67}	typ.	85	90	dB
VCO capture range		>	3,5	3,5	%
Total harmonic distortion					
$f_m = 1$ kHz	THD	typ.	0,2	0,1	%
$f_m = 300$ Hz to 10 kHz	THD	typ.	0,2	0,1	%
BFC suppression	d_{BFC}	>	40	60	dB

PACKAGE OUTLINES

TDA1005A ; 16-lead DIL; plastic (SOT-38).
TDA1005AT; 16-lead flat pack; plastic (SO-16; SOT-109A).

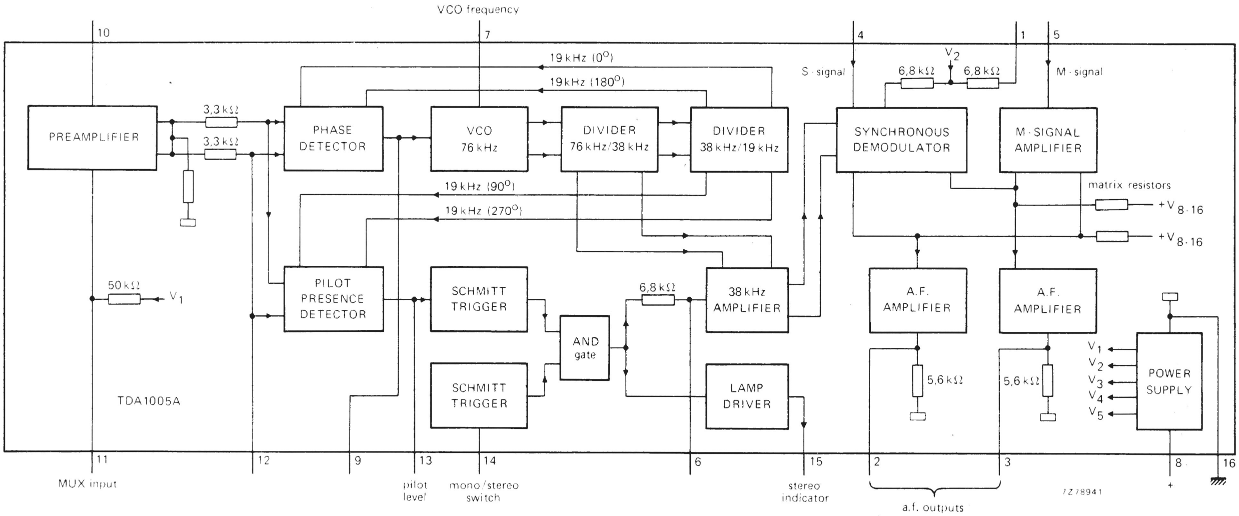

VCO frequency
10
7
4
1
5
19 kHz (0°)
19 kHz (180°)
S - signal
V2
6,8 kΩ
6,8 kΩ
M - signal
PREAMPLIFIER
3,3 kΩ
3,3 kΩ
PHASE DETECTOR
VCO 76 kHz
DIVIDER 76 kHz/38 kHz
DIVIDER 38 kHz/19 kHz
SYNCHRONOUS DEMODULATOR
M-SIGNAL AMPLIFIER
matrix resistors
+V 8-16
+V 8-16
19 kHz (90°)
19 kHz (270°)
50 kΩ
V1
PILOT PRESENCE DETECTOR
SCHMITT TRIGGER
6,8 kΩ
38 kHz AMPLIFIER
A.F. AMPLIFIER
A.F. AMPLIFIER
AND gate
5,6 kΩ
5,6 kΩ
V1
V2
V3
V4
V5
POWER SUPPLY
SCHMITT TRIGGER
LAMP DRIVER
TDA1005A
11
12
9
13
14
6
15
2
3
8
16
MUX input
pilot level
mono/stereo switch
stereo indicator
a.f. outputs
7Z78941
+

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{8\text{-}16}$	max.	18	V
Indicator lamp voltage	$V_{15\text{-}16}$	max.	22	V
Mono/stereo switching voltage	$V_{14\text{-}16}$	max.	4	V
Indicator lamp current	I_{15}	max.	100	mA
Indicator lamp turn-on current (peak value)	I_{15M}	max.	200	mA
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature (see also Fig. 2)	T_{amb}	−25 to + 150		°C

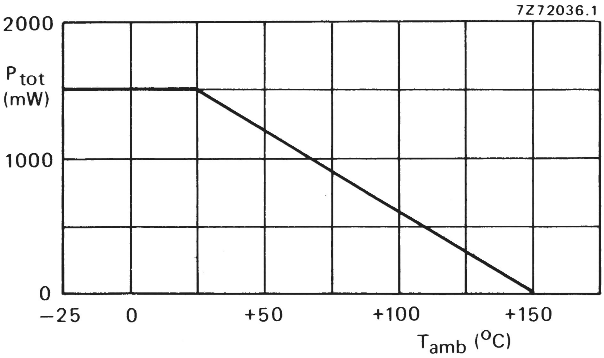


Fig. 2 Power derating curve.

A.C. CHARACTERISTICS and APPLICATION INFORMATION

T_{amb} = 25 °C; $V_{8\text{-}16}$ = 15 V (unless otherwise specified); see also Fig. 7 and Fig. 10.

	note	pin	parameter		t.d.m.	f.d.m.	unit
Channel separation see Figs 23 and 24	1, 2	2, 3	α	>	40	45	dB
				typ.	50	55	dB
F.M.—I.F. roll-off correction range	1, 2				48 to 72	—	kHz
Input MUX-voltage; L = 1; R = 1 for THD < 0,35%	1, 2	11	$V_{i(p\text{-}p)}$	typ.	1	1	V
Input impedance		11	$\lvert Z_i \rvert$	>	35	35	kΩ
				typ.	50	50	kΩ
Voltage gain per channel	1, 2		G_v	typ.	7	10	dB
Channel balance	1, 2		$\pm \Delta G_v$	<	1	1	dB
Output voltage (r.m.s. value) L = 1; R = 1	1, 2	2	$V_{2\text{-}16(rms)}$	>	0,61	0,97	V
		3	$V_{3\text{-}16(rms)}$	>	0,61	0,97	V
Output impedance	3	2, 3	$\lvert Z_o \rvert$	typ.	5,6	5,6	kΩ
					4 to 7	4 to 7	kΩ
Total harmonic distortion; see Figs 25 and 26							
f_m = 1 kHz (all conditions)	1	2, 3	THD	typ.	0,2	0,1	%
f_m = 1 kHz; L = 1; R = 1	1	2, 3	THD	<	0,35	0,35	%
f_m = 300 Hz to 10 kHz		2, 3	THD	typ.	0,2	0,1	%
Carrier suppression		2, 3					
f = 19 kHz; without notch filter	1		α_{19}	typ.	36	36	dB
f = 19 kHz; with notch filter	1, 9		α_{19}	typ.	60	60	dB
f = 38 kHz; without notch filter	1		α_{38}	>	40	38	dB
f = 38 kHz; with notch filter	1, 9		α_{38}	>	72	72	dB
f = 57 kHz; without notch filter	1		α_{57}	typ.	46	56	dB
f = 57 kHz; with notch filter	1, 9		α_{57}	typ.	59	61	dB
f = 76 kHz; without notch filter	1		α_{76}	typ.	80	75	dB
ACI rejection		2, 3					
at f = 114 kHz	4		α_{114}	typ.	52	70	dB
at f = 190 kHz	4		α_{190}	typ.	55	74	dB
SCA rejection at f = 67 kHz	5	2, 3	α_{67}	typ.	85	90	dB
Ripple rejection; f = 100 Hz; $V_{8\text{-}16(rms)}$ = 200 mV			RR	>	40	40	dB
				typ.	50	50	dB

	note	pin	parameter		t.d.m.	f.d.m.	unit
VCO; adjustable with R_{7-16}							
nominal frequency	6		f_{VCO}	typ.	76	76	kHz
capture range (deviation from 76 kHz centre frequency) 19 kHz pilot signal of 32 mV	6			>	3,5	3,5	%
temperature coefficient							
uncompensated	6		$-TC$	typ.	450.10^{-6}	450.10^{-6}	K^{-1}
compensated	6		$\pm TC$	typ.	200.10^{-6}	200.10^{-6}	K^{-1}
Stereo/mono switch							
when equal to 19 kHz pilot-tone threshold voltage; adjustable with R_{13-8}	7	11	V_i		10 to 100	10 to 100	mV
when equal to threshold voltage at R_{13-8} = 620 kΩ							
for switching to stereo		11	V_i		7 to 16	7 to 16	mV
for switching to mono		11	V_i	<	5	5	mV
hysteresis	8	11	ΔV_i	typ.	2,5	2,5	dB
Smooth take-over circuit							
full mono	8	6	V_{6-16}	<	0,65	0,65	V
full stereo	8	6	V_{6-16}	>	1,3	1,3	V

Notes

1. $V_{i(p-p)} = 1$ V (MUX signal with 8% pilot level).
2. $f_m = 1$ kHz.
3. At supply voltages of 8 to 11 V, resistors of 5,6 kΩ have to be connected from ground to pins 2 and 3.
4. Measured with a composite input signal: L = R; f_m = 1 kHz; 90% M-signal; 9% pilot signal; 1% spurious signal of 110 kHz (for α_{114}) or 186 kHz (for α_{190}).
   ACI suppression is defined as: $20 \log \frac{V_o \text{ (at 4 kHz)}}{V_o \text{ (at 1 kHz)}}$.
5. Measured with a composite input signal: L = R; f_m = 1 kHz; 80% S-signal; 9% pilot signal; 10% SCA carrier (67 kHz); $d_{13} = 20 \log \frac{V_o \text{ (at 9 kHz)}}{V_o \text{ (at 1 kHz)}}$.
6. See also Figs 7 and 10; compensated with RC network on pin 7.
7. Adjustable with R_{13-8}; see also Fig. 28; for field strength dependent input (pin 14) see next page.
8. $\Delta V_i = 20 \log \frac{V_{11-16} \text{ (mono/stereo)}}{V_{11-16} \text{ (stereo/mono)}}$.
   For additional circuitry on pin 6 see Figs 7 and 10; for graph see Fig. 29.
9. For example of notch filter see Fig. 6.

D.C. CHARACTERISTICS

T_{amb} = 25 °C; V_{8-16} = 15 V (unless otherwise specified)

Supply voltage range	V_{8-16}		8 to 18	V *
Total current (except indicator lamp)	I_8	typ.	21	mA
Power dissipation (operating) at lamp current I_{15} = 100 mA; V_{8-16} = 18 V	P_{tot}	<	570	mW
Saturation voltage of lamp driver at I_{15} = 100 mA	V_{15-16}	typ.	0,9	V
Maximum lamp driver voltage	V_{15-16}	<	22	V
Switching voltage				
to mono	V_{14-16}	>	1,2	V **
to stereo	V_{14-16}	<	0,65	V
hysteresis	V_{14-16}	typ.	0,2	V

APPLICATION NOTES

1. Switching-off the VCO

If the internal gain is used with A.M. reception, the VCO can be switched off by connecting pin 9 via a 100 kΩ resistor to ground (no h.f. signal on the leads), or connecting pin 7 to ground.

2. Mono button

The decoder can be switched to the mono position by connecting pin 12 to ground. The VCO then remains operational so this possibility cannot be used with A.M. reception.

3. Economic periphery

a. For a fixed stereo switching level of ⩽ 16 mV a resistor of 620 kΩ can be connected between pin 13 and positive supply (+) instead of a potentiometer in series with a resistor.
b. The 10 kΩ resistor connected in parallel with the stereo indicator lamp can be omitted, however, some TDA1005A circuits will switch to mono during lamp failure.
c. The 10 μF capacitor in series with a 1 kΩ resistor at pin 9 can be decreased to a 1 μF capacitor, bearing in mind that the distortion will increase, especially around loop resonance.
d. A MUX-input filter is not needed, if i.f. roll-off starts at a frequency of 62 kHz.

4. Printed-circuit boards

For both the f.d.m. and t.d.m. stereo decoder circuits a printed-circuit board layout is given as an example (Figs 8 and 11). Also for an active filter, which is mainly used with a t.d.m. decoder, a printed-circuit board layout is given in Fig. 4.

5. Notch filter

If attention has to be paid for suppression of the 57 kHz signal (T.W.S. = Traffic Warning System) and the 19 kHz signal, an input filter can be used as given in Fig. 6.

---

* At supply voltages of 8 to 11 V, resistors of 5,6 kΩ have to be connected from ground to pins 2 and 3.

** Maximum voltage for safe operation: $V_{14-16} < 4$ V.

APPLICATION INFORMATION

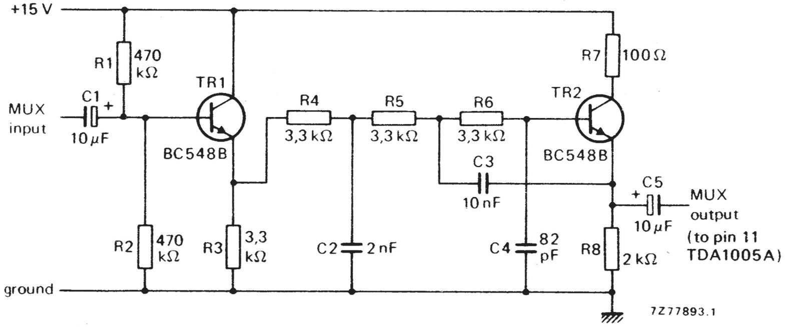

+15 V
R1
470 kΩ
C1
+
10 µF
MUX input
TR1
BC548B
R2
470 kΩ
R3
3,3 kΩ
R4
3,3 kΩ
R5
3,3 kΩ
R6
3,3 kΩ
C2
2 nF
C3
10 nF
C4
82 pF
R7
100 Ω
TR2
BC548B
C5
+
10 µF
MUX output (to pin 11 TDA1005A)
R8
2 kΩ
ground
7Z77893.1

Fig. 3 Active filter circuit diagram.

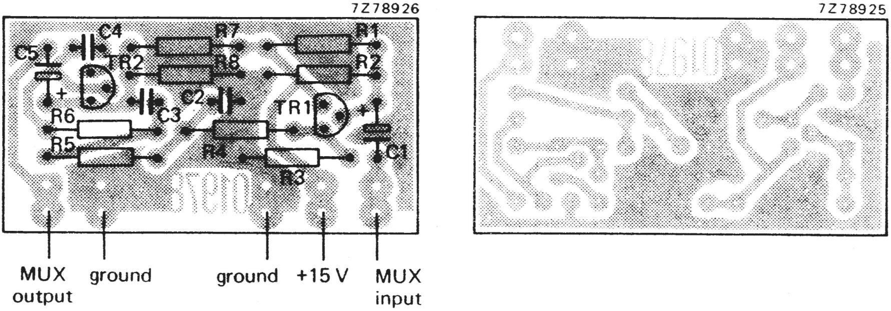
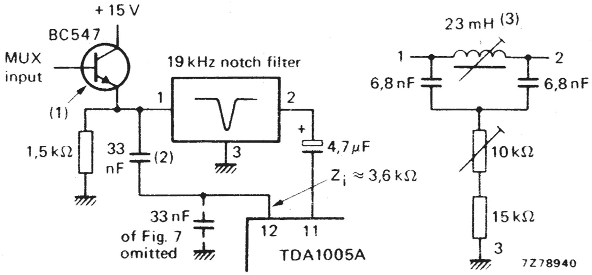

7Z78926
C4
R7
R1
C5
TR2
R8
R2
+
C2
C3
TR1
+
R6
C1
R5
R4
R3
MUX output
ground
ground
+15 V
MUX input
7Z78925

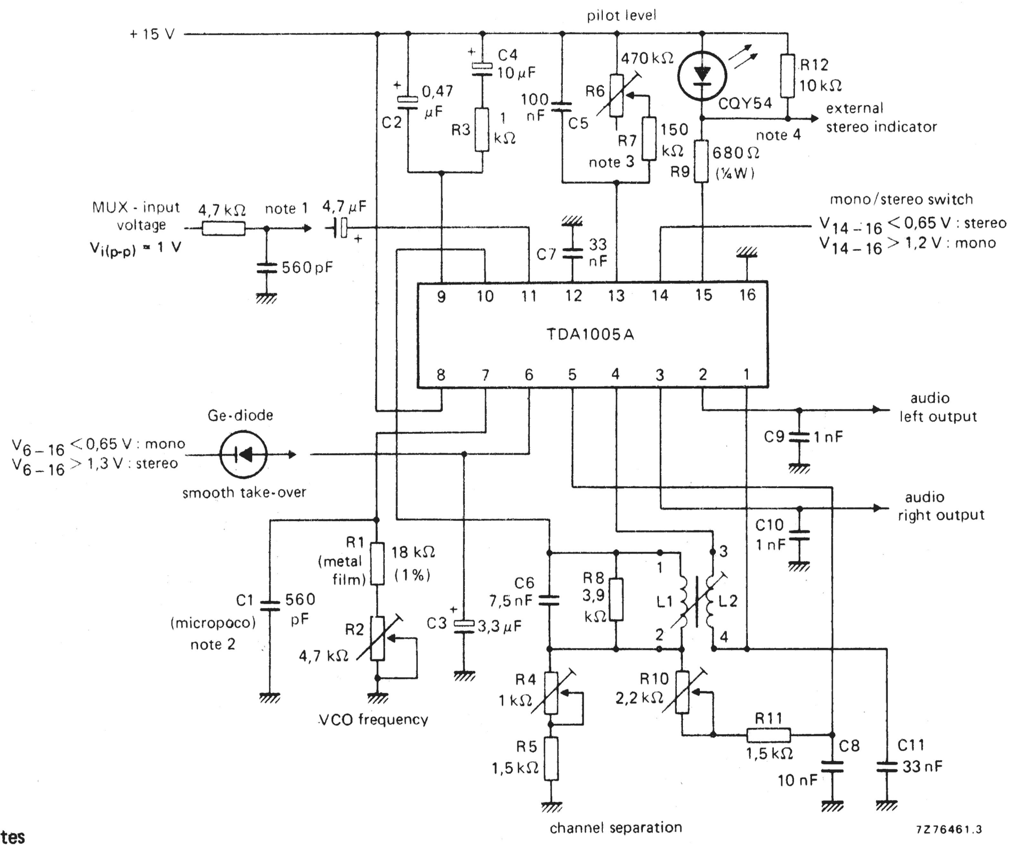
Fig. 4 Printed-circuit board component side, showing component layout.

Fig. 5 Printed-circuit board showing track side.


+ 15 V
BC547
MUX input
(1)
1,5 kΩ
33 nF
(2)
19 kHz notch filter
1
2
3
+
4,7 µF
$Z_i \approx 3{,}6$ kΩ
33 nF of Fig. 7 omitted
12
11
TDA1005A
23 mH (3)
1
2
6,8 nF
6,8 nF
10 kΩ
15 kΩ
3
7Z78940

(1) Transistor to achieve low impedance driving of notch filter.
(2) 33 nF will give common mode suppression of 19 kHz.
(3) Coil: TOKO 10 PA, 700 turns, ϕ0,07 mm Cu; case type: P06-0114; drumcore: AN01-0021; base 5 pins type: 07-0084-02; core type CAN02-0029.

Fig. 6 Example of using a 19 kHz tuned notch filter; for other input structures see Figs 13 to 21.


pilot level
+ 15 V
C4
10 μF
0,47 μF
C2
R3
1 kΩ
100 nF
C5
R6
470 kΩ
R7
150 kΩ
note 3
CQY54
R12
10 kΩ
external stereo indicator
note 4
680 Ω
R9
(¼W)
MUX - input voltage
$V_{i(p-p)} \approx 1$ V
4,7 kΩ
note 1
4,7 μF
560 pF
C7
33 nF
mono/stereo switch
$V_{14-16} < 0,65$ V : stereo
$V_{14-16} > 1,2$ V : mono
9 10 11 12 13 14 15 16
TDA1005A
8 7 6 5 4 3 2 1
audio left output
C9
1 nF
Ge-diode
$V_{6-16} < 0,65$ V : mono
$V_{6-16} > 1,3$ V : stereo
smooth take-over
audio right output
C10
1 nF
R1
(metal film)
18 kΩ
(1%)
C1
(micropoco)
note 2
560 pF
R2
4,7 kΩ
VCO frequency
C3
3,3 μF
C6
7,5 nF
R8
3,9 kΩ
1
2
3
4
L1
L2
R4
1 kΩ
R5
1,5 kΩ
R10
2,2 kΩ
R11
1,5 kΩ
C8
10 nF
C11
33 nF
channel separation
7Z76461.3

Coil data:

$L_1L_2 = 2,6$ mH

$Q_{1-2} = 35$; $Q_{min} \doteq 30$

$N_{1-2} = 357½$ turns;

$N_{3-4} = 297½$ turns:

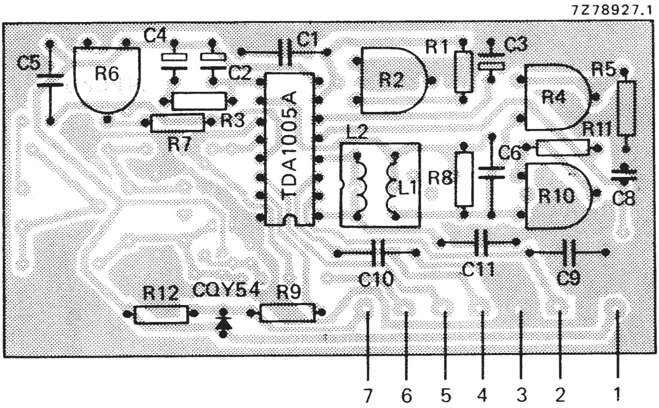
scrambled wound with wire diameter 0,09 mm,

$\frac{E_{3-4}}{E_{1-2}} \times 100\% = 82\%$

Notes

1. For other input structures see Figs 13 to 21; shown here is with RC-filter (Fig. 15).
2. The micropoco capacitor has a temperature coefficient of $125.10^{-6} \pm 60.10^{-6}$ K^{-1}.
3. In simplified circuits a fixed resistor (e.g. 620 kΩ) can be used for a guaranteed switching level of ⩽ 16 mV.
4. Either the LED circuit or an external stereo indicator can be used.

Fig. 7 Basic application circuit of a frequency-division multiplex (f.d.m.) stereo decoder.


7Z78927.1
C5
R6
C4
C2
C1
R3
R7
TDA1005A
R2
R1
C3
R5
R4
R11
L2
L1
R8
C6
R10
C8
C10
C11
C9
R12
CQY54
R9
7
6
5
4
3
2
1

1. Positive supply (+ 15 V).
2. Left output.
3. Ground.
4. Right output.
5. Mono/stereo switch.
6. MUX input.
7. External stereo indicator.

Fig. 8 Printed-circuit board component side of an f.d.m. decoder, showing component layout. For circuit diagram see Fig. 7.

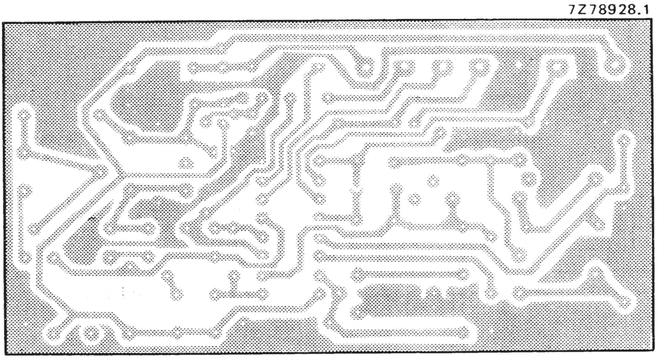
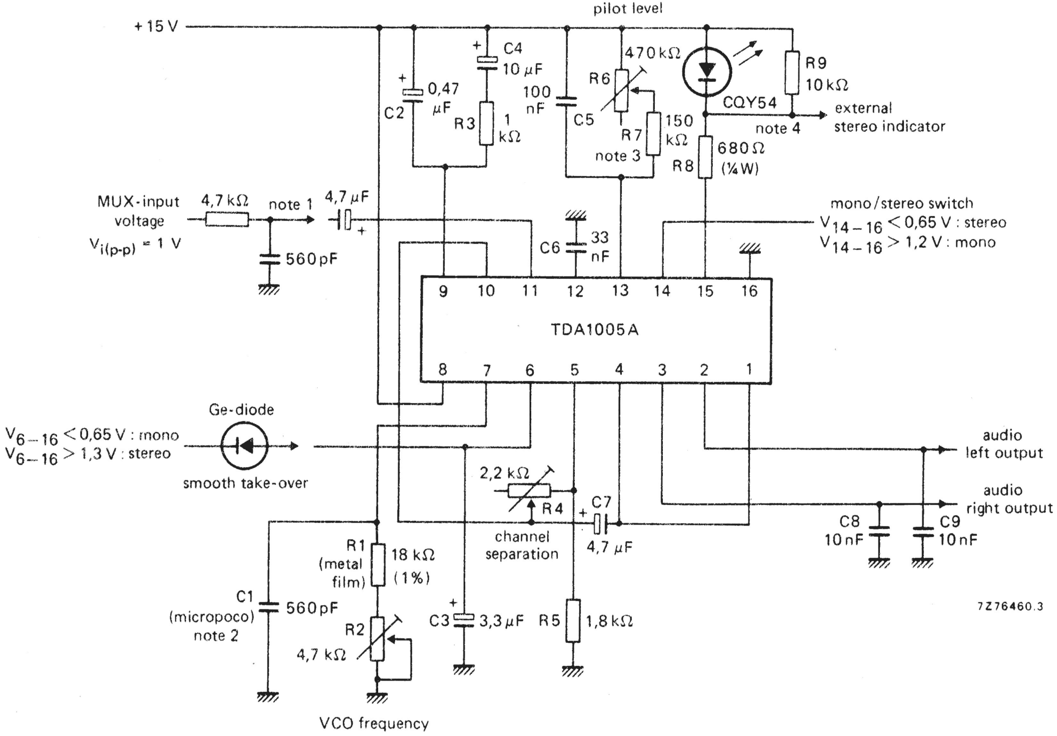
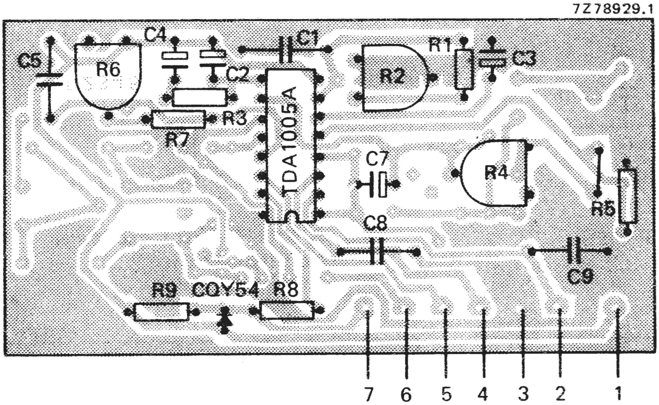


Fig. 9 Printed-circuit board showing track side.


+15 V
pilot level
C4
10 μF
C2
0,47 μF
R3
1 kΩ
100 nF
C5
470 kΩ
R6
R7
150 kΩ
note 3
CQY54
R9
10 kΩ
external stereo indicator
note 4
680 Ω
R8
(¼ W)
MUX-input voltage
$V_{i(p-p)} \approx 1$ V
4,7 kΩ
note 1
4,7 μF
560 pF
C6
33 nF
mono/stereo switch
$V_{14-16} < 0{,}65$ V : stereo
$V_{14-16} > 1{,}2$ V : mono
TDA1005A
9
10
11
12
13
14
15
16
8
7
6
5
4
3
2
1
Ge-diode
$V_{6-16} < 0{,}65$ V : mono
$V_{6-16} > 1{,}3$ V : stereo
smooth take-over
2,2 kΩ
R4
channel separation
C7
4,7 μF
audio left output
audio right output
C8
10 nF
C9
10 nF
R1
(metal film)
18 kΩ
(1%)
C1
(micropoco)
note 2
560 pF
R2
4,7 kΩ
VCO frequency
C3
3,3 μF
R5
1,8 kΩ
7Z76460.3

Notes
1. For other input structures see Figs 13 to 21; shown here is with RC-filter (Fig. 15).
2. The micropoco capacitor has a temperature coefficient of $125.10^{-6} \pm 60.10^{-6}$ $^{\circ}C^{-1}$.
3. In simplified circuits a fixed resistor (e.g. 620 kΩ) can be used for a guaranteed switching level of $\leqslant 16$ mV.
4. Either the LED circuit or an external stereo indicator can be used.

Fig. 10 Basic application circuit of a time-division multiplex (t.d.m.) stereo decoder.


7Z78929.1
C5
R6
C4
C2
C1
R2
R1
C3
R3
R7
TDA1005A
C7
R4
R5
C8
C9
R9
CQY54
R8
7
6
5
4
3
2
1

1. Positive supply (+ 15 V).
2. Left output.
3. Ground.
4. Right output.
5. Mono/stereo switch.
6. MUX input.
7. External stereo indicator.

Fig. 11 Printed-circuit board component side of a t.d.m. decoder, showing component layout. For circuit diagram see Fig. 10.

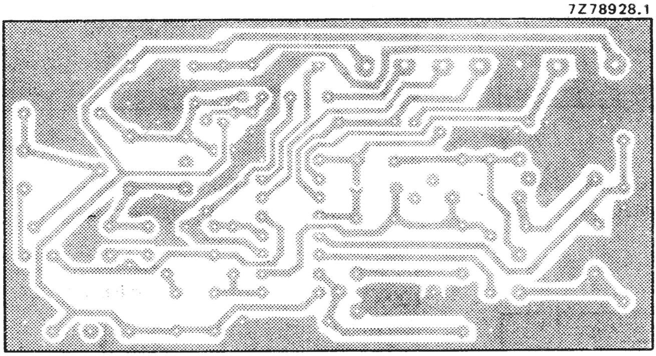


Fig. 12 Printed-circuit board showing track side.

INPUT STRUCTURES (see also Figs 7 and 10)

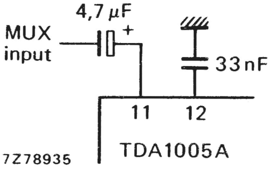

4,7 μF
+
MUX input
33 nF
11
12
TDA1005A
7Z78935

Fig. 13 Without filtering.

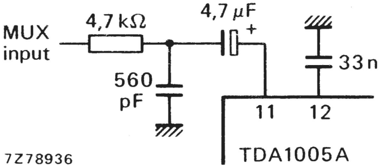

MUX input
4,7 kΩ
4,7 μF
+
560 pF
33 nF
11
12
TDA1005A
7Z78936

Fig. 15 With RC-filter for achieving i.f. roll-off (typ. 62 kHz).

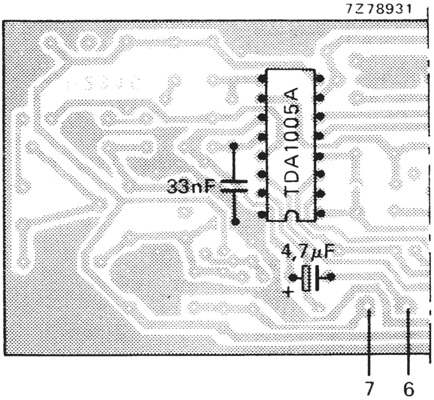

7Z78931
TDA1005A
33nF
4,7 μF
+
7
6

Fig. 14 Printed-circuit board component side, showing component layout of Fig. 13.

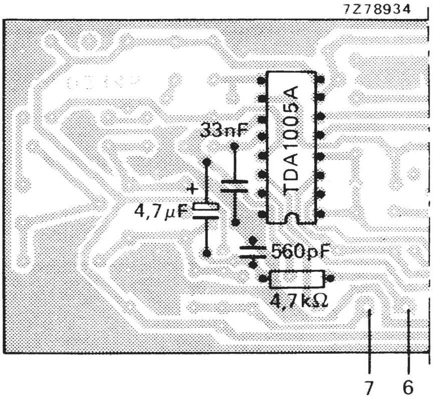

7Z78934
TDA1005A
33nF
+
4,7 μF
560pF
4,7kΩ
7
6

Fig. 16 Printed-circuit board component side, showing component layout of Fig. 15.

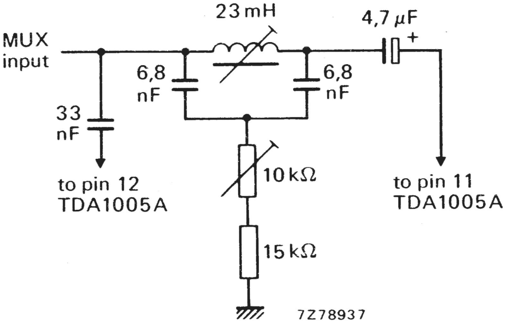

23 mH
4,7 μF
+
MUX input
6,8 nF
6,8 nF
33 nF
to pin 12 TDA1005A
10 kΩ
to pin 11 TDA1005A
15 kΩ
7Z78937

Fig. 17 With 19 kHz notch filter.

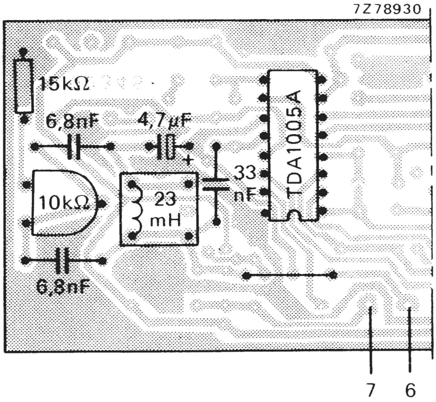

7Z78930
15kΩ
6,8nF
4,7 μF
+
33 nF
TDA1005A
10kΩ
23 mH
6,8nF
7
6

Fig. 18 Printed-circuit board component side, showing component layout of Fig. 17.

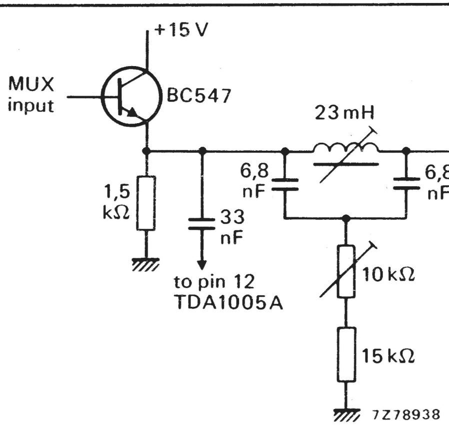

+15 V
MUX input
BC547
23 mH
4,7 μF
+
to pin 11 TDA1005A
6,8 nF
6,8 nF
1,5 kΩ
33 nF
to pin 12 TDA1005A
10 kΩ
15 kΩ
7Z78938

Fig. 19 With buffer stage (to achieve low impedance driving of notch filter; see Fig. 6) and 19 kHz notch filter.

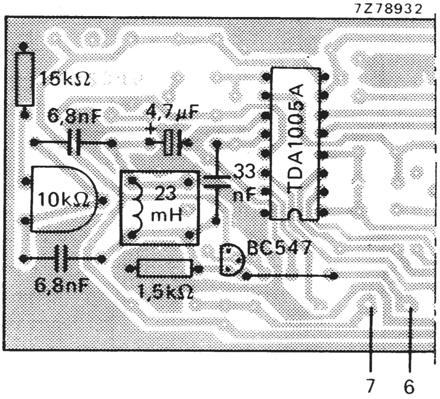

7Z78932
15kΩ
6,8nF
4,7μF
+
33 nF
TDA1005A
10kΩ
23 mH
BC547
6,8nF
1,5kΩ
7
6

Fig. 20 Printed-circuit board component side, showing component layout of Fig. 19.

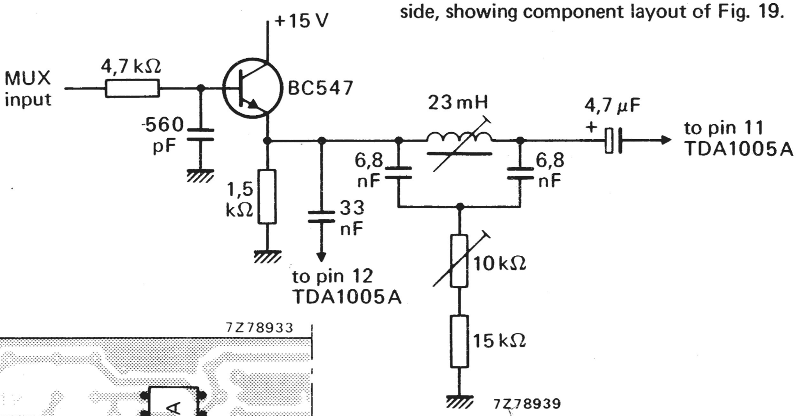

+15 V
MUX input
4,7 kΩ
BC547
560 pF
23 mH
4,7 μF
+
to pin 11 TDA1005A
6,8 nF
6,8 nF
1,5 kΩ
33 nF
to pin 12 TDA1005A
10 kΩ
15 kΩ
7Z78939

Fig. 21 With RC-filter, buffer stage and 19 kHz notch filter.

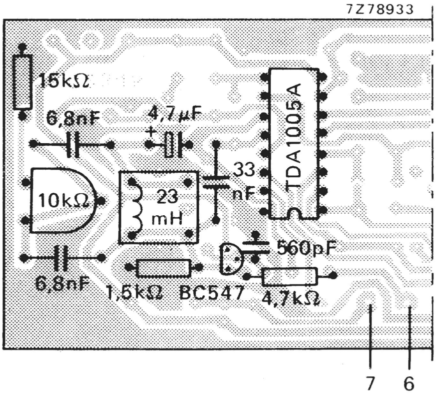
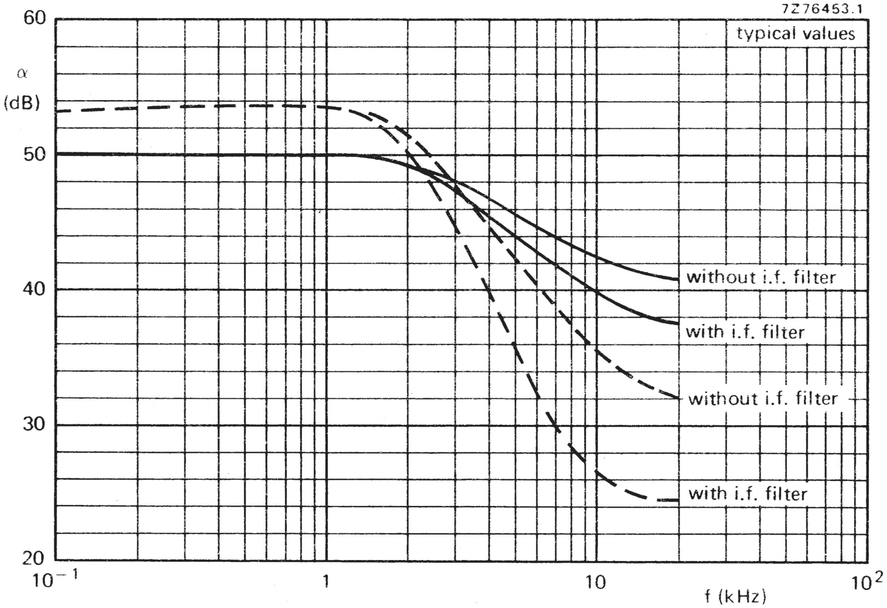
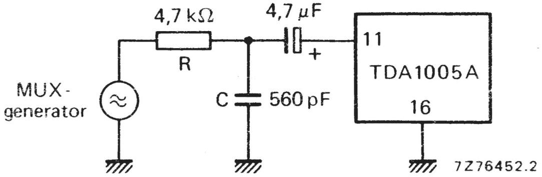

7Z78933
15kΩ
6,8nF
4,7μF
+
33 nF
TDA1005A
10kΩ
23 mH
560pF
6,8nF
1,5kΩ
BC547
4,7kΩ
7
6

Fig. 22 Printed-circuit board component side, showing component layout of Fig. 21.




4,7 kΩ
R
4,7 μF
+
MUX-
generator
C
560 pF
11
TDA1005A
16
7Z76452.2

—— time-division multiplex system; adjusted at 1 kHz (R4 in Fig. 10)

– – – frequency-division multiplex system; adjusted at 1 and 5 kHz (R4 and R10 in Fig. 7)

Conditions: $V_{8\text{-}16} = 15$ V; $V_{i(p\text{-}p)} = 1$ V.

Note: RC-filter for simulating the i.f. roll-off (typ. 62 kHz).

Fig. 23 Channel separation as a function of frequency.

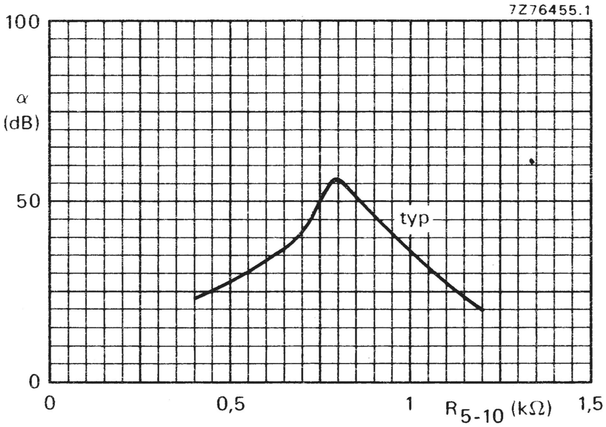


Fig. 24 Channel separation at f = 1 kHz as a function of resistance between pins 5 and 10 for a t.d.m. system. For test circuit see Fig. 23.

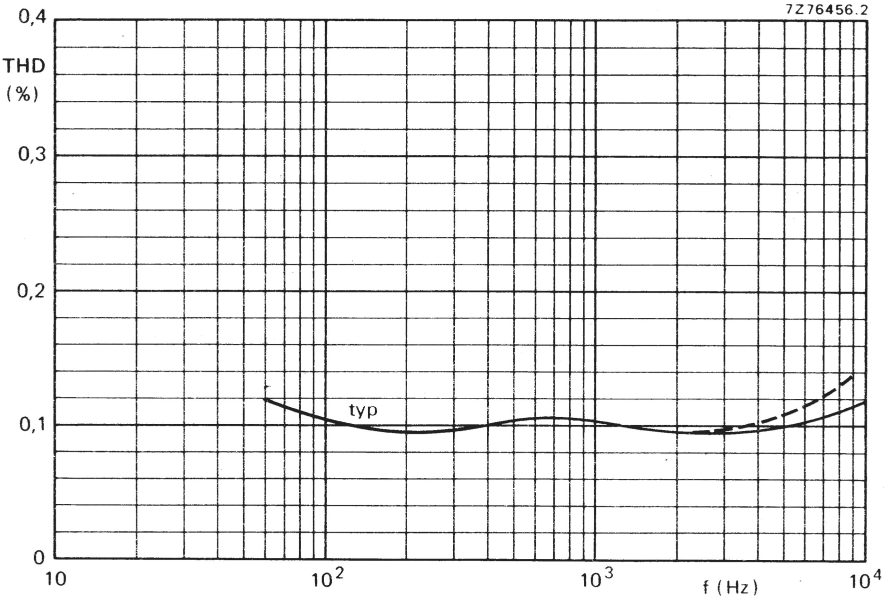
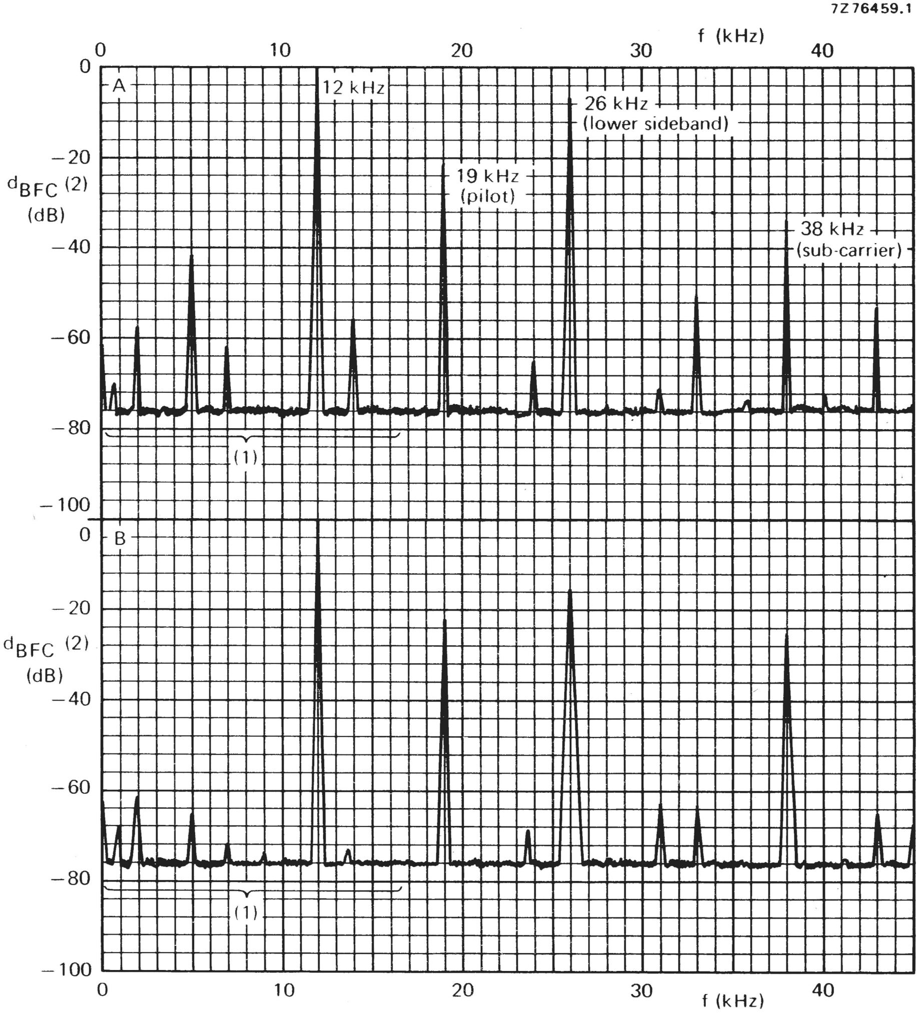


Fig. 25 Distortion as a function of audio frequency; R = 1; L = 0; $V_{8\text{-}16}$ = 15 V; $V_{2\text{-}16} = V_{3\text{-}16}$ = 1 V (r.m.s.). — — — t.d.m. system; ——— f.d.m. system.



(1) Audible interferences (BFC-distortion) and desired 12 kHz signal.

(2) $d_{BFC} = 20 \log \frac{V_{BFC}}{V\text{ (at 12 kHz)}}$.

Fig. 26 Spectrum at the decoder outputs; A for t.d.m.; B for f.d.m. $V_{i(p-p)} = 1$ V; R = 1; L = 0; m = 90% for f = 12 kHz; m = 10% for f = 19 kHz.

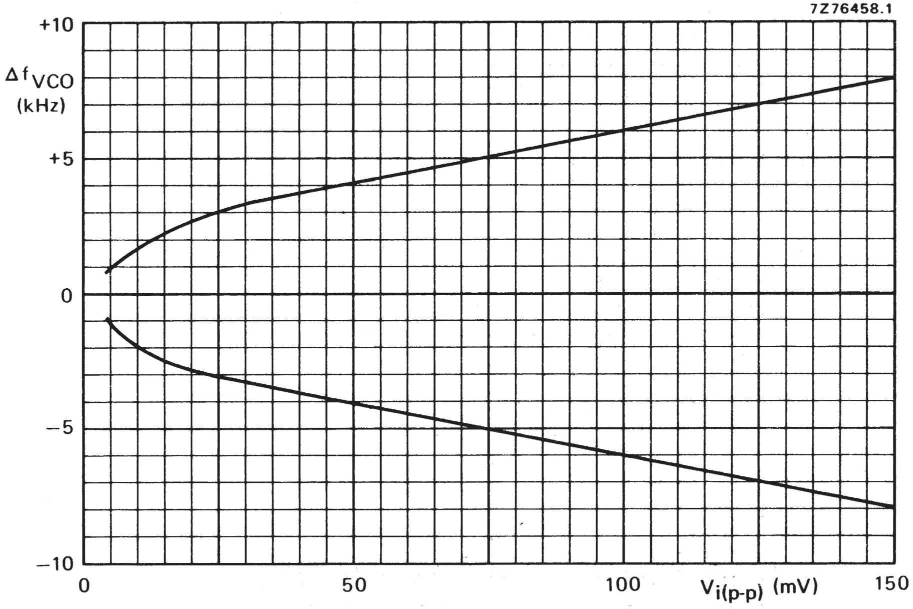


Fig. 27 Typical values of the capture range of the oscillator as a function of the pilot threshold voltage at MUX-input.
V_{8-16} = 15 V; $\Delta f_{VCO} = f_{VCO} - 76$ kHz where: f_{VCO} = modulated, free-running oscillator frequency; Δf_{VCO} = maximum f_{VCO} deviation which will be captured if pilot signal (pin 11) is switched-on.

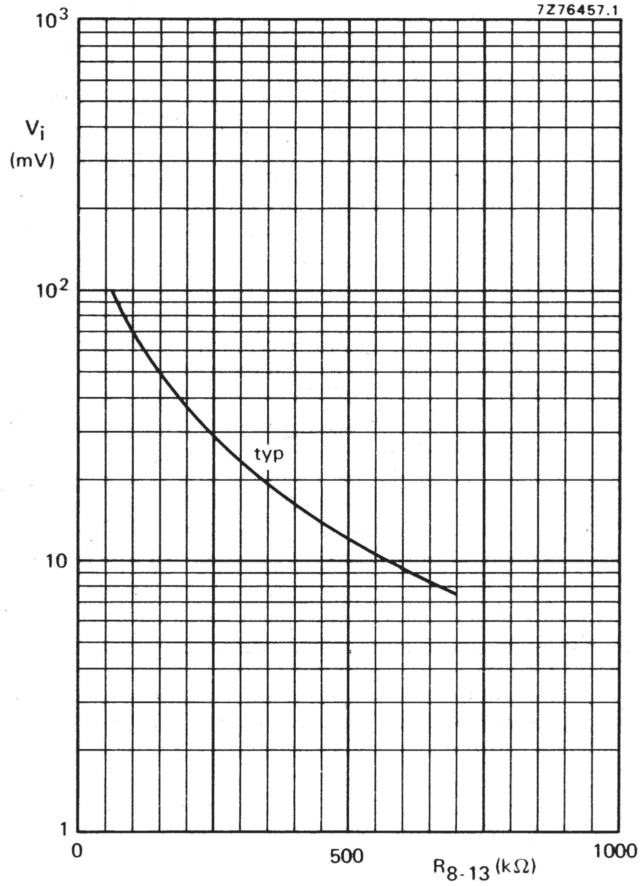


Fig. 28 Pilot input voltage switching level (stereo 'on') as a function of resistance between pins 8 and 13.

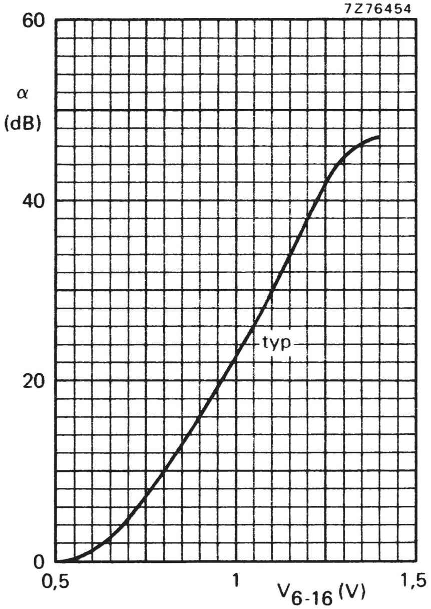


Fig. 29 Channel separation as a function of $V_{6\text{-}16}$ at 1 kHz (smooth take-over).

MOTOR REGULATOR WITH AUTOMATIC TAPE-END INDICATOR

The TDA1006A is for use in car radio tape-decks

The circuit incorporates the following functions:
- capstan motor speed control;
- an electronic motor stop in conjunction with hysteresis slip-coupling or commutator pulses;
- an automatic switch from playback to radio at tape-end;
- playback indication with lamp;
- tape-end indication with intermittent light.

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 22	V
Ambient temperature	T_{amb}	typ.	25	°C
Supply voltage	V_P	typ.	14	V
Motor regulator				
Current consumption ($R_{3\text{-}4}$ = 7,5 kΩ)				
radio	I_4	typ.	9	mA
playback ($I_1 = 0$)	I_4	typ.	12	mA
playback	I_4	typ.	52	mA
tape-end	I_4	typ.	32	mA
Operating motor current	I_3	typ.	200	mA
Supply voltage rejection	$\Delta V_{3\text{-}2}/\Delta V_{4\text{-}2}$	typ.	1	mV/V
Automatic stop circuit				
Input current	I_{14}	>	25	μA
Input voltage at commutator	$V_{11\text{-}2}$		−6 to +6	V

PACKAGE OUTLINE

16-lead DIL; plastic power (SOT-38BE-2).

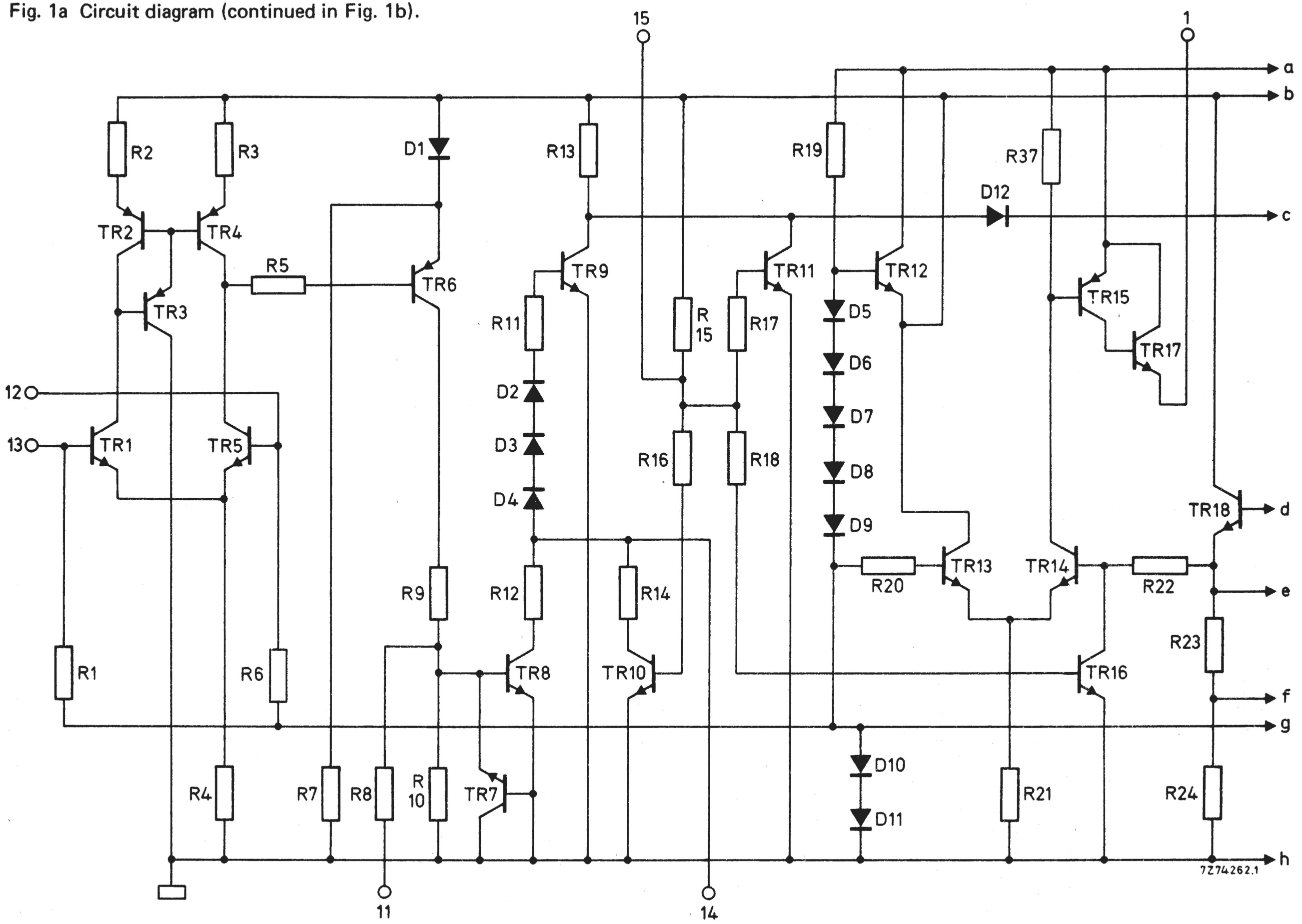

15
1
a
b
c
d
e
f
g
h
12
13
11
14
R1
R2
R3
R4
R5
R6
R7
R8
R9
R 10
R11
R12
R13
R14
R 15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R37
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
TR9
TR10
TR11
TR12
TR13
TR14
TR15
TR16
TR17
TR18
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
7Z74262.1

Fig. 1a Circuit diagram (continued in Fig. 1b).

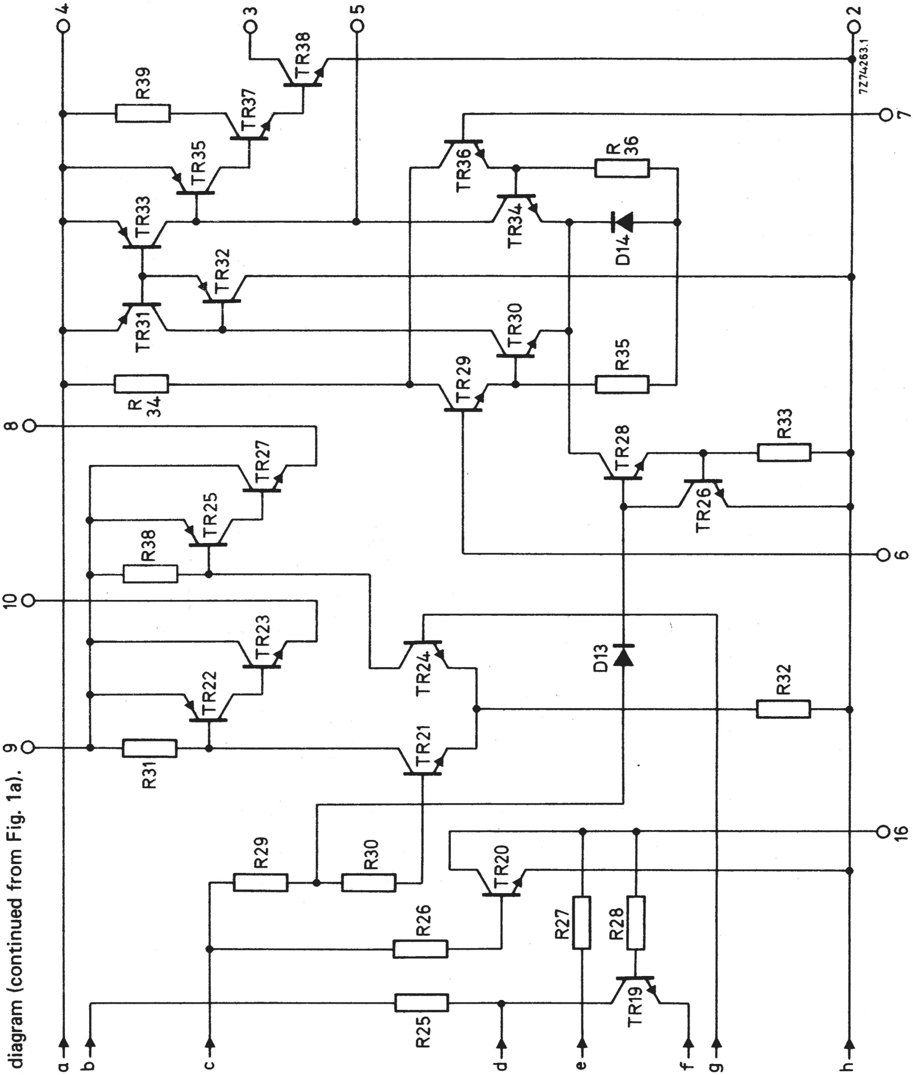

4
3
5
2
7Z74263.1
7
6
16
8
10
9
a
b
c
d
e
f
g
h
TR19
TR20
TR21
TR22
TR23
TR24
TR25
TR26
TR27
TR28
TR29
TR30
TR31
TR32
TR33
TR34
TR35
TR36
TR37
TR38
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R38
R39
D13
D14

Fig. 1b Circuit diagram (continued from Fig. 1a).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage				
pin 4	$V_{4\text{-}2}$	max.	24	V
pin 9	$V_{9\text{-}2}$	max.	24	V
	$V_{4\text{-}2}$	$\geqslant$	$V_{9\text{-}2}$	
Output current				
pin 1 (d.c. value)	$-I_1$	max.	40	mA
(peak value)	$-I_{1M}$	max.	100	mA
pin 3 (d.c. value)	I_3	max.	250	mA
(non-repetitive peak value)	I_{3SM}	max.	600	mA
pin 8 (d.c. value)	$-I_8$	max.	45	mA
(peak value)	$-I_{8M}$	max.	80	mA
pin 10 (d.c. value)	$-I_{10}$	max.	20	mA
(peak value)	$-I_{10M}$	max.	20	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature see power derating curve Fig. 2	T_{amb}		−25 to +150	°C

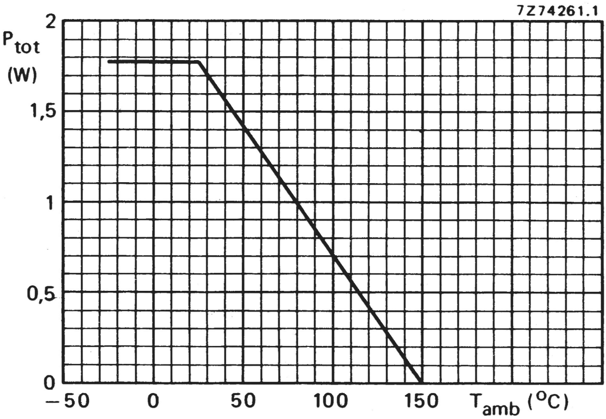


Fig. 2 Power derating curve; derating factor: 14,3 mW/°C.

CHARACTERISTICS

V_P = 14 V; T_{amb} = 25 °C unless otherwise specified (see test circuit Fig. 3).

Supply voltage range (pins 4 and 9)	V_P		6 to 22	V
	$V_{4\text{-}2}$	$\geqslant$	$V_{9\text{-}2}$	
Motor regulator				
Current consumption ($R_{3\text{-}4}$ = 7,5 kΩ)				
radio	I_4	typ.	9	mA
playback (I_1 = 0)	I_4	typ.	12	mA
			9,5 to 17	mA
playback	I_4	typ.	52	mA
tape-end	I_4	typ.	32	mA
Input offset voltage at I_3 = 3 mA	$\lvert V_{7\text{-}6}\rvert$	typ.	2	mV
		$<$	8	mV
Input voltage range (common mode)	$V_{6\text{-}2}$; $V_{7\text{-}2}$		2,4 to V_P–0,2	V
Input bias current	I_6; I_7	typ.	80	nA
		$<$	700	nA
Input sensitivity (for ΔI_3 = 100 mA)	$\Delta V_{7\text{-}6}$	$<$	13	mV
Operating voltage of TR38 at I_{3SM} = 600 mA	$V_{3\text{-}2}$	typ.	900	mV
		$<$	1800	mV
Supply voltage rejection	$\Delta V_{3\text{-}2}/\Delta V_{4\text{-}2}$	typ.	1	mV/V
Operating motor current	I_3	typ.	200	mA
		$<$	250	mA
Automatic motor 'stop' circuit				
Input current	I_{14}	$>$	25	μA
Voltage when TR20 is not conducting (pin 16; peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$		0,9 to 1,4	V
Voltage when TR20 is conducting (pin 16)	$V_{16\text{-}2}$	$<$	250	mV
Input voltage at commutator (pin 11)	$V_{11\text{-}2}$		–6 to +6	V
Stop signal amplifier				
Differential input voltage	$V_{12\text{-}13}$	typ.	3,5	mV
			2,6 to 4,4	mV
Voltage without input signal	$V_{11\text{-}2}$		85 to 170	mV
Input voltage (r.m.s. value)	$V_{12\text{-}13(rms)}$	$>$	10	mV

CHARACTERISTICS (continued)

Radio and preamplifier supply

Radio supply current (d.c.)	$-I_8$	$\leqslant$	45	mA
Saturation voltage at $-I_{8M} = 80$ mA	$V_{8\text{-}9}$	$\leqslant$	1,35	V
Preamplifier supply current (d.c.)	$-I_{10}$	$\leqslant$	20	mA
Saturation voltage at $-I_{10} = 20$ mA	$V_{10\text{-}9}$	$\leqslant$	1,2	V

Lamp driver

Output current (d.c.)	$-I_1$	$\leqslant$	40	mA
Saturation voltage at $-I_{1M} = 100$ mA	$V_{4\text{-}1}$	$\leqslant$	1,85	V
D.C. voltage level	$V_{15\text{-}2}$	0,75 to	1,2	V

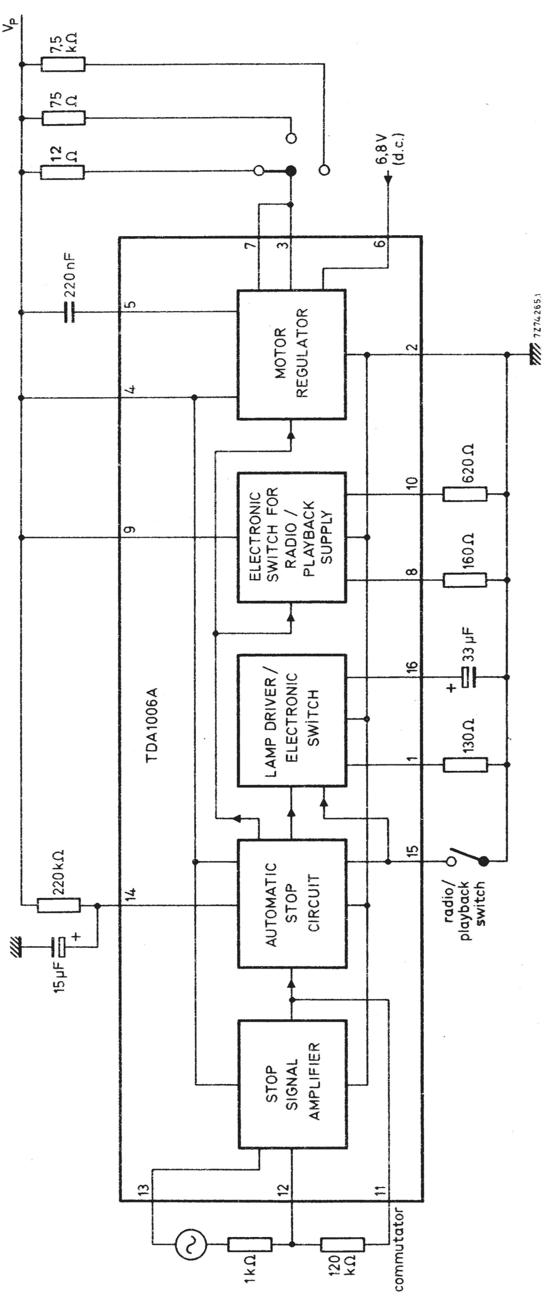
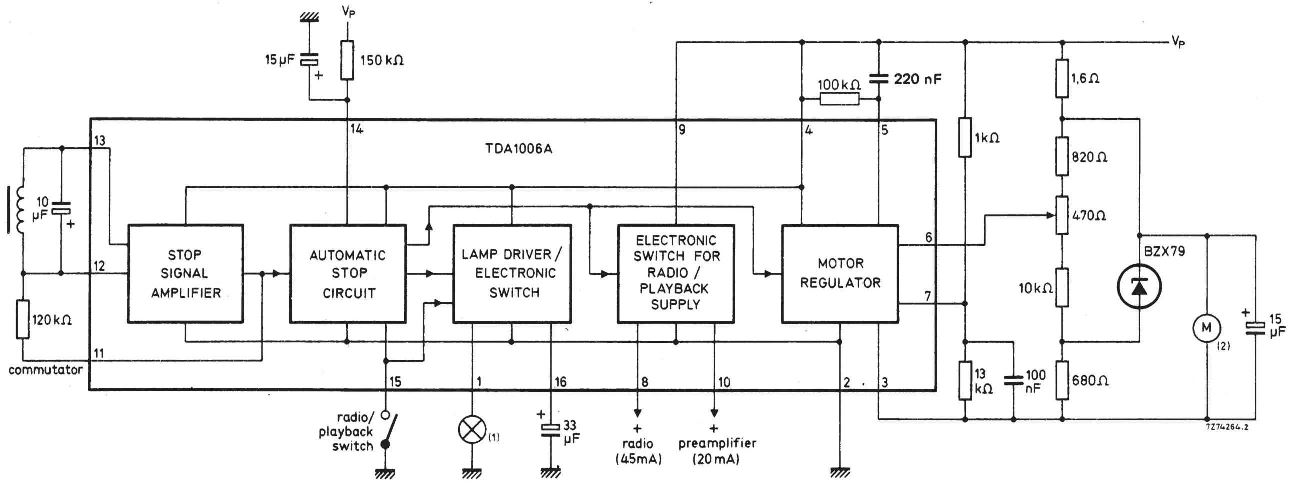

V_P
7,5 kΩ
75 Ω
12 Ω
6,8 V (d.c.)
220 nF
7
3
6
5
4
2
MOTOR REGULATOR
7Z74265.1
ELECTRONIC SWITCH FOR RADIO / PLAYBACK SUPPLY
10
9
8
620 Ω
160 Ω
LAMP DRIVER / ELECTRONIC SWITCH
16
1
+
33 µF
130 Ω
TDA1006A
AUTOMATIC STOP CIRCUIT
15
14
220 kΩ
+
15 µF
radio/ playback switch
STOP SIGNAL AMPLIFIER
13
12
11
1 kΩ
120 kΩ
commutator

Fig. 3 Test circuit.

APPLICATION INFORMATION


VP
15 µF
+
150 kΩ
100 kΩ
220 nF
1 kΩ
1,6 Ω
820 Ω
470 Ω
10 kΩ
680 Ω
BZX79
M
(2)
15 µF
13 kΩ
100 nF
TDA1006A
13
12
11
14
9
4
5
6
7
15
1
16
8
10
2
3
10 µF
120 kΩ
commutator
STOP SIGNAL AMPLIFIER
AUTOMATIC STOP CIRCUIT
LAMP DRIVER / ELECTRONIC SWITCH
ELECTRONIC SWITCH FOR RADIO / PLAYBACK SUPPLY
MOTOR REGULATOR
radio/ playback switch
(1)
33 µF
+ radio (45mA)
+ preamplifier (20 mA)
7Z74264.2

(1) Radio: lamp off
Playback: lamp on
Tape-end: intermittent light

(2) D.C. motor
$E_{3000} = 7,2$ to $8,3$ V
$R_m = 27\ \Omega$

Fig. 4 Application circuit diagram.

GATING/FREQUENCY DIVIDER FOR ELECTRONIC MUSICAL INSTRUMENTS

The TDA1008 is a monolithic bipolar integrated circuit based on I^2L (integrated injection logic), with frequency dividers directly coupled to the gating system.

The outputs of the dividers, together with the input signal, are applied internally to nine gate inputs. By activating a key input, five successive signals out of the nine are selected and transferred to the outputs. Five key inputs are available, each selecting a different combination; e.g. 16', 8', 4', 2' and 1'. The output signal level is proportional to the voltage applied to the key inputs. By connecting RC combinations to the key inputs, sustain of the output signal is easily obtained. The duration of the sustained signal can be adjusted by connecting a variable voltage to the appropriate terminal (pin 7).

In electronic organs using a top octave synthesizer directly coupled to twelve TDA1008 circuits, only one busbar per manual is needed to obtain five octave-related tones per key.

The tone output signals are symmetrical around a fixed d.c. voltage, thereby avoiding key clicks.

QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_{P1\text{-}16}$	typ.	12	V
Supply voltage divider (pin 13)	$V_{P13\text{-}16}$	typ.	6	V
Supply voltage tone outputs (pins 2, 3, 4, 5, 6)	V_{Ptone}	typ.	9	V
Input voltage; HIGH	V_{IH}	>	1,5	V
Input voltage; LOW	V_{IL}	<	0,4	V
Required key voltage (pins 8, 9, 10, 11, 12)	V_{K1} to V_{K5}	typ.	$V_{P13\text{-}16}$	
Key input impedance (see note)	Z_{K1} to Z_{K5}	>	8	MΩ
Supply current (pin 1)				
all keys activated	I_1	typ.	13	mA
no activated keys	I_1	typ.	0	mA
Supply current (pin 13)	I_{13}	typ.	11	mA
Sustaining voltage range (pin 7)	V_{7sust}		0 to 2	V
Input frequency	f_i	<	100	kHz
Tone output signal voltage with one key activated	$V_{Q(p\text{-}p)}$	typ.	600	mV
Operating ambient temperature range	T_{amb}		0 to + 70	°C

Note

Key input impedance is determined by the voltage applied to pin 7. This impedance is stated at zero volt on pin 7.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

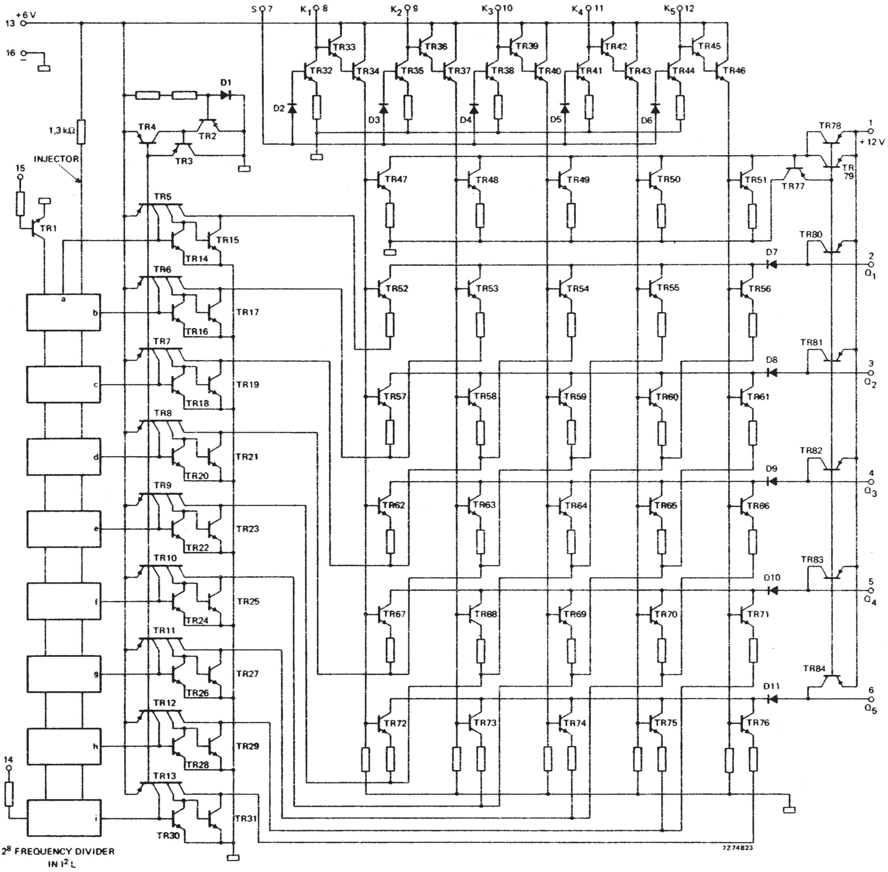

+6 V
13
16
S 7
K1 8
K2 9
K3 10
K4 11
K5 12
1
+12 V
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
TR9
TR10
TR11
TR12
TR13
TR14
TR15
TR16
TR17
TR18
TR19
TR20
TR21
TR22
TR23
TR24
TR25
TR26
TR27
TR28
TR29
TR30
TR31
TR32
TR33
TR34
TR35
TR36
TR37
TR38
TR39
TR40
TR41
TR42
TR43
TR44
TR45
TR46
TR47
TR48
TR49
TR50
TR51
TR52
TR53
TR54
TR55
TR56
TR57
TR58
TR59
TR60
TR61
TR62
TR63
TR64
TR65
TR66
TR67
TR68
TR69
TR70
TR71
TR72
TR73
TR74
TR75
TR76
TR77
TR78
TR79
TR80
TR81
TR82
TR83
TR84
1,3 kΩ
INJECTOR
15
14
a
b
c
d
e
f
g
h
i
2
Q1
3
Q2
4
Q3
5
Q4
6
Q5
2⁸ FREQUENCY DIVIDER
IN I²L
7Z74823

Fig. 1 Circuit diagram.

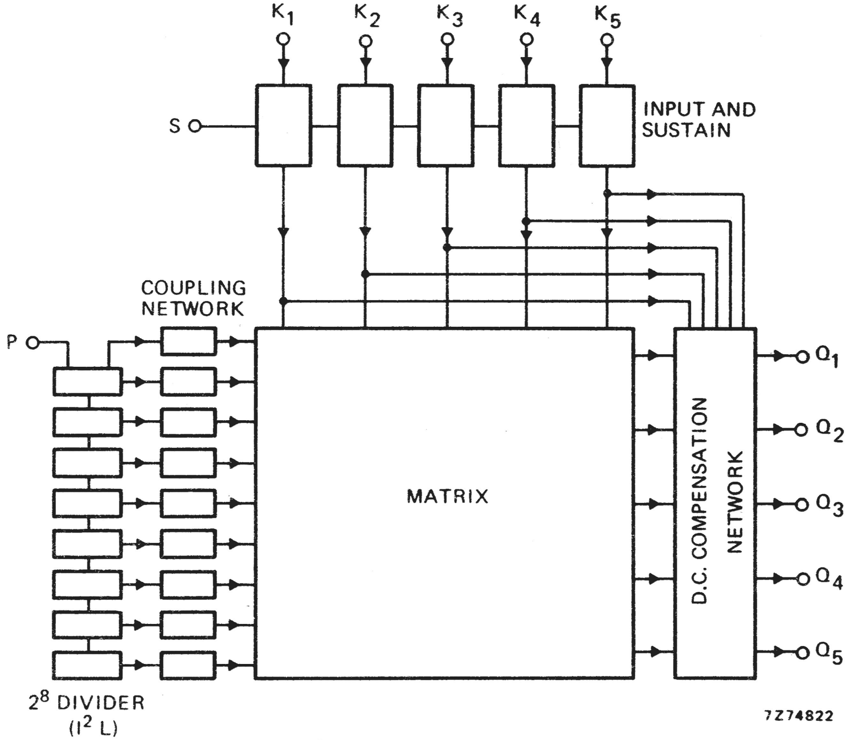

K1
K2
K3
K4
K5
S
INPUT AND SUSTAIN
COUPLING NETWORK
P
MATRIX
D.C. COMPENSATION NETWORK
Q1
Q2
Q3
Q4
Q5
2⁸ DIVIDER (I² L)
7Z74822

Fig. 2 Block diagram.

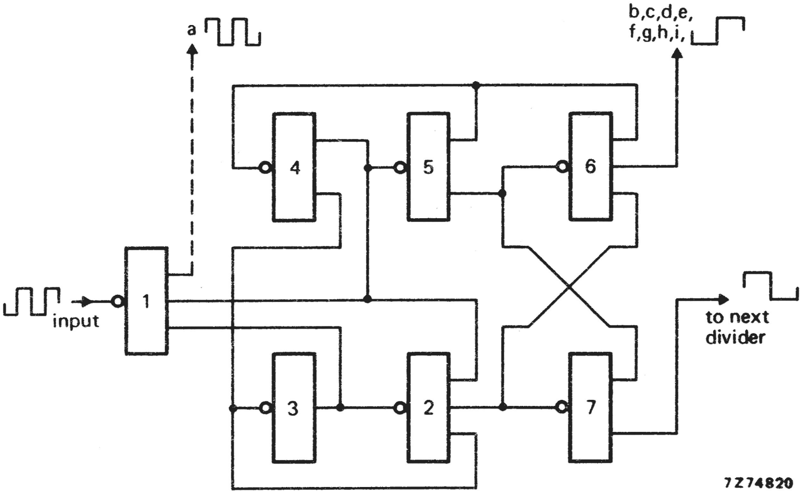

a
b,c,d,e, f,g,h,i,
input
1
2
3
4
5
6
7
to next divider
7Z74820

Fig. 3 Logic diagram of the I^2L 2-divider.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages				
pin 1	$V_{P1\text{-}16}$	max.	13	V
pin 13	$V_{P13\text{-}16}$	max.	6,5	V
pin 14	$V_{P14\text{-}16}$	max.	6,5	V
Input voltages				
K inputs (pins 8, 9, 10, 11, 12)	V_{K1} to V_{K5}	max.	$V_{P13\text{-}16}$	
f_i input (pin 15)	V_{fi}	max.	15	V
S input (pin 7)	V_S	max.	2,5	V
Output voltages				
Q_1 to Q_5 (pins 2, 3, 4, 5, 6)	V_{Q1} to V_{Q5}	max.	12	V
Operating ambient temperature	see derating curve Fig. 4			
Storage temperature	T_{stg}		−25 to + 125	°C
Total power dissipation	see derating curve Fig. 4			

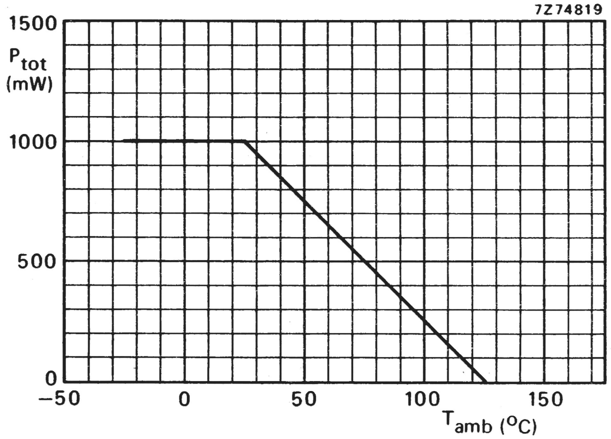


Fig. 4 Power derating curve.

CHARACTERISTICS

All voltages with reference to pin 16; all currents positive into the IC.

Supply voltage range				
pin 13	$V_{P13\text{-}16}$		5 to 6,5	V
pin 1	$V_{P1\text{-}16}$		10 to 13	V
pin 9	$V_{P9\text{-}16}$	see note 1		

Characteristics at T_{amb} = 25 °C; $V_{P13\text{-}16}$ = 6 V; $V_{P1\text{-}16}$ = 12 V; see Fig. 6.

Supply current (pin 13) K-inputs at 6 V	I_{13}		7,5 to 16	mA
		typ.	11	mA
Supply current (pin 1) K-inputs at 6 V	I_1		8 to 16	mA
		typ.	12,7	mA
Input current at f_i (pin 15) V_{fi} = 6 V	I_{15}		100 to 200	µA
		typ.	150	µA
Input current K-inputs (pins 8, 9, 10, 11, 12) V_K = 6 V S-input connected to 0 V	I_K	typ.	150	nA
		$<$	750	nA
S-input connected to 2,0 V	I_K		80 to 150	µA
		typ.	100	µA
Input current S-input (pin 7)				
no key inputs activated	I_S	typ.	500	µA
all key inputs activated	I_S	typ.	10	µA
Output current Q-output (pins 2, 3, 4, 5, 6) V_Q = LOW (note 2)	$+I_Q$		230 to 450	µA
		typ.	300	µA
V_Q = HIGH (note 2)	$-I_Q$		230 to 450	µA
		typ.	300	µA
Output current pin 14	I_{14}	$<$	20	µA
Peak output voltage (pins 2, 3, 4, 5, 6) by activating one K-input only (Fig. 5)	V_{QM}	typ.	300	mV
Input frequency at pin 15 $V_{15HIGH} > 1{,}5$ V; $V_{15LOW} < 0{,}4$ V	f_i	$<$	100	kHz

Notes
1. This voltage has to be in the middle of $V_{P1\text{-}16}$ and $V_{13\text{-}16}$.
2. To be multiplied by the number of activated K-inputs.

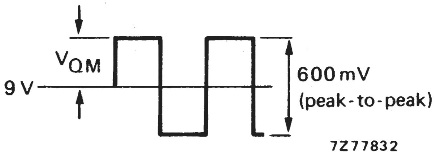


Fig. 5

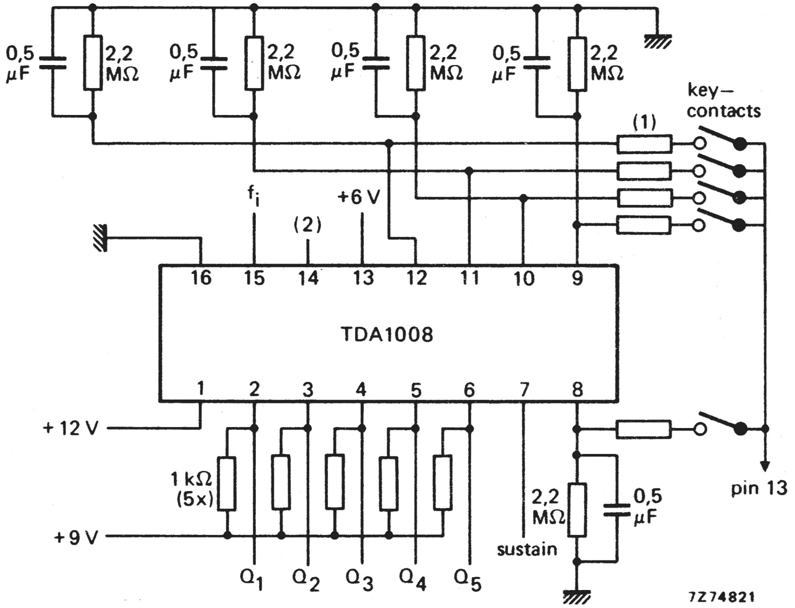
TRUTH TABLE

	K_1	K_2	K_3	K_4	K_5
Q_1	f_i	$f_i/2$	$f_i/4$	$f_i/8$	$f_i/16$
Q_2	$f_i/2$	$f_i/4$	$f_i/8$	$f_i/16$	$f_i/32$
Q_3	$f_i/4$	$f_i/8$	$f_i/16$	$f_i/32$	$f_i/64$
Q_4	$f_i/8$	$f_i/16$	$f_i/32$	$f_i/64$	$f_i/128$
Q_5	$f_i/16$	$f_i/32$	$f_i/64$	$f_i/128$	$f_i/256$

Activating 'one' key input only gives the notified output frequency.

By activating more key inputs at a time, the output amplitude will be the sum signal of the notified frequencies.

APPLICATION INFORMATION


0,5 µF
2,2 MΩ
0,5 µF
2,2 MΩ
0,5 µF
2,2 MΩ
0,5 µF
2,2 MΩ
key–contacts
(1)
f_i
+6 V
(2)
16
15
14
13
12
11
10
9
TDA1008
1
2
3
4
5
6
7
8
+ 12 V
1 kΩ (5x)
+9 V
Q_1
Q_2
Q_3
Q_4
Q_5
2,2 MΩ
sustain
0,5 µF
pin 13
7Z74821

(1) If required contact-current limiting resistors.

(2) a. Factory test point; ungated output from the final divider.

b. Can be used for obtaining very low frequencies (pedals). It should be connected to pin 13 (+ 6 V) via a resistor of minimum 300 kΩ to deliver the current I_{14}.

Fig. 6 Basic application diagram.

6 W AUDIO POWER AMPLIFIER IN CAR APPLICATIONS
10 W AUDIO POWER AMPLIFIER IN MAINS-FED APPLICATIONS

The TDA1010A is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a 6 W car radio amplifier for use with 4 Ω and 2 Ω load impedances. The wide supply voltage range and the flexibility of the IC make it an attractive proposition for record players and tape recorders with output powers up to 10 W.

Special features are:
- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- low-cost external components
- good ripple rejection
- thermal protection

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 24	V
Repetitive peak output current	I_{ORM}	max.	3	A
Output power at pin 2; d_{tot} = 10%				
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	6,4	W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6,2	W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,4	W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	typ.	30	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20	kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31	mA
Sensitivity for P_o = 5,8 W; R_L = 4 Ω	V_i	typ.	10	mV
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

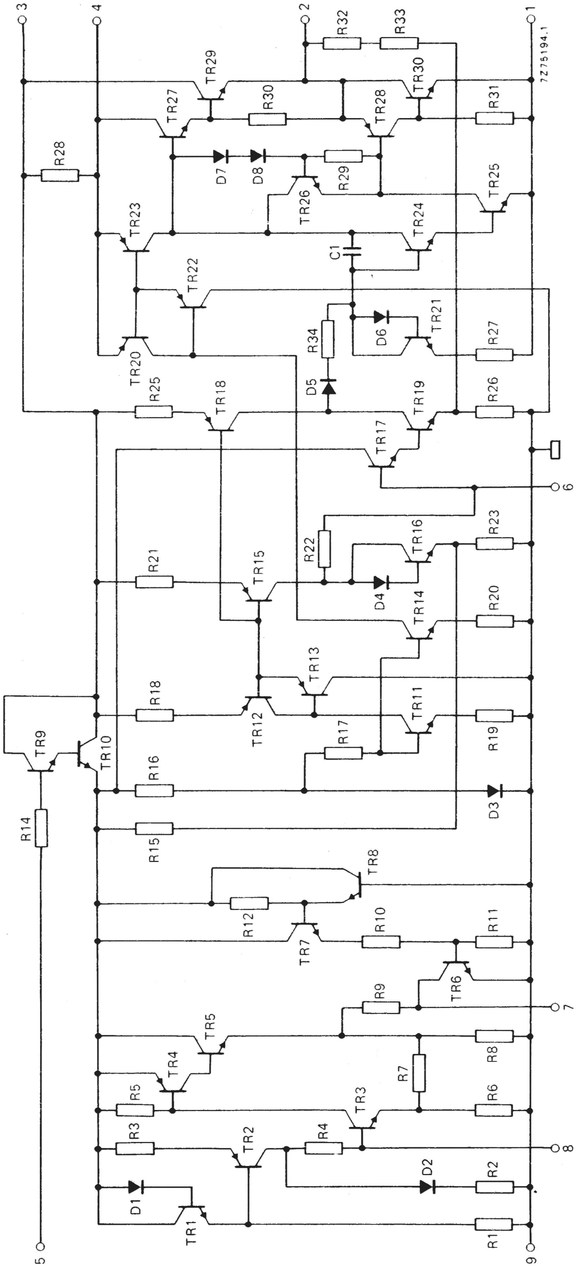

3
4
2
1
5
9
6
7
8
7Z75194.1
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
TR9
TR10
TR11
TR12
TR13
TR14
TR15
TR16
TR17
TR18
TR19
TR20
TR21
TR22
TR23
TR24
TR25
TR26
TR27
TR28
TR29
TR30
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
D1
D2
D3
D4
D5
D6
D7
D8
C1

Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24	V
Peak output current	I_{OM}	max.	5	A
Repetitive peak output current	I_{ORM}	max.	3	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature	T_{amb}	−25 to + 150		°C
A.C. short-circuit duration of load during sine-wave drive; without heatsink at V_P = 14,4 V	t_{sc}	max.	100	hours

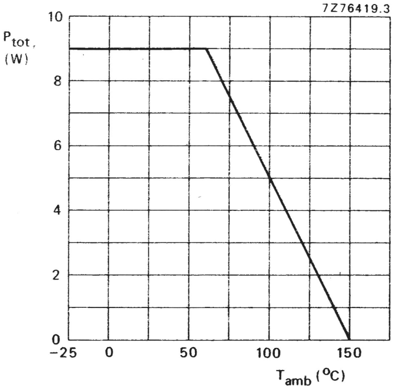


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 14,4 V; R_L = 2 Ω; T_{amb} = 60 °C maximum; thermal shut-down starts at T_j = 150 °C. The maximum sine-wave dissipation in a 2 Ω load is about 5,2 W. The maximum dissipation for music drive will be about 75% of the worst-case sine-wave dissipation, so this will be 3,9 W. Consequently, the total resistance from junction to ambient

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{150 - 60}{3{,}9} = 23\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 10 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W,

$$R_{th\ h\text{-}a} = 23 - (10 + 1) = 12\ \text{K/W}.$$

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 24	V
Repetitive peak output current	I_{ORM}	$<$	3	A
Total quiescent current at $V_P = 14{,}4$ V	I_{tot}	typ.	31	mA

A.C. CHARACTERISTICS

$T_{amb} = 25$ °C; $V_P = 14{,}4$ V; $R_L = 4\ \Omega$; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power (see Fig. 4) at $d_{tot} = 10\%$; measured at pin 2; with bootstrap				
$V_P = 14{,}4$ V; $R_L = 2\ \Omega$ (note 1)	P_o	typ.	6,4	W
$V_P = 14{,}4$ V; $R_L = 4\ \Omega$ (note 1 and 2)	P_o	$>$ typ.	5,9 6,2	W W
$V_P = 14{,}4$ V; $R_L = 8\ \Omega$ (note 1)	P_o	typ.	3,4	W
$V_P = 14{,}4$ V; $R_L = 4\ \Omega$; without bootstrap	P_o	typ.	5,7	W
$V_P = 14{,}4$ V; $R_L = 2\ \Omega$; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9	W
Voltage gain				
preamplifier (note 3)	G_{v1}	typ.	24 21 to 27	dB dB
power amplifier	G_{v2}	typ.	30 27 to 33	dB dB
total amplifier	$G_{v\,tot}$	typ.	54 51 to 57	dB dB
Total harmonic distortion at $P_o = 1$ W	d_{tot}	typ.	0,2	%
Efficiency at $P_o = 6$ W	η	typ.	75	%
Frequency response (–3 dB)	B		80 Hz to 15	kHz
Input impedance				
preamplifier (note 4)	$\|Z_i\|$	typ.	30 20 to 40	kΩ kΩ
power amplifier (note 5)	$\|Z_i\|$	typ.	20 14 to 26	kΩ kΩ
Output impedance of preamplifier; pin 7 (note 5)	$\|Z_o\|$	typ.	20 14 to 26	kΩ kΩ
Output voltage preamplifier (r.m.s. value) $d_{tot} < 1\%$ (pin 7) (note 3)	$V_{o(rms)}$	$>$	0,7	V
Noise output voltage (r.m.s. value; note 6)				
$R_S = 0\ \Omega$	$V_{n(rms)}$	typ.	0,3	mV
$R_S = 8{,}2$ kΩ	$V_{n(rms)}$	typ. $<$	0,7 1,4	mV mV
Ripple rejection at f = 1 kHz to 10 kHz (note 7)	RR	$>$	42	dB
at f = 100 Hz; C2 = 1 μF	RR	$>$	37	dB
Sensitivity for $P_o = 5{,}8$ W	V_i	typ.	10	mV
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ.	30	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Up to $P_o \leqslant 3$ W : $d_{tot} \leqslant 1\%$.
3. Measured with a load impedance of 20 kΩ.
4. Independent of load impedance of preamplifier.
5. Output impedance of preamplifier ($|Z_o|$) is correlated (within 10%) with the input impedance ($|Z_i|$) of the power amplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The tab must be electrically floating or connected to the substrate (pin 9).

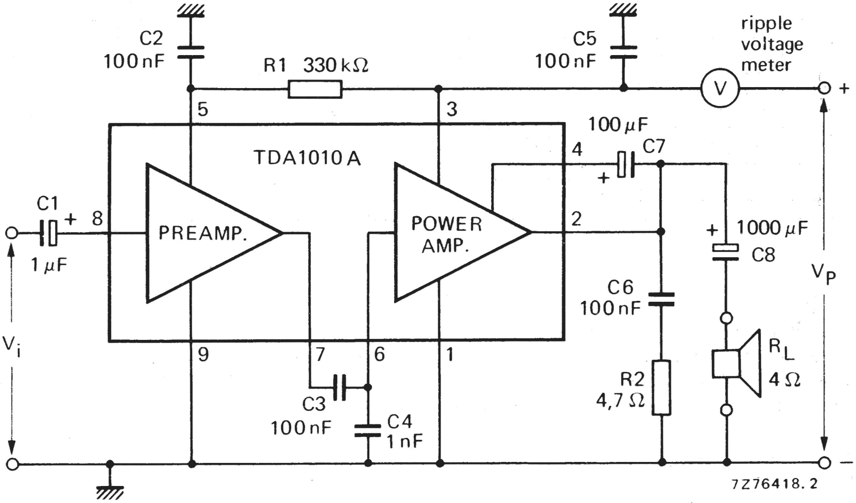

C2
100 nF
R1 330 kΩ
C5
100 nF
ripple
voltage
meter
V
+
5
3
TDA1010 A
100 μF
4
C7
+
C1
+
8
PREAMP.
POWER
AMP.
2
+
1000 μF
C8
1 μF
C6
100 nF
V_P
V_i
9
7
6
1
R_L
4 Ω
C3
100 nF
C4
1 nF
R2
4,7 Ω
–
7Z76418.2

Fig. 3 Test circuit.

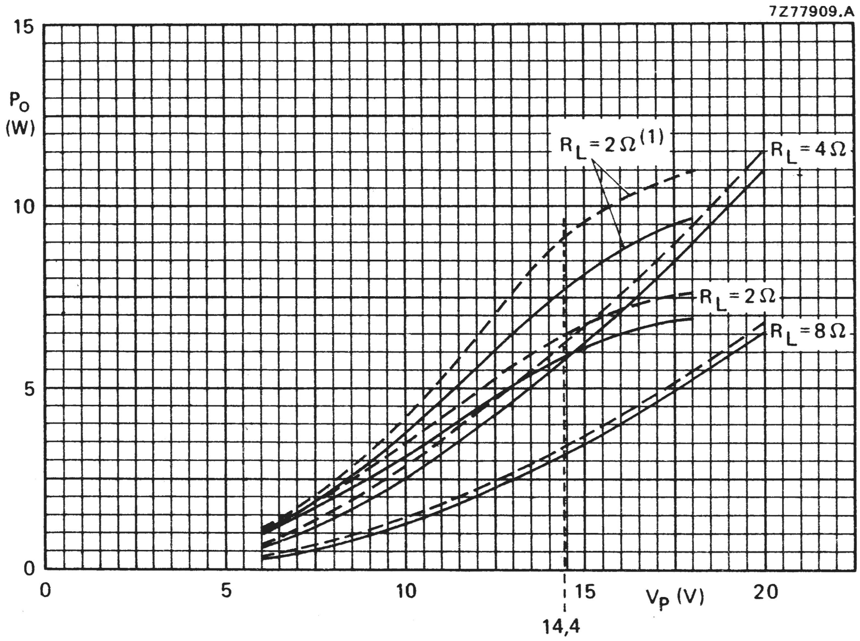


Fig. 4 Output power of the circuit of Fig. 3 as a function of the supply voltage with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega^{(1)}$ has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, d_{tot} = 10%, T_{amb} = 25 °C.

Fig. 5 See next page.
Total harmonic distortion in the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\,\Omega^{(1)}$ has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, V_P = 14,4 V.

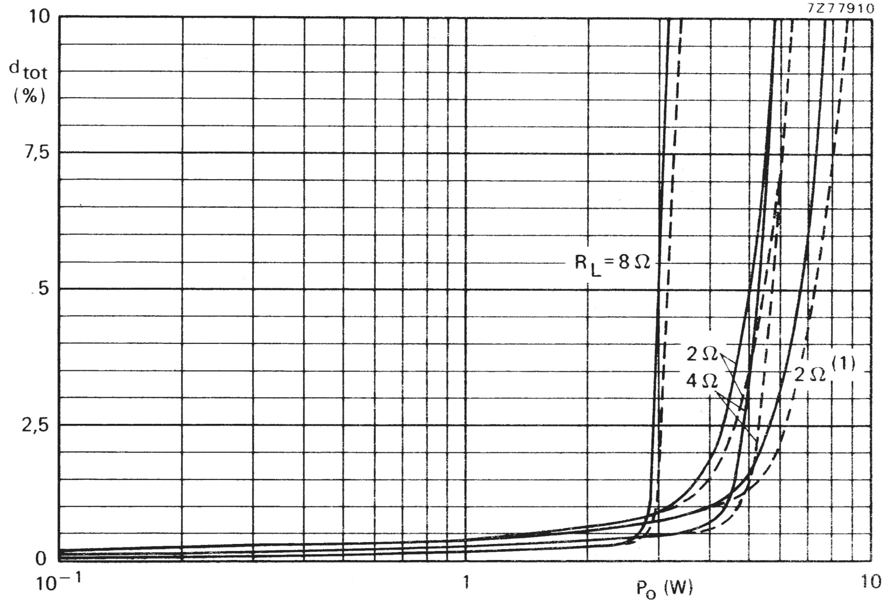


Fig. 5 For caption see page 6.

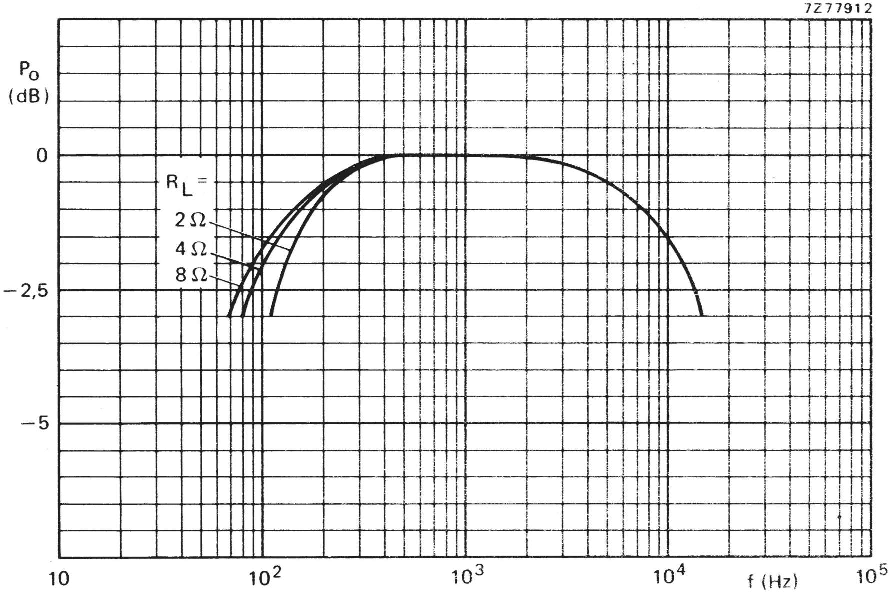


Fig. 6 Frequency characteristics of the circuit of Fig. 3 for three values of load impedance; typical values. P_o relative to 0 dB = 1 W; V_P = 14,4 V.

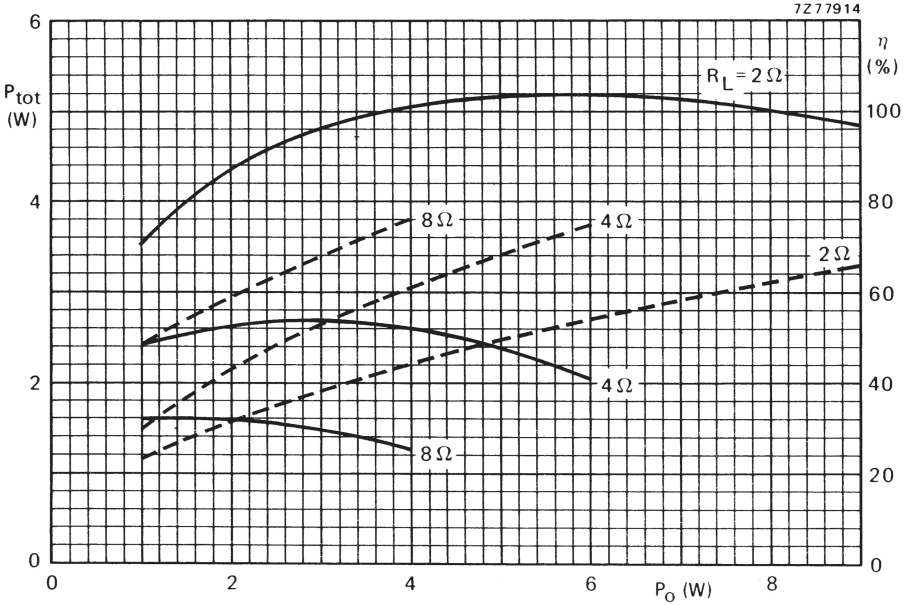


Fig. 7 Total power dissipation (solid lines) and the efficiency (dashed lines) of the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter (for R_L = 2 Ω an external bootstrap resistor of 220 Ω has been used); typical values. V_P = 14,4 V; f = 1 kHz.

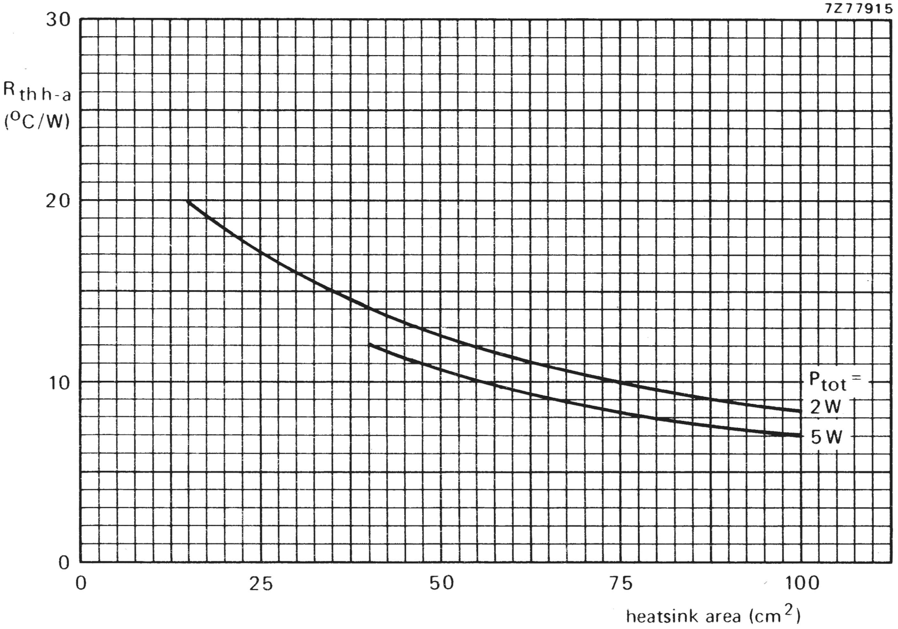


Fig. 8 Thermal resistance from heatsink to ambient of a 1,5 mm thick bright aluminium heatsink as a function of the single-sided area of the heatsink with the total power dissipation as a parameter.

APPLICATION INFORMATION

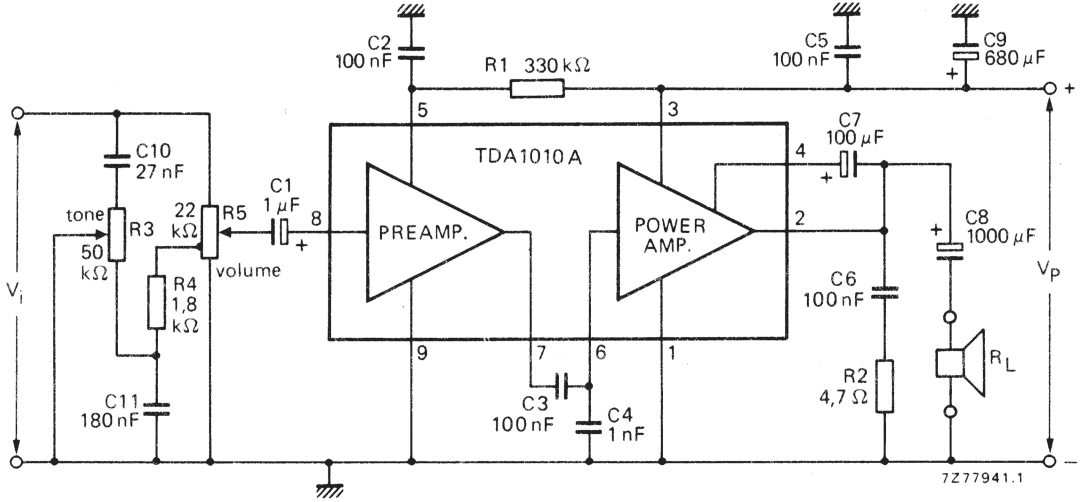

C2
100 nF
R1 330 kΩ
C5
100 nF
C9
680 µF
+
5
3
TDA1010A
4
C7
100 µF
+
C10
27 nF
tone
R3
50
kΩ
22
kΩ
R5
volume
C1
1 µF
+
8
PREAMP.
POWER
AMP.
2
C8
1000 µF
+
R4
1,8
kΩ
V_i
C6
100 nF
V_P
9
7
6
1
R_L
C11
180 nF
C3
100 nF
C4
1 nF
R2
4,7 Ω
+
−
7Z77941.1

Fig. 9 Complete mono audio amplifier of a car radio.

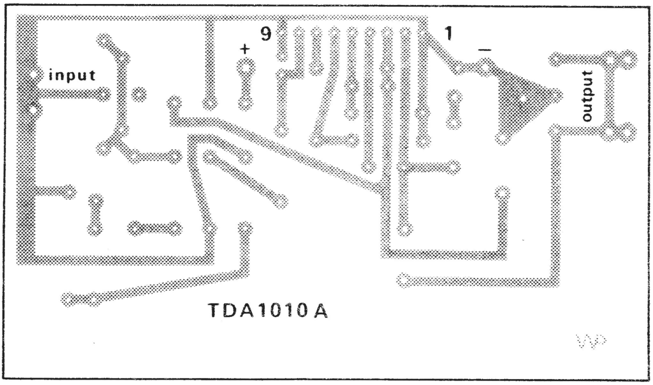

9
+
1
–
input
output
TDA1010 A
7Z77931

Fig. 10 Track side of printed-circuit board used for the circuit of Fig. 9; p.c. board dimensions 92 mm x 52 mm.

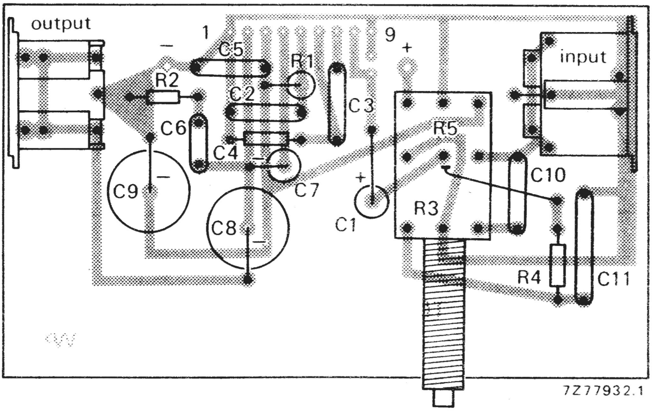

output
1
–
C5
R1
9
+
input
R2
C2
C3
C6
R5
C4
C10
C9
C7
+
C1
R3
C8
R4
C11
7Z77932.1

Fig. 11 Component side of printed-circuit board showing component layout used for the circuit of Fig. 9.

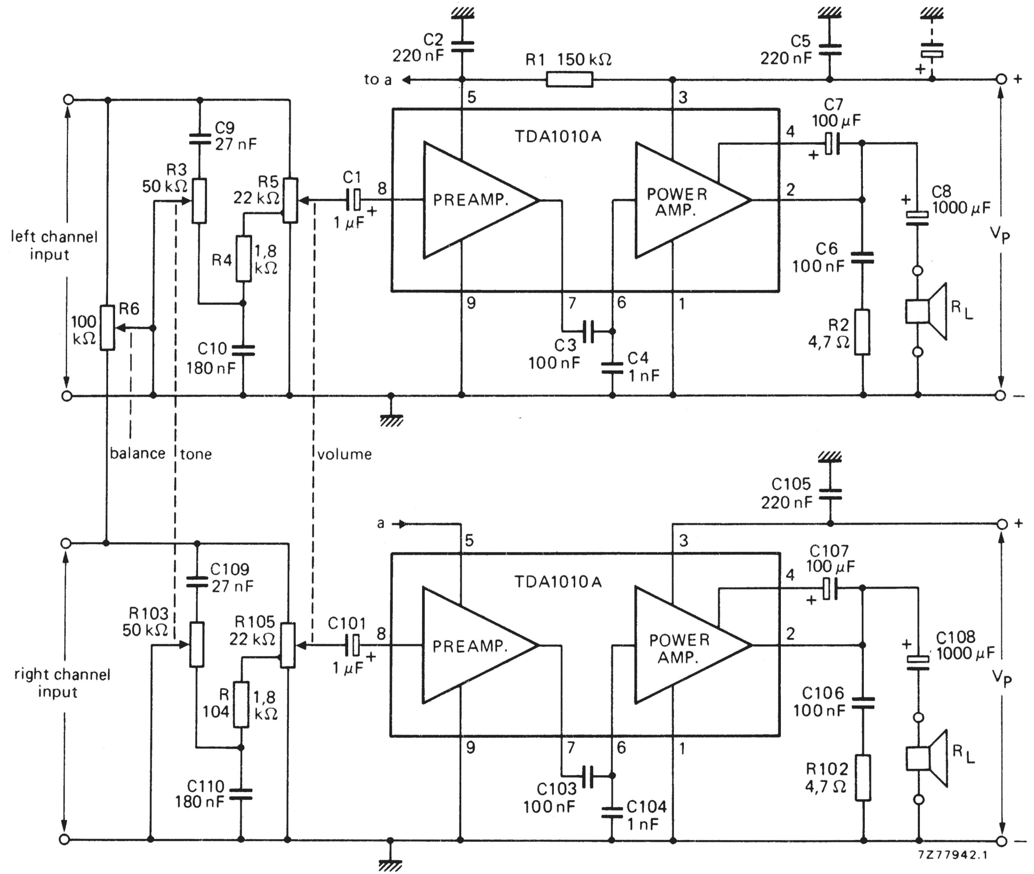

C2
220 nF
R1 150 kΩ
C5
220 nF
to a
+
5
3
TDA1010A
C7
100 µF
4
+
C9
27 nF
R3
50 kΩ
R5
22 kΩ
C1
1 µF
+
8
PREAMP.
POWER
AMP.
2
C8
1000 µF
+
left channel
input
R4
1,8
kΩ
C6
100 nF
VP
R6
100
kΩ
9
7
6
1
RL
C10
180 nF
C3
100 nF
C4
1 nF
R2
4,7 Ω
–
balance
tone
volume
C105
220 nF
a
+
5
3
TDA1010A
C107
100 µF
4
+
C109
27 nF
R103
50 kΩ
R105
22 kΩ
C101
1 µF
+
8
PREAMP.
POWER
AMP.
2
C108
1000 µF
+
right channel
input
R
104
1,8
kΩ
C106
100 nF
VP
9
7
6
1
RL
C110
180 nF
C103
100 nF
C104
1 nF
R102
4,7 Ω
–
7Z77942.1

Fig. 12 Complete stereo car radio amplifier.

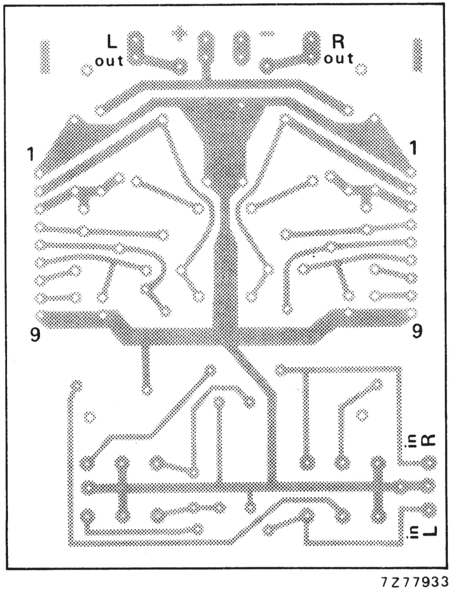

L
out
R
out
1
1
9
9
in
R
in
L
7Z77933

Fig. 13 Track side of printed-circuit board used for the circuit of Fig. 12; p.c. board dimensions 83 mm x 65 mm.

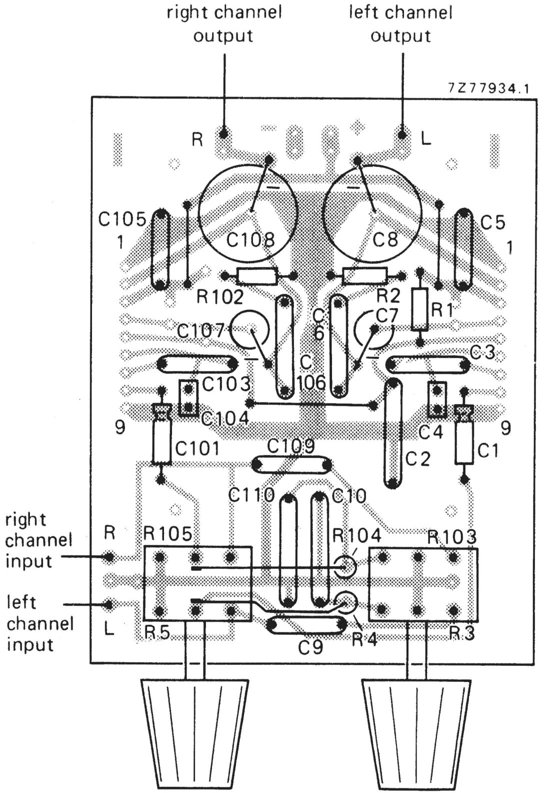

right channel
output
left channel
output
7Z77934.1
R
L
C105
1
C108
C8
C5
1
R102
R2
R1
C107
C
6
C7
C3
C
106
C103
C104
9
C101
C109
C4
C2
C1
9
C110
C10
right
channel
input
left
channel
input
R
L
R105
R104
R103
R5
C9
R4
R3

Fig. 14 Component side of printed-circuit board showing component layout used for the circuit of Fig. 12. Balance control is not on the p.c. board.

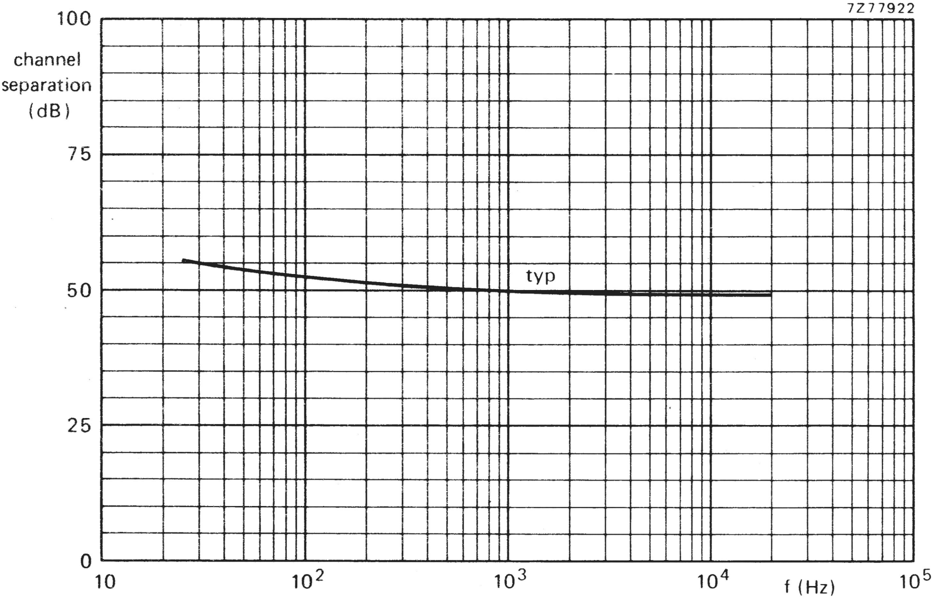


Fig. 15 Channel separation of the circuit of Fig. 12 as a function of the frequency.

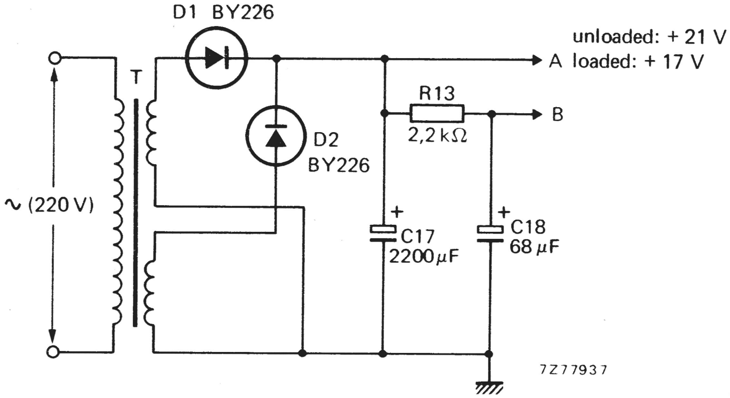

D1 BY226
unloaded: + 21 V
A loaded: + 17 V
T
R13
B
D2
BY226
2,2 kΩ
∼ (220 V)
+
C17
2200 μF
+
C18
68 μF
7Z77937

Fig. 16 Power supply of circuit of Fig. 17.

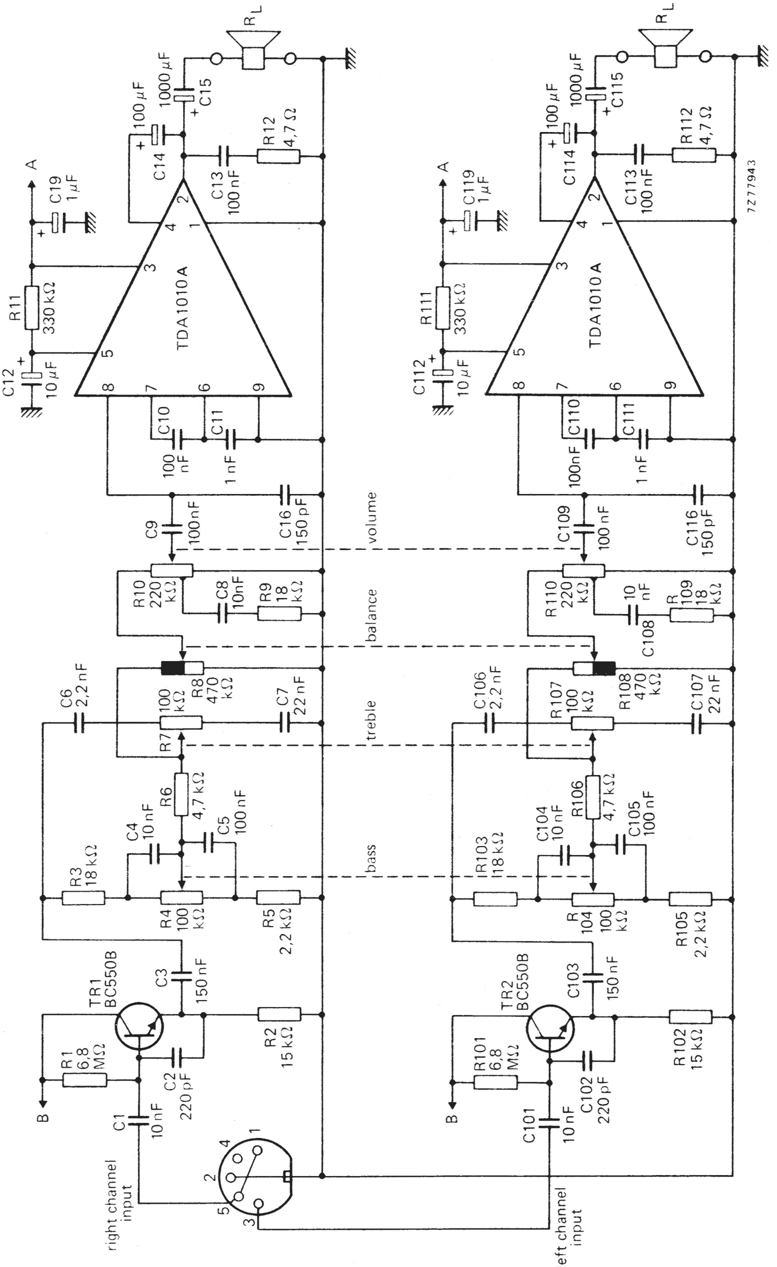

R11
330 kΩ
C12
10 µF
C19
1 µF
A
B
TDA1010A
C14
100 µF
C15
1000 µF
R12
4,7 Ω
C13
100 nF
R_L
C10
100 nF
C11
1 nF
C9
100 nF
C16
150 pF
volume
balance
treble
bass
R10
220 kΩ
C8
10nF
R9
18 kΩ
R8
470 kΩ
R7
100 kΩ
C6
2,2 nF
C7
22 nF
R6
4,7 kΩ
C4
10 nF
C5
100 nF
R3
18 kΩ
R4
100 kΩ
R5
2,2 kΩ
C3
150 nF
TR1
BC550B
R1
6,8 MΩ
C2
220 pF
R2
15 kΩ
C1
10 nF
right channel input
left channel input
R111
330 kΩ
C112
10 µF
C119
1 µF
C114
100 µF
C115
1000 µF
R112
4,7 Ω
C113
100 nF
C110
100nF
C111
1 nF
C109
100 nF
C116
150 pF
R110
220 kΩ
C108
10 nF
R109
18 kΩ
R108
470 kΩ
R107
100 kΩ
C106
2,2 nF
C107
22 nF
R106
4,7 kΩ
C104
10 nF
C105
100 nF
R103
18 kΩ
R104
100 kΩ
R105
2,2 kΩ
C103
150 nF
TR2
BC550B
R101
6,8 MΩ
C102
220 pF
R102
15 kΩ
C101
10 nF
7Z77943

Fig. 17 Complete mains-fed ceramic stereo pick-up amplifier; for power supply see Fig. 16.

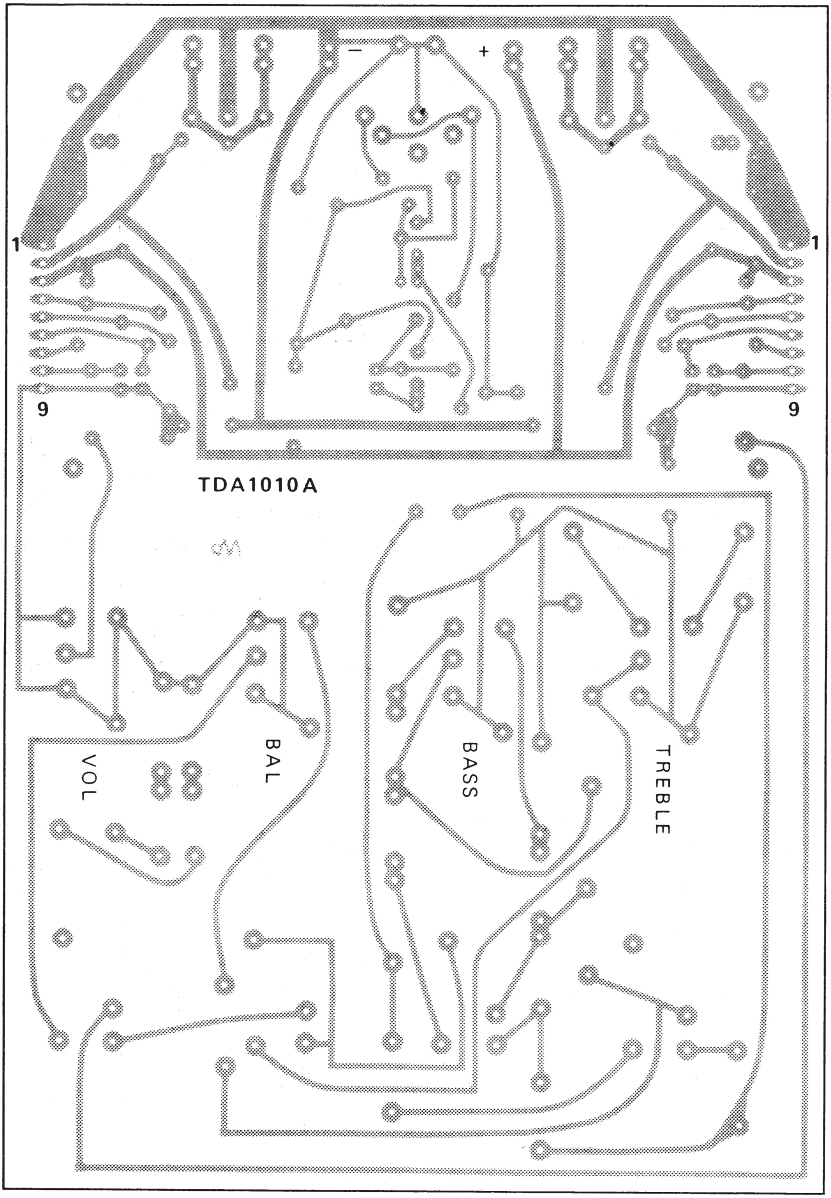

−
+
1
1
9
9
TDA1010A
VOL
BAL
BASS
TREBLE

Fig. 18 Track side of printed-circuit board used for the circuit of Fig. 17 (Fig. 16 partly); p.c. board dimensions 169 mm x 118 mm.

7Z77935

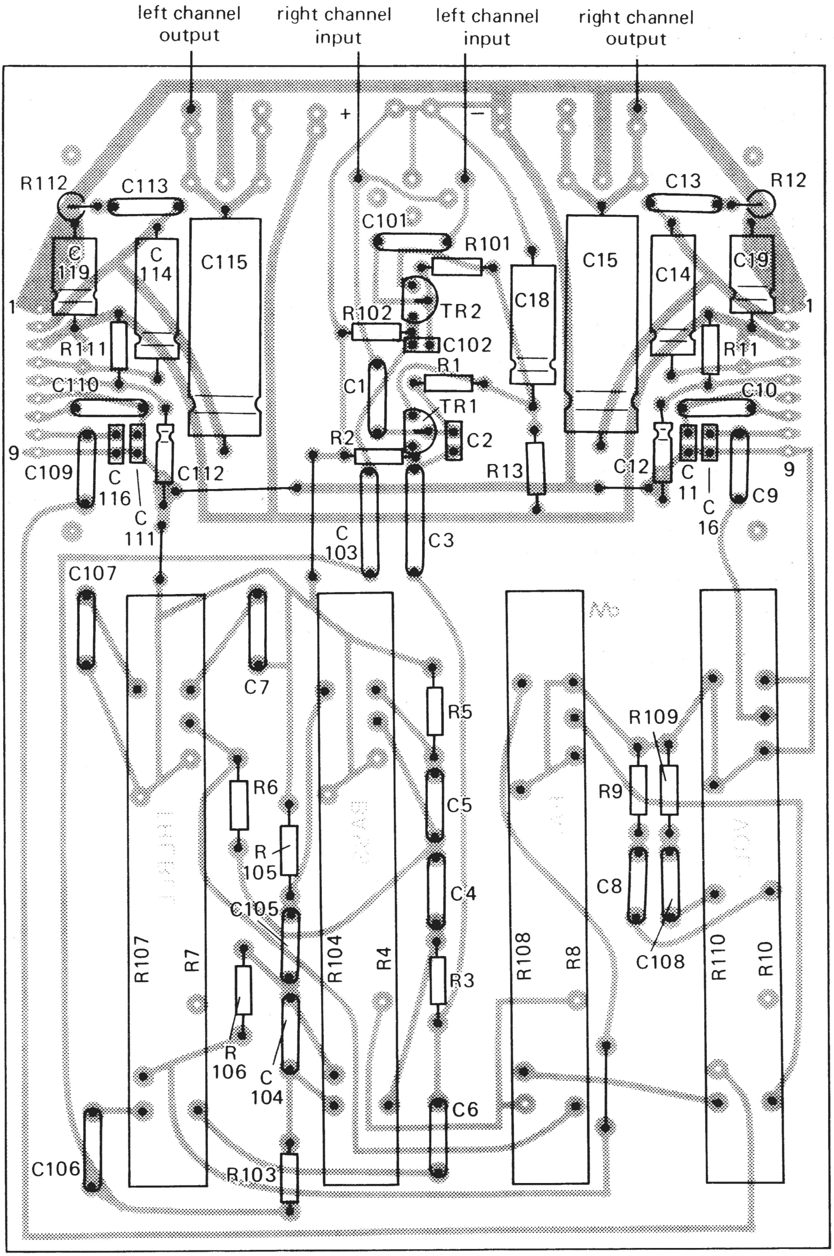

left channel output
right channel input
left channel input
right channel output
+
−
R112
C113
C101
R101
C15
C13
R12
C 119
C 114
C115
C18
C14
C19
1
1
R111
R102
TR2
C102
R11
C110
C1
R1
TR1
C10
C2
R2
9
C109
C 116
C 111
C112
R13
C12
C 11
C 16
9
C9
C 103
C3
C107
C7
R5
R109
R6
R9
C5
R 105
C4
C8
C105
C108
R107
R7
R104
R4
R3
R108
R8
R110
R10
R 106
C 104
C6
C106
R103
7Z77936

Fig. 19 Component side of printed-circuit board showing component layout used for the circuit of Fig. 17 (Fig. 16 partly).

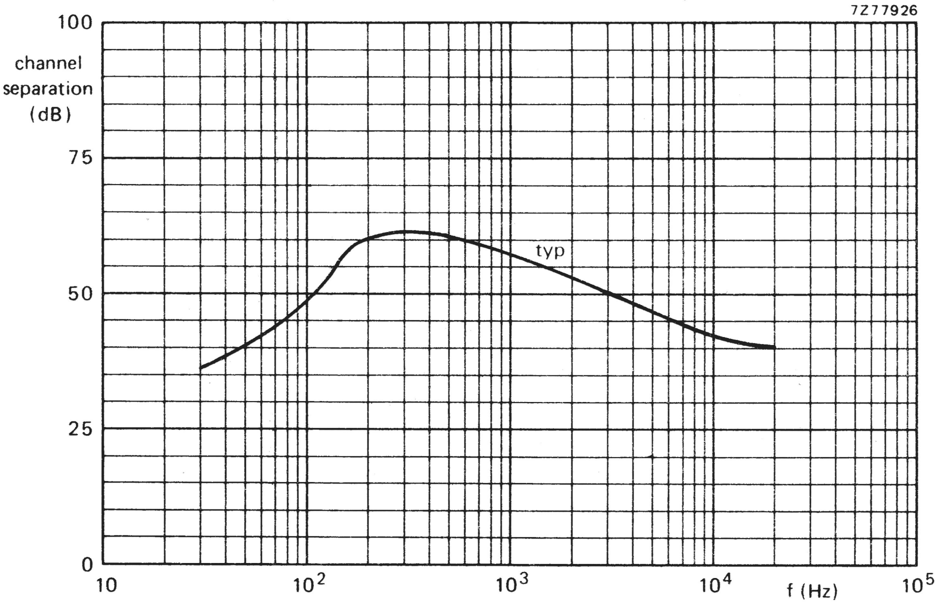


Fig. 20 Channel separation of the circuit of Fig. 17 as a function of frequency.

2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitabl for d.c. and a.c. apparatus, while the very low applicable supply voltage of 3,6 V permits 6 V application
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 20	V
Peak output current	I_{OM}	max.	3	A
Output power at d_{tot} = 10%				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\|Z_i\|$	>	100	kΩ
power amplifier (pin 6)	$\|Z_i\|$	typ.	20	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

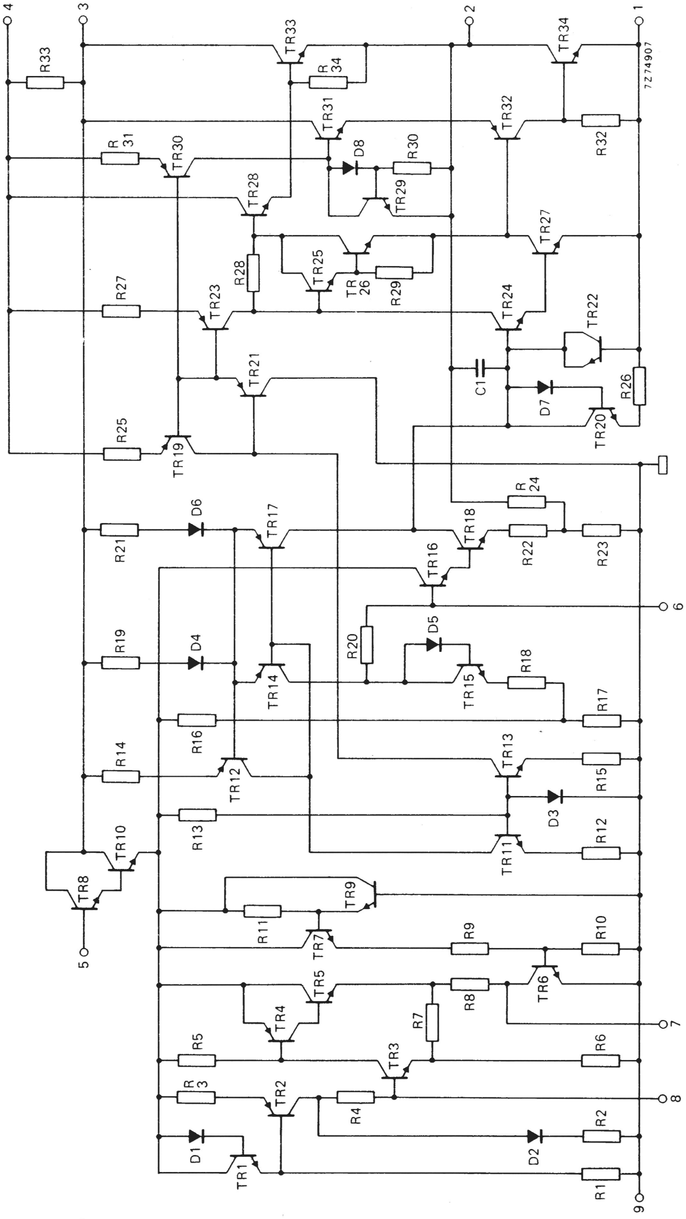

4
3
2
1
5
6
7
8
9
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
TR9
TR10
TR11
TR12
TR13
TR14
TR15
TR16
TR17
TR18
TR19
TR20
TR21
TR22
TR23
TR24
TR25
TR 26
TR27
TR28
TR29
TR30
TR31
TR32
TR33
TR34
R1
R2
R 3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R 24
R25
R26
R27
R28
R29
R30
R 31
R32
R33
R 34
D1
D2
D3
D4
D5
D6
D7
D8
C1
7Z74907

Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24	V
Peak output current	I_{OM}	max.	3	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature	T_{amb}	−25 to + 150		°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100	hours

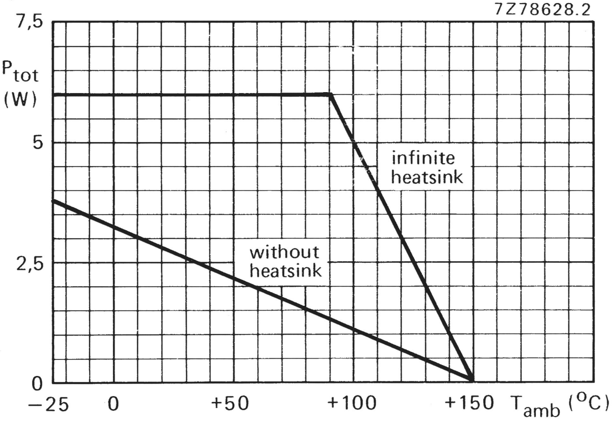


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 60 °C maximum; P_o = 3,8 W.

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150-60}{1,8} = 50\ \text{K/W}.$$

Since $R_{th\,j\text{-}tab}$ = 10 K/W and $R_{th\,tab\text{-}h}$ = 1 K/W, $R_{th\,h\text{-}a} = 50 - (10 + 1) = 39$ K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		3,6 to 20	V
Repetitive peak output current	I_{ORM}	<	2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ.	14	mA
		<	22	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)				
with bootstrap:				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	>	3,6	W
		typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
without bootstrap:				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	3,0	W
Voltage gain:				
preamplifier (note 2)	G_{v1}	typ.	23	dB
			21 to 25	dB
power amplifier	G_{v2}	typ.	29	dB
			27 to 31	dB
total amplifier	$G_{v\,tot}$	typ.	52	dB
			50 to 54	dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ.	0,3	%
		<	1	%
Frequency response; −3 dB (note 3)	B		60 Hz to 15	kHz
Input impedance:				
preamplifier (note 4)	$\|Z_{i1}\|$	>	100	kΩ
		typ.	200	kΩ
power amplifier	$\|Z_{i2}\|$	typ.	20	kΩ
Output impedance preamplifier	$\|Z_{o1}\|$	typ.	1	kΩ
Output voltage preamplifier (r.m.s. value)				
d_{tot} < 1% (note 2)	$V_{o(rms)}$	>	0,7	V
Noise output voltage (r.m.s. value; note 5)				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,6	mV
		<	1,4	mV
Noise output voltage at f = 500 kHz (r.m.s. value)				
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ.	8	μV
Ripple rejection (note 6)				
f = 1 to 10 kHz	RR	typ.	42	dB
f = 100 Hz; C2 = 1 μF	RR	>	35	dB
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ.	35	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

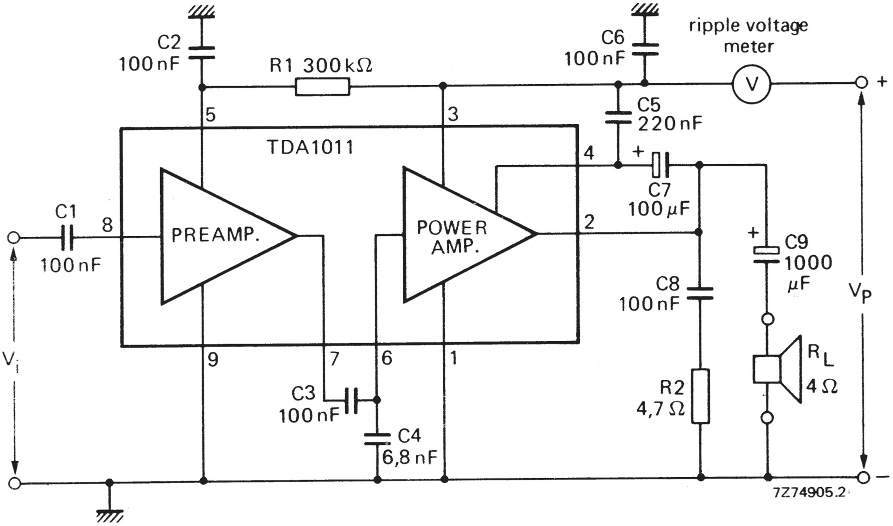

C2
100 nF
R1 300 kΩ
C6
100 nF
ripple voltage meter
V
+
5
3
C5
220 nF
TDA1011
4
+
C7
100 µF
C1
8
100 nF
PREAMP.
POWER AMP.
2
+
C9
1000 µF
C8
100 nF
V_P
V_i
9
7
6
1
R_L
4 Ω
C3
100 nF
C4
6,8 nF
R2
4,7 Ω
−
7Z74905.2

Fig. 3 Test circuit.

APPLICATION INFORMATION

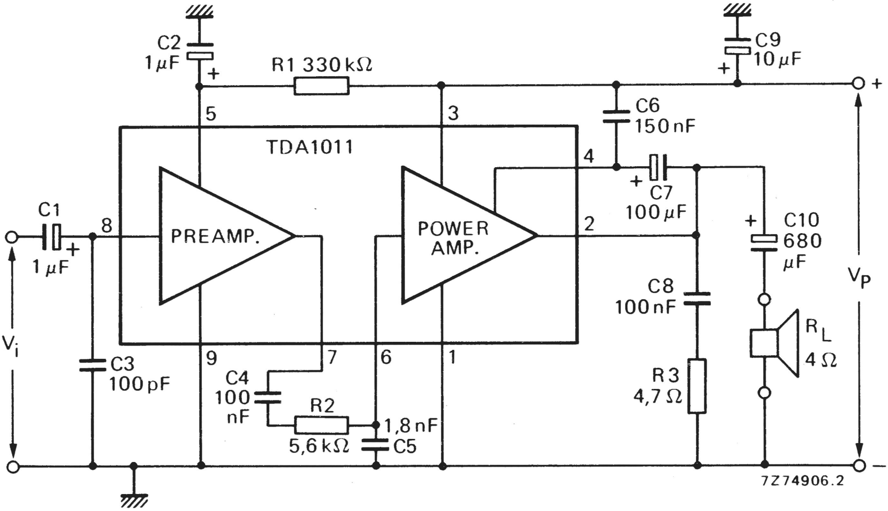

C2
1 μF
+
R1 330 kΩ
C9
10 μF
+
+
5
3
C6
150 nF
TDA1011
4
+
C7
100 μF
C1
8
PREAMP.
POWER
AMP.
2
+
C10
680
μF
V_P
+
1 μF
C8
100 nF
R_L
4 Ω
V_i
C3
100 pF
9
7
6
1
C4
100
nF
R2
5,6 kΩ
1,8 nF
C5
R3
4,7 Ω
−
7Z74906.2

Fig. 4 Circuit diagram of a 4 W amplifier.

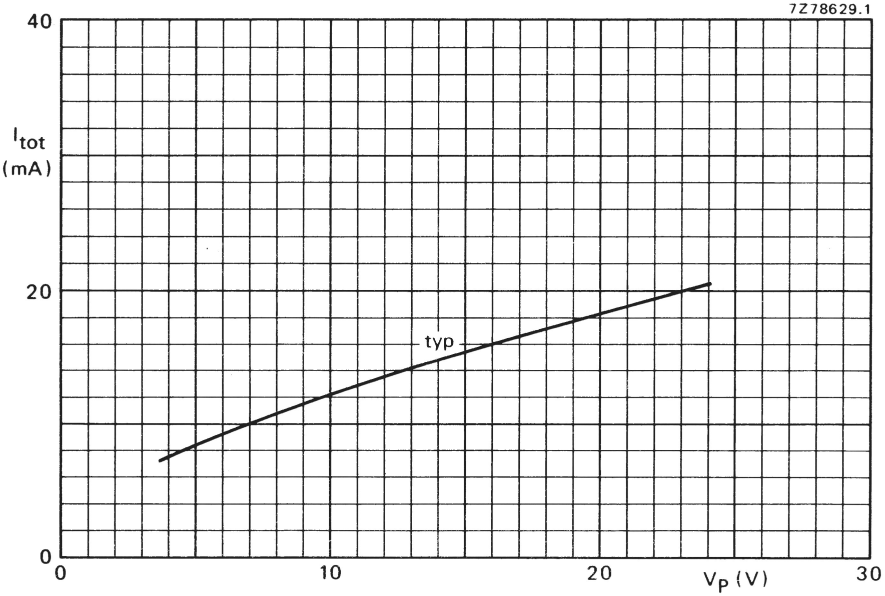
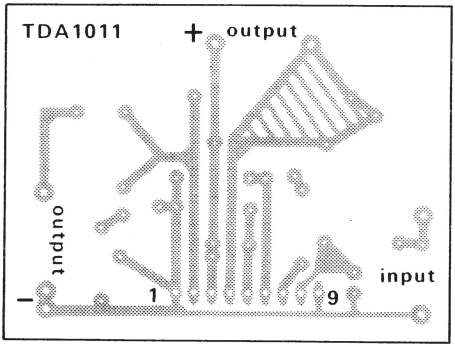
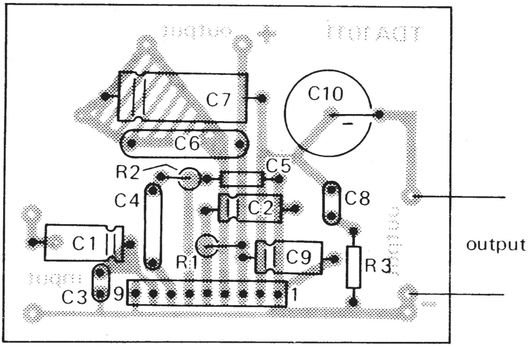


Fig. 5 Total quiescent current as a function of supply voltage.


TDA1011
+ output
output
–
1
9
input

7Z79431

Fig. 6 Track side of printed-circuit board used for the circuit of Fig. 4; p.c. board dimensions 62 mm x 48 mm.


C7
C10
C6
C5
R2
C4
C2
C8
C1
R1
C9
R3
output
C3
9
1

7Z79432.1

Fig. 7 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

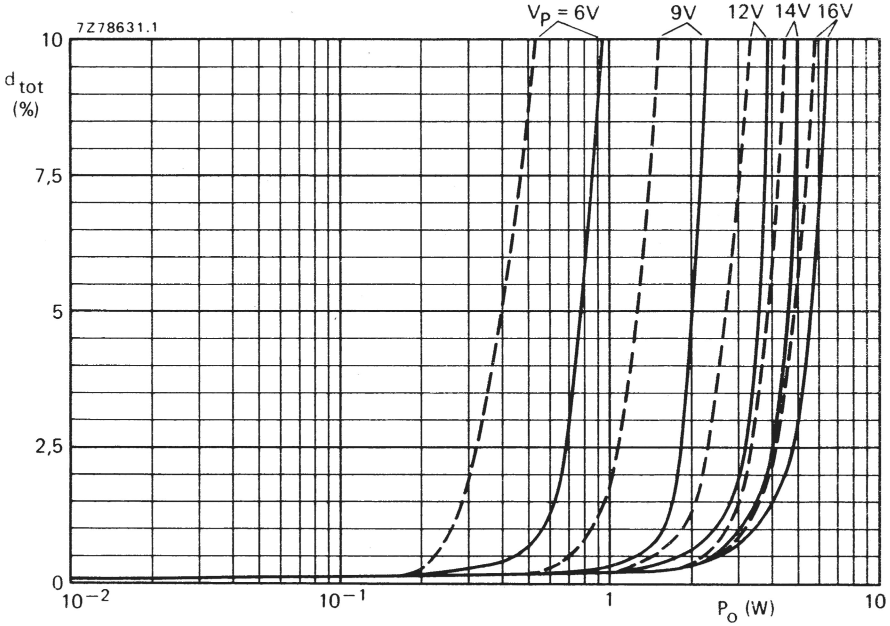


Fig. 8 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

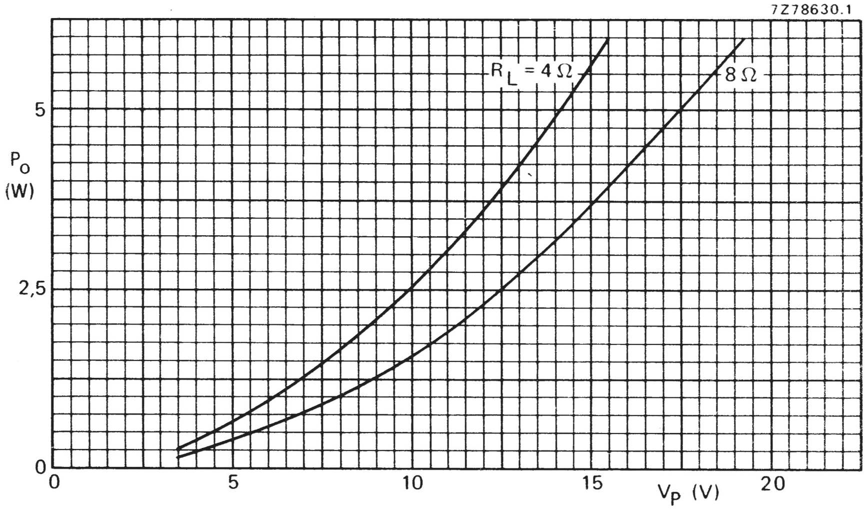


Fig. 9 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

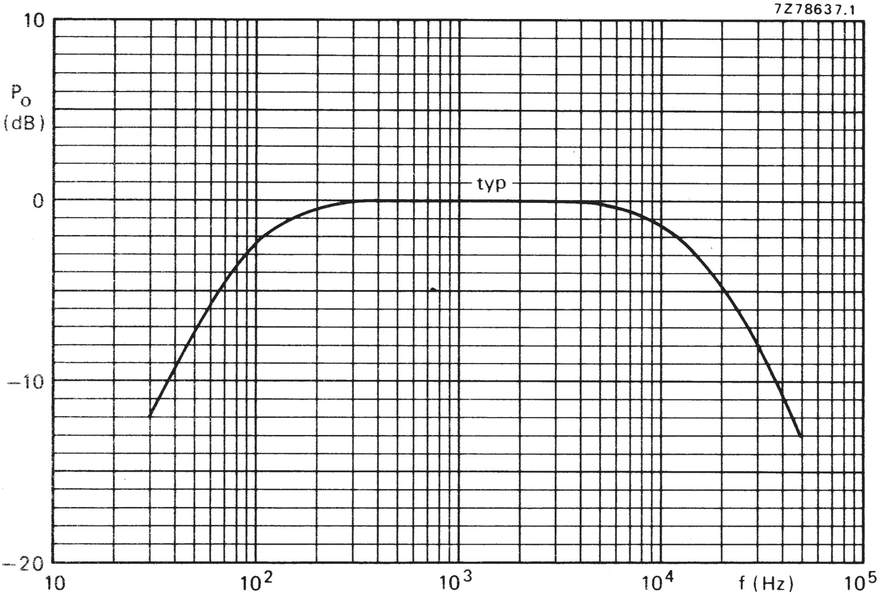


Fig. 10 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

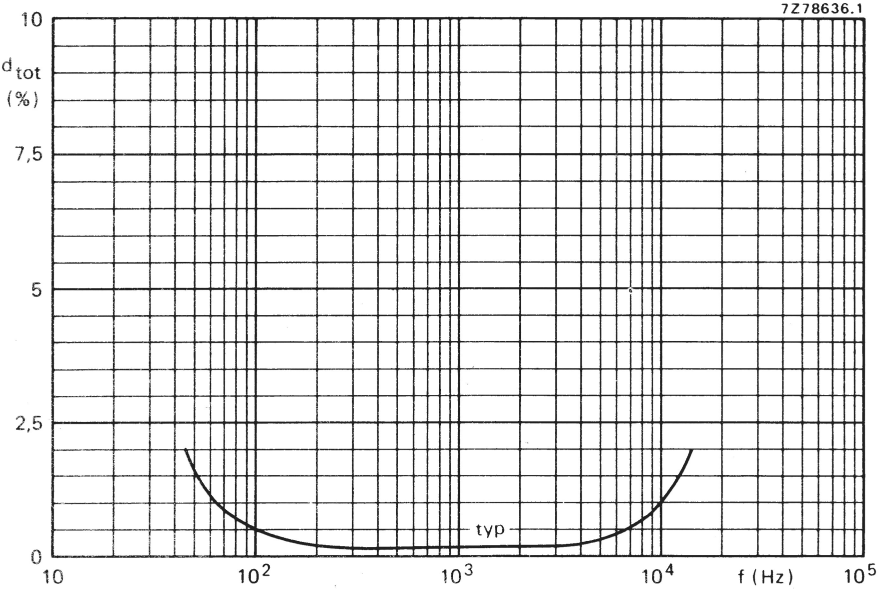


Fig. 11 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

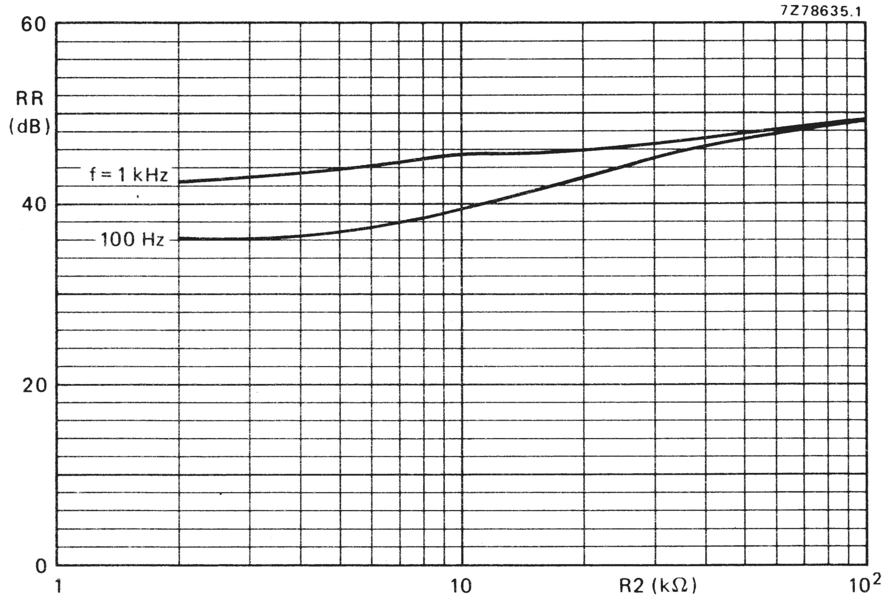


Fig. 12 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

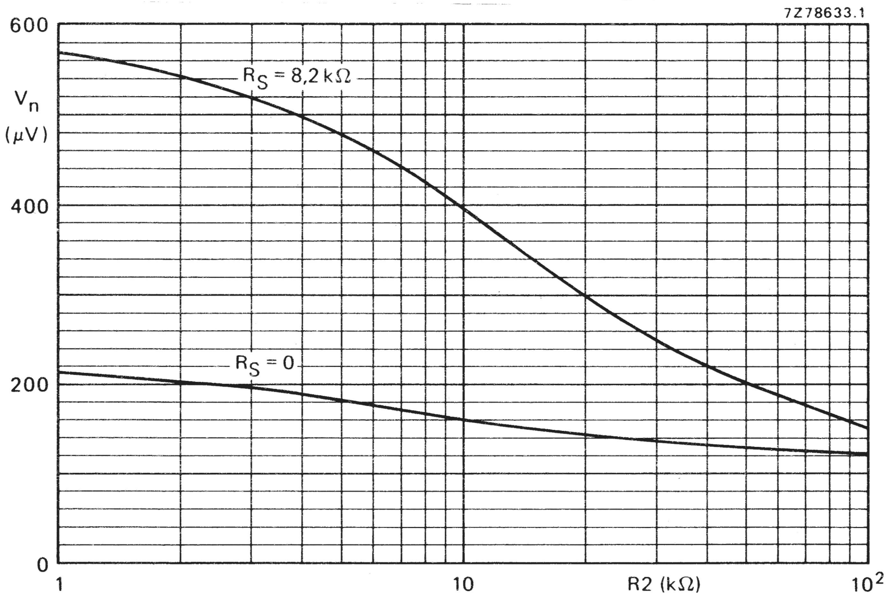


Fig. 13 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

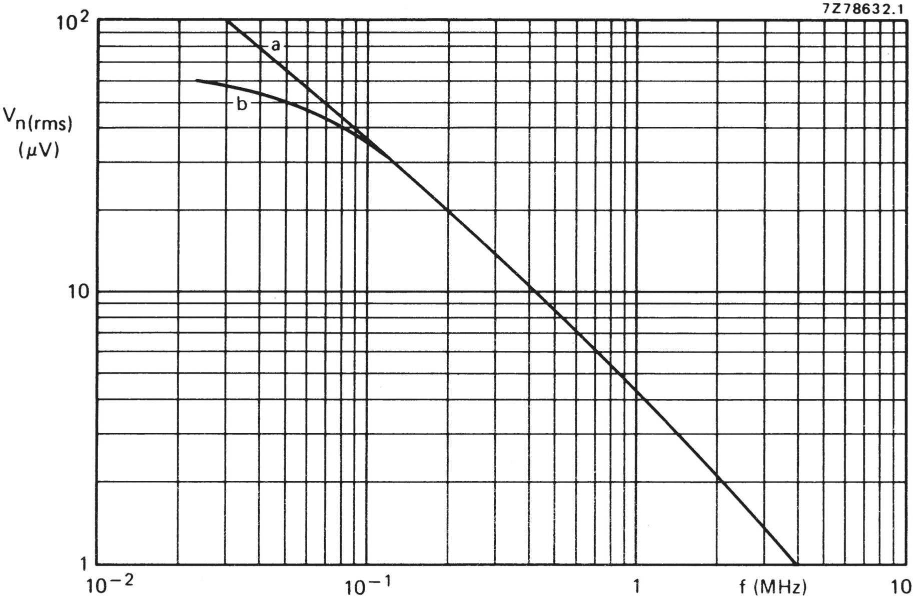


Fig. 14 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

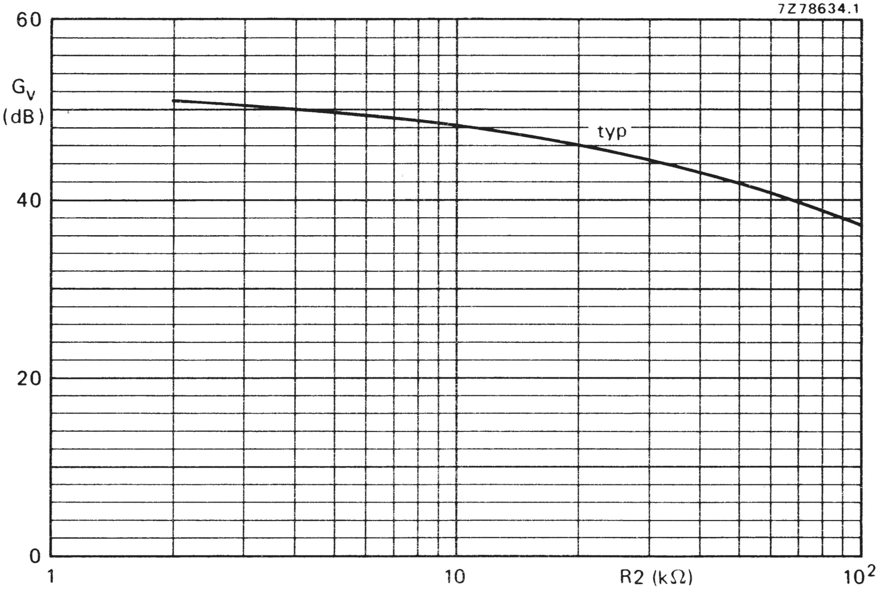


Fig. 15 Voltage gain as a function of R2 (see Fig. 4).

2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011A is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the low applicable supply voltage of 5,4 V permits 9 V applications. The power amplifier has an inverted input/output which makes the circuit optimal for applications with active tone control and spatial stereo. Special features are:

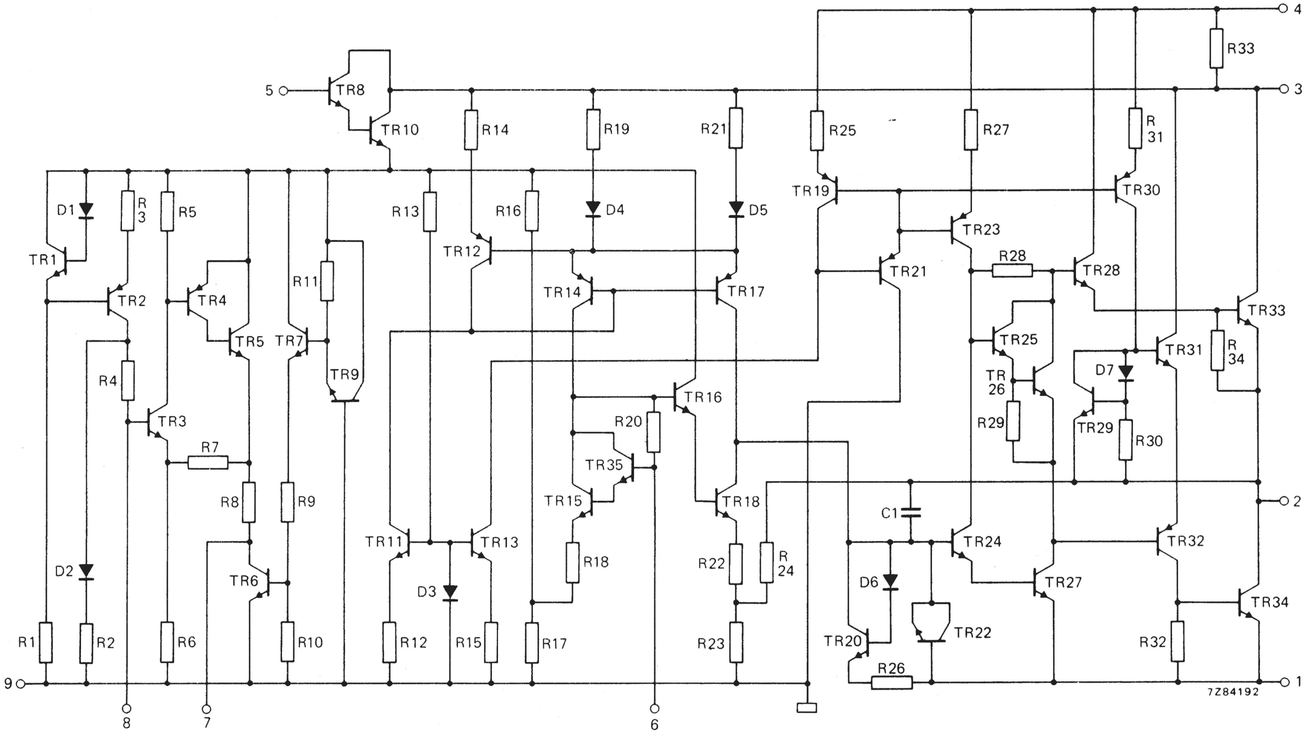
- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		5,4 to 20	V
Peak output current	I_{OM}	max.	3	A
Output power at d_{tot} = 10%				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	>	100	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).


4
3
2
1
5
9
8
7
6
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
TR9
TR10
TR11
TR12
TR13
TR14
TR15
TR16
TR17
TR18
TR19
TR20
TR21
TR22
TR23
TR24
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TR 26
TR27
TR28
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TR31
TR32
TR33
TR34
TR35
R1
R2
R 3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R 24
R25
R26
R27
R28
R29
R30
R 31
R32
R33
R 34
D1
D2
D3
D4
D5
D6
D7
C1
7Z84192

Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Peak output current	I_{OM}	max.	3 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150 °C	
Operating ambient temperature	T_{amb}	−25 to + 150 °C	
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

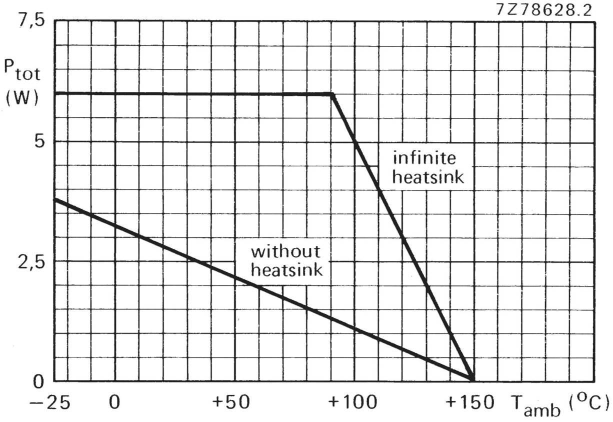


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume $V_P = 12$ V; $R_L = 4\ \Omega$; $T_{amb} = 60$ °C maximum; $P_o = 3{,}8$ W.

The maximum sine-wave dissipation is 1,8 W.

The derating of 10 K/W of the package requires the following external heatsink (for sine-wave drive):

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150 - 60}{1{,}8} = 50\ \text{K/W}.$$

Since $R_{th\,j\text{-}tab} = 10$ K/W and $R_{th\,tab\text{-}h} = 1$ K/W, $R_{th\,h\text{-}a} = 50 - (10 + 1) = 39$ K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		5,4 to 20	V
Repetitive peak output current	I_{ORM}	$<$	2	A
Total quiescent current at V_P = 12 V	I_{tot}	typ. $<$	14 22	mA mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)				
with bootstrap:				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	$>$ typ.	3,6 4,2	W W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
without bootstrap:				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	3,5	W
Voltage gain:				
preamplifier (note 2)	G_{v1}	typ. 	23 21 to 25	dB dB
power amplifier (note 3)	G_{v2}	typ.	29	dB
total amplifier (note 3)	$G_{v\,tot}$	typ.	52	dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ. $<$	0,3 1	% %
Frequency response; −3 dB (note 4)	B		60 Hz to 15	kHz
Input impedance:				
preamplifier (note 5)	$\lvert Z_{i1} \rvert$	$>$ typ.	100 200	kΩ kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ.	1	kΩ
Output voltage preamplifier (r.m.s. value)				
$d_{tot} < 1\%$ (note 2)	$V_{o(rms)}$	$>$	1,2	V
Noise output voltage (r.m.s. value; note 6)				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,5	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,8	mV
Noise output voltage at f = 500 kHz (r.m.s. value)				
B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ.	8	μV
Ripple rejection (note 6)				
f = 1 to 10 kHz	RR	typ.	42	dB
f = 100 Hz; C2 = 1 μF	RR	$>$	35	dB
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ.	35	mA
Stand-by current at maximum V_P (note 8)	I_{sb}	$<$	100	μA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured with R2 = 20 kΩ.
4. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
5. Independent of load impedance of preamplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).
8. The total current when disconnecting pin 5 or short-circuited to ground (pin 9).
9. The tab must be electrically floating or connected to the substrate (pin 9).

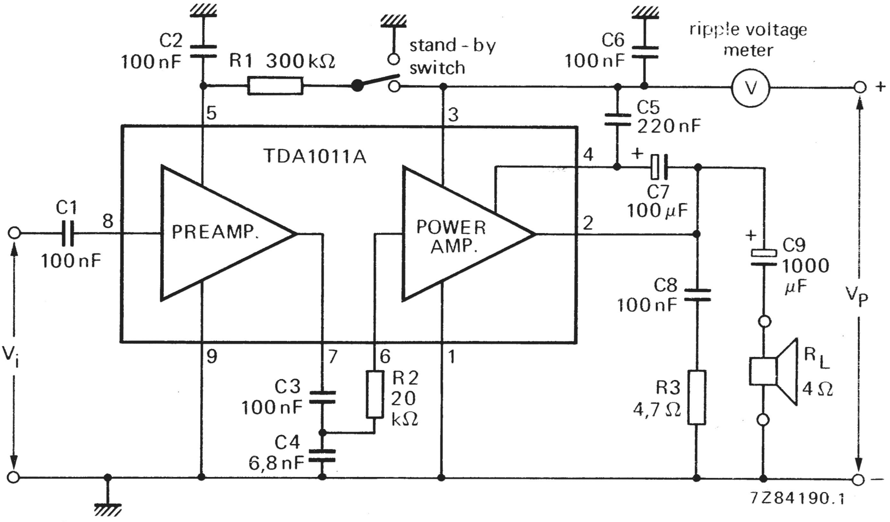

C2
100 nF
R1 300 kΩ
stand - by
switch
C6
100 nF
ripple voltage
meter
V
+
5
3
C5
220 nF
TDA1011A
4
+
C7
100 μF
C1
8
PREAMP.
POWER
AMP.
2
100 nF
+
C9
1000
μF
C8
100 nF
V_P
V_i
9
7
6
1
C3
100 nF
R2
20
kΩ
R3
4,7 Ω
R_L
4 Ω
C4
6,8 nF
−
7Z84190.1

Fig. 3 Test circuit.

APPLICATION INFORMATION

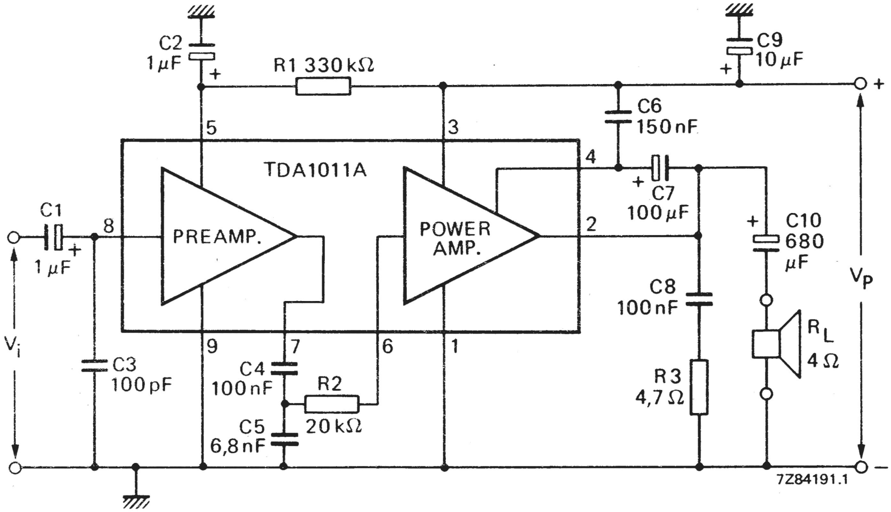

C2
1 μF
+
R1 330 kΩ
C9
10 μF
+
+
C6
150 nF
5
3
4
TDA1011A
C7
100 μF
+
C1
1 μF
+
8
PREAMP.
POWER
AMP.
2
C10
680
μF
+
V_P
C8
100 nF
R_L
4 Ω
V_i
C3
100 pF
9
7
6
1
C4
100 nF
R2
20 kΩ
C5
6,8 nF
R3
4,7 Ω
−
7Z84191.1

Fig. 4 Circuit diagram of a 4 W amplifier.

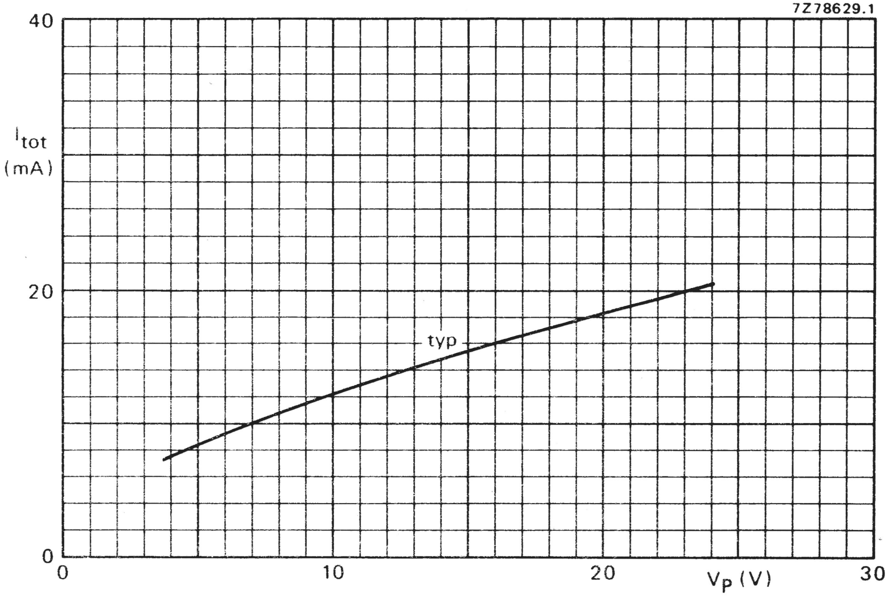


Fig. 5 Total quiescent current as a function of supply voltage.

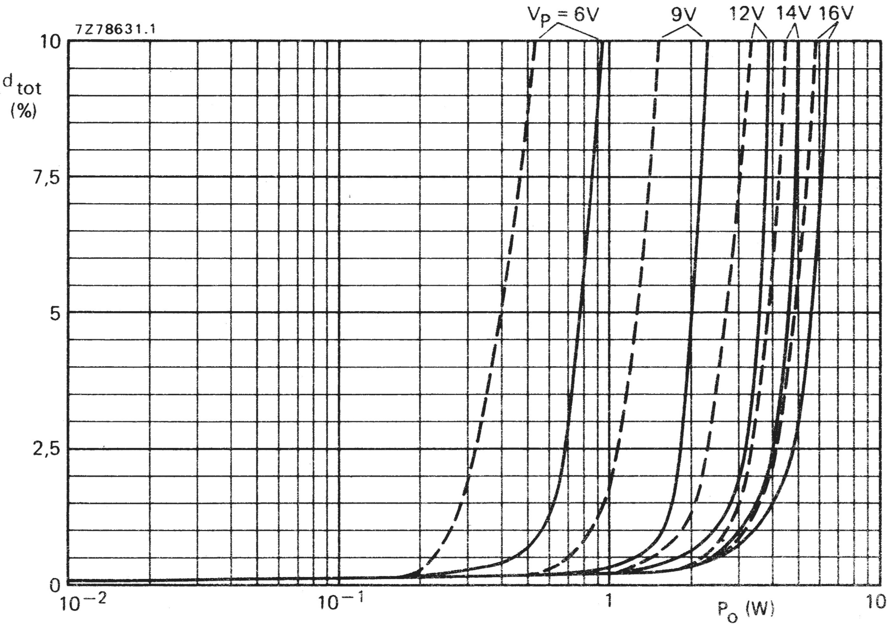


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; –·– – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

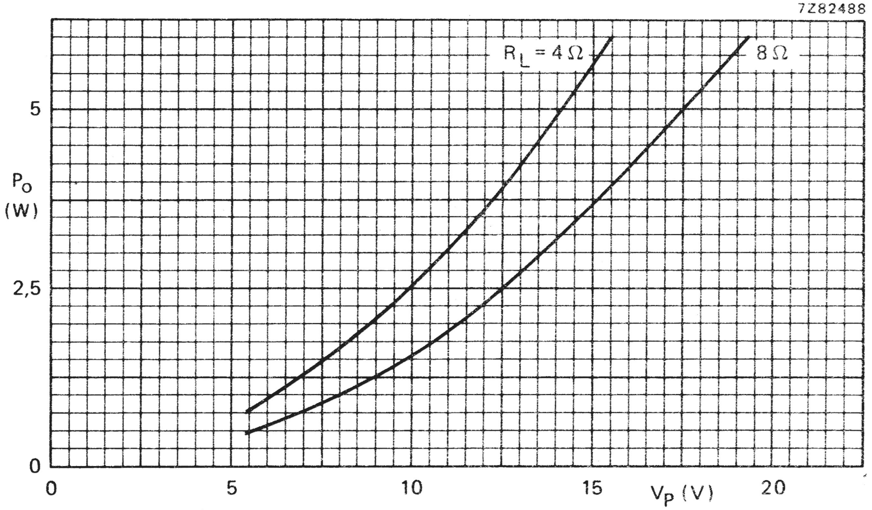


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

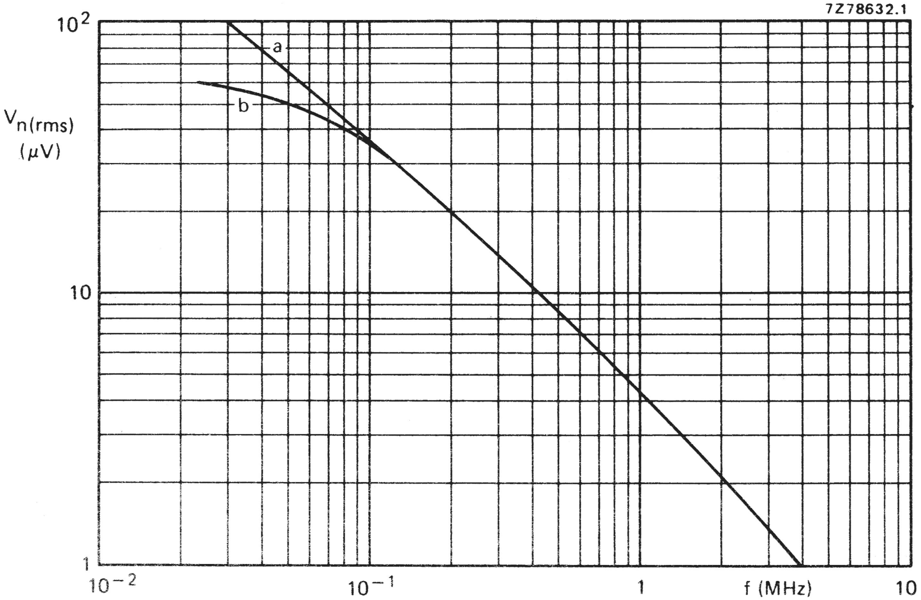


Fig. 8 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; $R_S = 0$; typical values.

RECORDING / PLAY-BACK AND 2 W AUDIO POWER AMPLIFIER

The TDA1012 is a monolithic integrated audio power amplifier, preamplifier and A.L.C. circuit designed for applications in radio-recorders and recorders. The wide supply voltage range makes this circuit very suitable for d.c. and a.c. apparatus. The circuit is thermal protected and contains the following functions:

- Power amplifier
- Preamplifier
- Automatic Level Control (A.L.C.) circuit
- Voltage stabilizer

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 18	V
Total quiescent current at $V_p = 9$ V	I_{tot}	typ.	14	mA
Power amplifier				
Output power at $d_{tot} = 10$ % $V_P = 9$ V; $R_L = 4\ \Omega$	P_o	typ.	2	W
Closed loop voltage gain	G_c	typ.	36	dB
Preamplifier				
Open loop voltage gain	G_o	>	66	dB
Minimum closed loop voltage gain	$G_{c\ min}$		31	dB
Output voltage at $d_{tot} = 1$ %	V_o	>	2	V
Automatic Level Control (A.L.C.)				
Gain variation for $\Delta V_i = 40$ dB	ΔG_v	typ.	2	dB
Stabilized supply voltage				
Output voltage	$V_{11\text{-}15}$	typ.	4,2	V

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT-38WE-2).

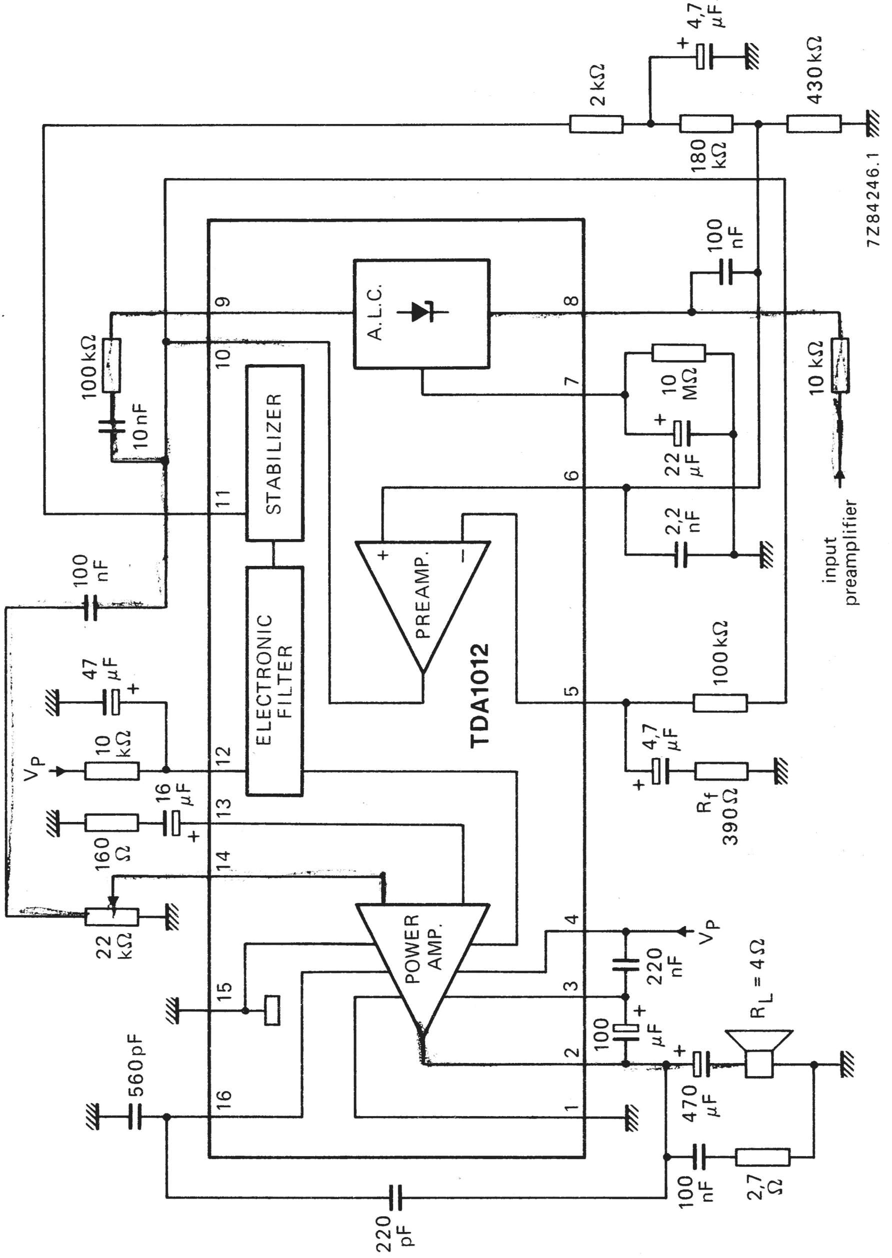

TDA1012
A.L.C.
STABILIZER
ELECTRONIC FILTER
PREAMP.
POWER AMP.
+
−
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
2 kΩ
4,7 μF
180 kΩ
430 kΩ
100 nF
10 kΩ
input preamplifier
10 MΩ
22 μF
2,2 nF
100 kΩ
4,7 μF
R_f 390 Ω
V_P
220 nF
100 μF
R_L = 4 Ω
470 μF
100 nF
2,7 Ω
220 pF
560 pF
22 kΩ
160 Ω
16 μF
10 kΩ
47 μF
100 nF
10 nF
100 kΩ
7Z84246.1

Fig. 1 Block diagram/test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 4)	$V_P = V_{4-1}$	max.	18 V
Non-repetitive peak output current (pin 2)	I_{OSM}	max.	2 A
Storage temperature	T_{stg}		−55 to +150 °C
Crystal temperature	T_c	max.	150 °C
Total power dissipation	see derating curve Fig. 2		
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100 hours

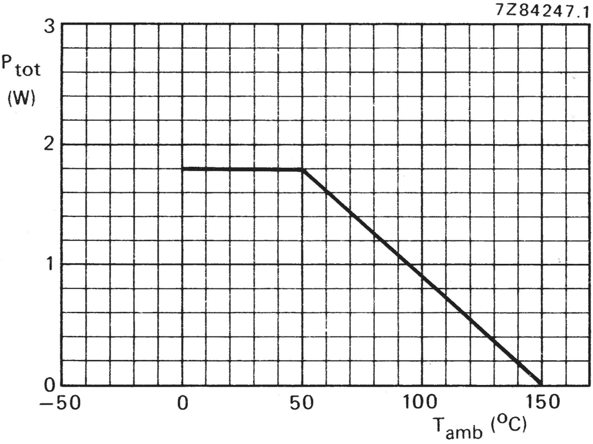


Fig. 2 Power derating curve.

THERMAL RESISTANCE

From junction to ambient	$R_{th\,j\text{-}a}$	=	55 K/W

CHARACTERISTICS

V_P = 9 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 1; unless otherwise specified.

Power amplifier

Output power at d_{tot} = 10 %	P_o	typ.	2 W
Closed loop voltage gain	G_c	typ.	36 dB
Total harmonic distortion at P_o = 1W	d_{tot}	<	1 %
Input impedance	$\lvert Z_i \rvert$	>	1 MΩ
Ripple rejection at f = 100 Hz	RR	>	40 dB
Noise output voltage (r.m.s. value) R_S = 0 Ω; B = 60 Hz to 15 kHz	$V_{n(rms)}$	typ.	150 μV

Preamplifier

Open loop voltage gain	G_o	>	66 dB
Closed loop voltage gain	G_c	typ.	48 dB
Minimum closed loop voltage gain (when changing R_f)	$G_{c\,min}$		31 dB
Output voltage at d_{tot} = 1 %	V_o	>	2 V
Output voltage with A.L.C. V_i = 4,8 mV	V_o	typ.	1,1 V
Total harmonic distortion with A.L.C. V_i = 4,8 mV	d_{tot}	<	1 %
V_i = 480 mV	d_{tot}	<	3 %
Signal-to-noise ratio related to V_i = 1,2 mV; R_S = 0 Ω; B = 60 Hz to 15 kHz	S/N	typ.	60 dB
Input impedance	$\lvert Z_i \rvert$	>	100 kΩ
Ripple rejection at f = 100 Hz	RR	>	52 dB
Output impedance	$\lvert Z_o \rvert$	<	50 Ω

Automatic Level Control (A.L.C.)

Gain variation for ΔV_i = 40 dB	ΔG_v	typ.	2 dB
Limiting time at ΔV_i = 40 dB	t_l	<	50 ms
Level setting time at ΔV_i = 40 dB	t_s	<	50 ms
Recovery time at ΔV_i = 40 dB	t_r	typ.	100 s

Voltage stabilizer

Output voltage	$V_{11\text{-}15}$	typ.	4,2 V
Load current	I_{11}	<	1 mA
Ripple rejection at f = 100 Hz	RR	>	40 dB

4 W AUDIO POWER AMPLIFIER WITH D.C. VOLUME CONTROL

The TDA1013A is a monolithic integrated audio amplifier circuit with d.c. volume control in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit very suitable for applications in mains-fed apparatus such as television receivers and record players.

The d.c. volume control stage has a logarithmic control characteristic with a range of more than 80 dB; control can be obtained by means of a variable d.c. voltage between 3,5 and 8 V.

The audio amplifier has a well defined open loop gain and a fixed integrated closed loop gain. This offers an optimum in number of external components, performance and stability.

The SIL package (SOT-110B) offers a simple and low-cost heatsink connection.

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35 V
Repetitive peak output current	I_{ORM}	max.	1,5 A
Total sensitivity (d.c. control at max. gain) for P_o = 2,5 W	V_i	typ.	55 mV
Audio amplifier			
Output power at d_{tot} = 10% V_P = 18 V; R_L = 8 Ω	P_o	typ.	4,5 W
Total harmonic distortion at P_o = 2,5 W; R_L = 8 Ω	d_{tot}	typ.	0,5 %
Sensitivity for P_o = 2,5 W	V_i	typ.	125 mV
D.C. volume control unit			
Gain control range	ϕ	>	80 dB
Signal handling at d_{tot} < 1% (d.c. control at 0 dB)	V_i	>	1,2 V
Sensitivity for V_o = 125 mV at max. voltage gain	V_i	typ.	55 mV
Input impedance (pin 8)	$\|Z_i\|$	typ.	250 kΩ

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

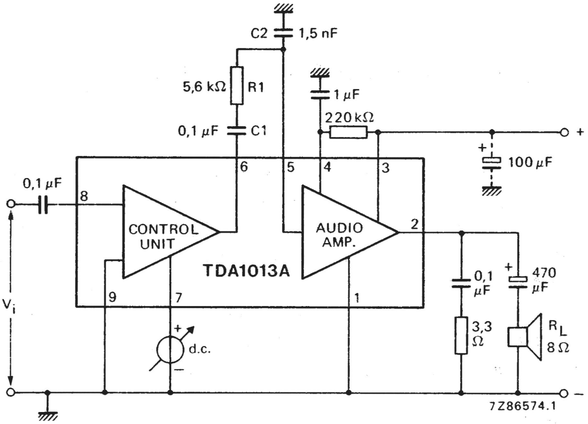

C2
1,5 nF
5,6 kΩ
R1
0,1 µF
C1
1 µF
220 kΩ
+ 18 V
+
100 µF
0,1 µF
8
6
5
4
3
CONTROL UNIT
AUDIO AMP.
2
TDA1013A
0,1 µF
+
470 µF
9
7
1
V_i
+
d.c.
–
3,3 Ω
R_L
8 Ω
–
7Z86574.1

Fig. 1 Application diagram and external components; also used as test circuit with R1 = 5,1 kΩ, C1 = 220 nF and C2 = 2,2 nF.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Storage temperature	T_{stg}		−55 to + 150 °C
Crystal temperature	T_j		−25 to + 150 °C
Total power dissipation	see derating curve Fig. 2		

HEATSINK DESIGN

Assume $V_P = 18$ V; $R_L = 8\ \Omega$; $T_{amb} = 60\ ^{o}C$ (max.); $T_j = 150\ ^{o}C$ (max.; for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,5 W.
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2,5} = 36\ K/W.$$

Since $R_{th\ j\text{-}tab} = 9$ K/W and $R_{th\ tab\text{-}h} = 1$ K/W, $R_{th\ h\text{-}a} = 36 - (9 + 1) = 26$ K/W.

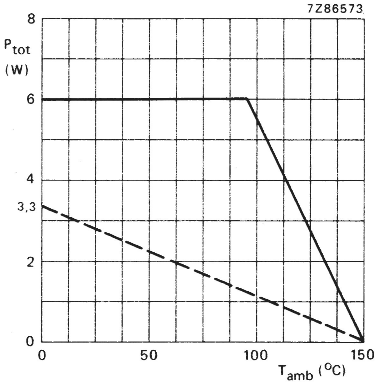


Fig. 2 Power derating curve.
——— infinite heatsink;
– – – without heatsink.

CHARACTERISTICS

$V_P = 18$ V; $R_L = 8\ \Omega$; f = 1 kHz; $T_{amb} = 25$ °C; unless otherwise specified

Supply voltage	V_P	typ.	18	V
			15 to 35	V
Total quiescent current	I_{tot}	typ.	35	mA
Noise output voltage (see also note)	V_n	<	2	mV
Total sensitivity (d.c. control at maximum gain) for $P_o = 2{,}5$ W	V_i	typ.	55	mV
Frequency response (–3 dB)	f		35 Hz to 20	kHz
Audio amplifier				
Repetitive peak output current	I_{ORM}	<	1,5	A
Output power at $d_{tot} = 10\%$	P_o	>	4	W
		typ.	4,5	W
Total harmonic distortion at $P_o = 2{,}5$ W	d_{tot}	typ.	0,5	%
Voltage gain	G_v	typ.	30	dB
Sensitivity for $P_o = 2{,}5$ W	V_i	typ.	125	mV
Input impedance (pin 5)	$\|Z_i\|$	>	100	kΩ
		typ.	250	kΩ

Note

Measured in a bandwidth according to IEC-curve ‘A’; $R_S = 5$ kΩ.

CHARACTERISTICS (continued)

D.C. volume control unit

Gain control range (see also Fig. 3)	ϕ	>	80 dB
Signal handling at $d_{tot} < 1\%$ (d.c. control at 0 dB)	V_i	>	1,2 V
Sensitivity for V_o = 125 mV at max. voltage gain	V_i	typ.	55 mV
Input impedance (pin 8)	$\lvert Z_i \rvert$	> typ.	100 kΩ 250 kΩ
Output impedance (pin 6)	$\lvert Z_o \rvert$	typ.	200 Ω

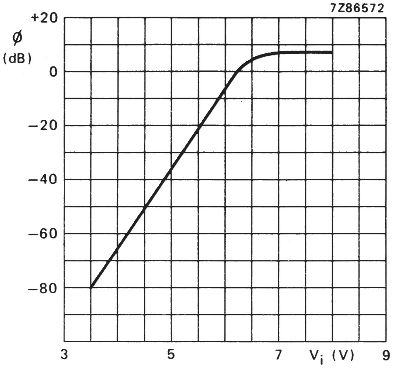


Fig. 3 Gain control curve; V_i at pin 7.

1 TO 4 W AUDIO POWER AMPLIFIER

The TDA1015 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The very low applicable supply voltage of 3,6 V permits 6 V applications. Special features are:

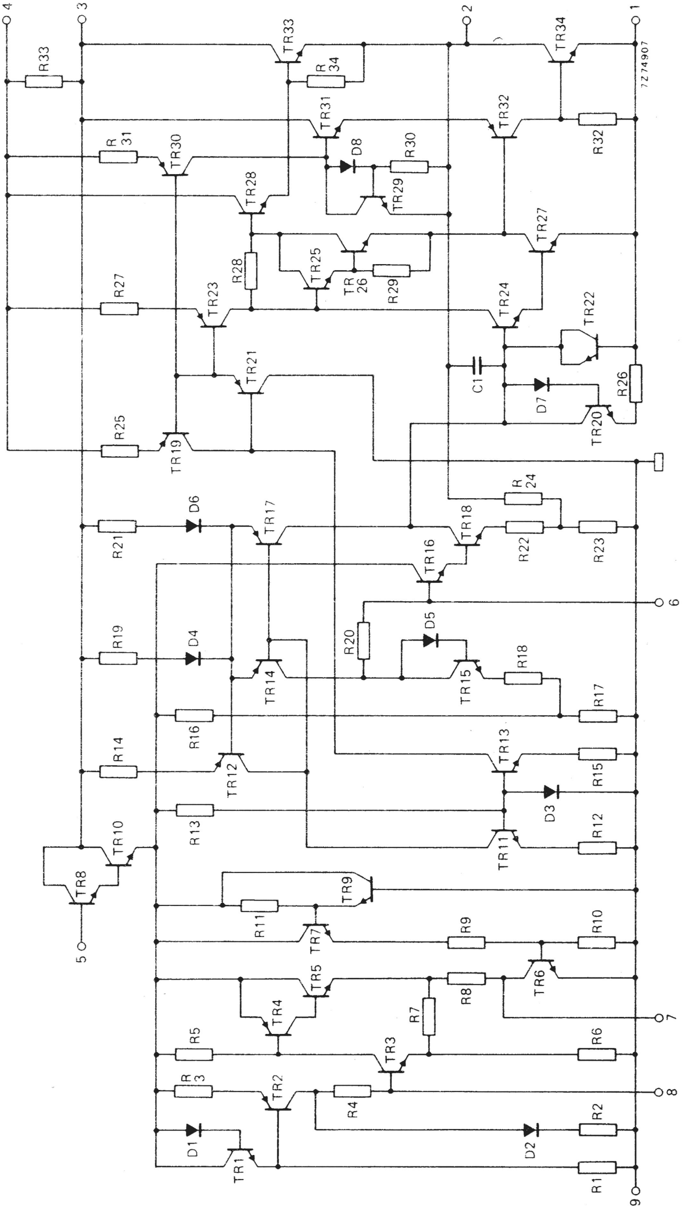
- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 18	V
Peak output current	I_{OM}	max.	2,5	A
Output power at d_{tot} = 10%				
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,3	%
Input impedance				
preamplifier (pin 8)	$\|Z_i\|$	>	100	kΩ
power amplifier (pin 6)	$\|Z_i\|$	typ.	20	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).


4
3
2
1
5
6
7
8
9
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
TR9
TR10
TR11
TR12
TR13
TR14
TR15
TR16
TR17
TR18
TR19
TR20
TR21
TR22
TR23
TR24
TR25
TR 26
TR27
TR28
TR29
TR30
TR31
TR32
TR33
TR34
R1
R2
R 3
R4
R5
R6
R7
R8
R9
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R11
R12
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R14
R15
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R17
R18
R19
R20
R21
R22
R23
R 24
R25
R26
R27
R28
R29
R30
R 31
R32
R33
R 34
D1
D2
D3
D4
D5
D6
D7
D8
C1
7Z74907

Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Peak output current	I_{OM}	max.	2,5	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100	hours

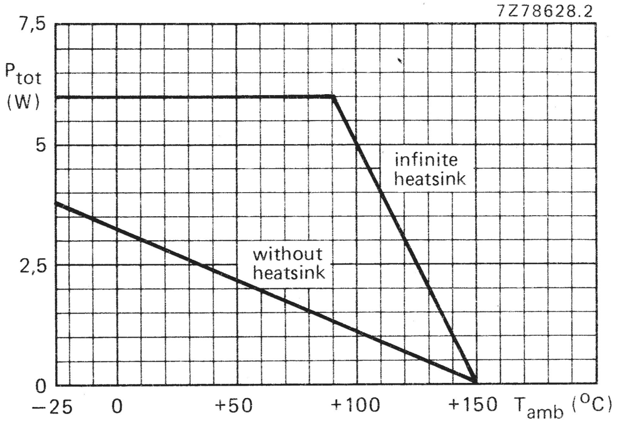


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 12 V; R_L = 4 Ω; T_{amb} = 45 °C maximum.

The maximum sine-wave dissipation is 1,8 W.

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150 - 45}{1,8} = 58 \text{ K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 45 K/W, so no external heatsink is required.

D.C. CHARACTERISTICS

Supply voltage range	V_P		3,6 to 18	V
Repetitive peak output current	I_{ORM}	<	2	A
Total quiescent current at $V_P = 12$ V	I_{tot}	typ. <	14 25	mA mA

A.C. CHARACTERISTICS

$T_{amb} = 25\ ^oC$; $V_P = 12$ V; $R_L = 4\ \Omega$; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at $d_{tot} = 10\%$ (note 1)				
with bootstrap:				
$V_P = 12$ V; $R_L = 4\ \Omega$	P_o	typ.	4,2	W
$V_P = 9$ V; $R_L = 4\ \Omega$	P_o	typ.	2,3	W
$V_P = 6$ V; $R_L = 4\ \Omega$	P_o	typ.	1,0	W
without bootstrap:				
$V_P = 12$ V; $R_L = 4\ \Omega$	P_o	typ.	3,0	W
Voltage gain:				
preamplifier (note 2)	G_{v1}	typ.	23	dB
power amplifier	G_{v2}	typ.	29	dB
total amplifier	$G_{v\,tot}$	typ.	52 49 to 55	dB dB
Total harmonic distortion at $P_o = 1,5$ W	d_{tot}	typ. <	0,3 1,0	% %
Frequency response; −3 dB (note 3)	B		60 Hz to 15	kHz
Input impedance:				
preamplifier (note 4)	$\lvert Z_{i1} \rvert$	> typ.	100 200	kΩ kΩ
power amplifier	$\lvert Z_{i2} \rvert$	typ.	20	kΩ
Output impedance preamplifier	$\lvert Z_{o1} \rvert$	typ.	1	kΩ
Output voltage preamplifier (r.m.s. value)				
$d_{tot} < 1\%$ (note 2)	$V_{o(rms)}$	typ.	0,8	V
Noise output voltage (r.m.s. value; note 5)				
$R_S = 0\ \Omega$	$V_{n(rms)}$	typ.	0,2	mV
$R_S = 10$ kΩ	$V_{n(rms)}$	typ.	0,5	mV
Noise output voltage at f = 500 kHz (r.m.s. value)				
B = 5 kHz; $R_S = 0\ \Omega$	$V_{n(rms)}$	typ.	8	μV
Ripple rejection (note 6)				
f = 100 Hz	RR	typ.	38	dB

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).
7. The tab must be electrically floating or connected to the substrate (pin 9).

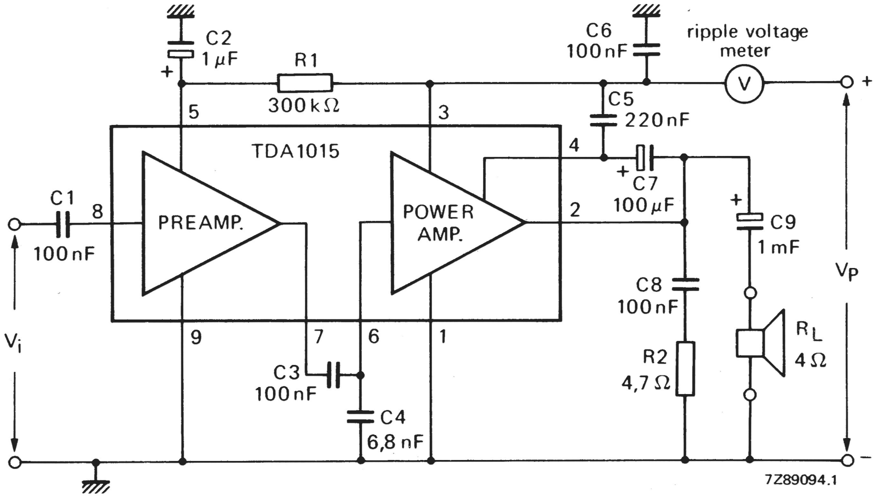

C2
1 μF
+
R1
300 kΩ
C6
100 nF
ripple voltage meter
V
+
5
3
C5
220 nF
TDA1015
4
+
C7
100 μF
C1
8
PREAMP.
POWER AMP.
2
+
C9
1 mF
100 nF
C8
100 nF
V_P
V_i
9
7
6
1
R2
4,7 Ω
R_L
4 Ω
C3
100 nF
C4
6,8 nF
–
7Z89094.1

Fig. 3 Test circuit.

APPLICATION INFORMATION

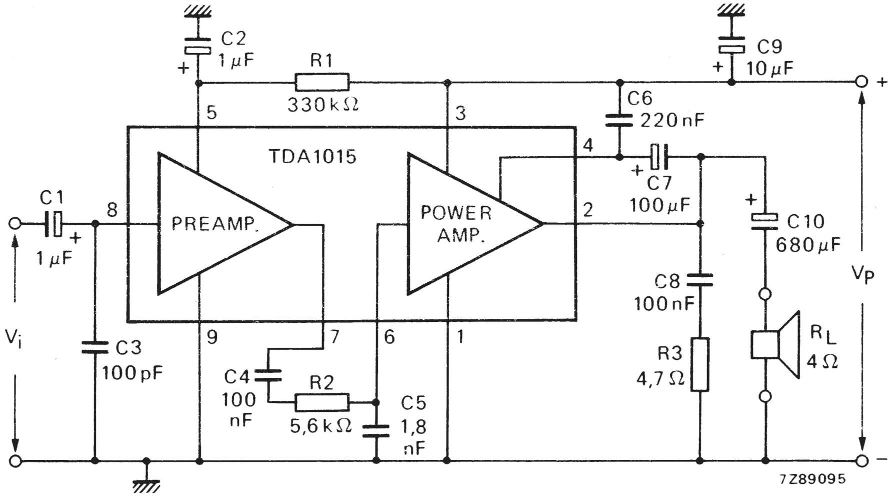

C2
1 μF
+
R1
330 kΩ
C9
10 μF
+
C6
220 nF
5
3
4
TDA1015
PREAMP.
POWER
AMP.
C1
1 μF
+
8
2
+
C7
100 μF
+
C10
680 μF
VP
Vi
C3
100 pF
9
7
6
1
C8
100 nF
R3
4,7 Ω
RL
4 Ω
C4
100
nF
R2
5,6 kΩ
C5
1,8
nF
7Z89095

Fig. 4 Circuit diagram of a 1 to 4 W amplifier.

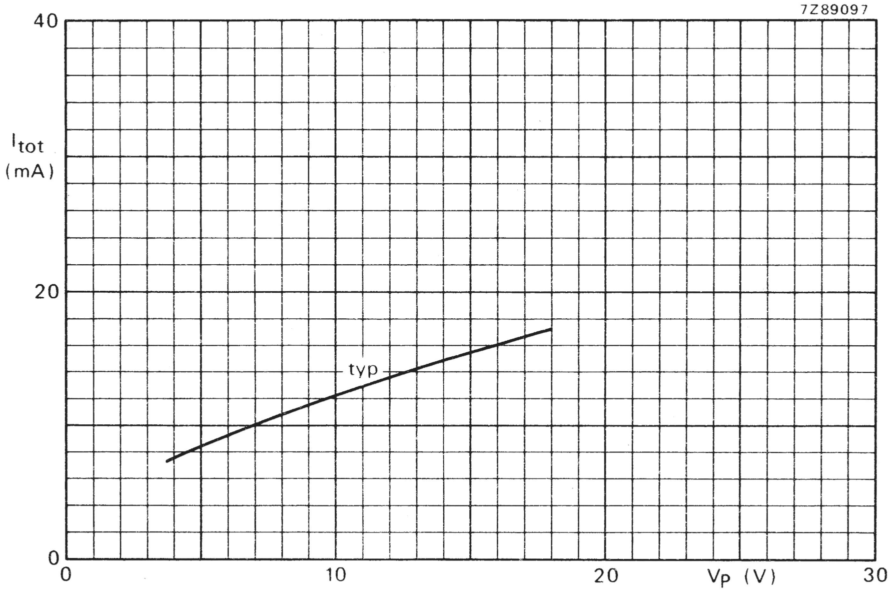


Fig. 5 Total quiescent current as a function of supply voltage.

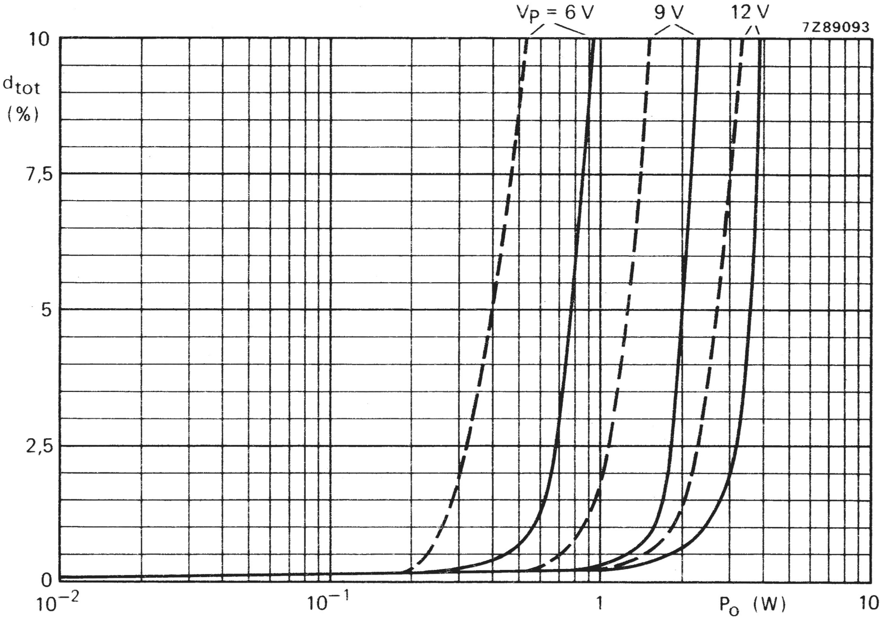


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

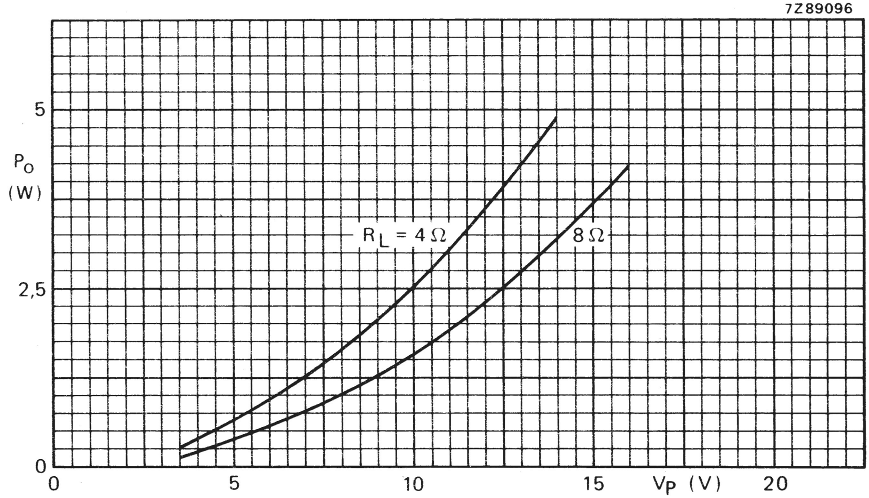


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

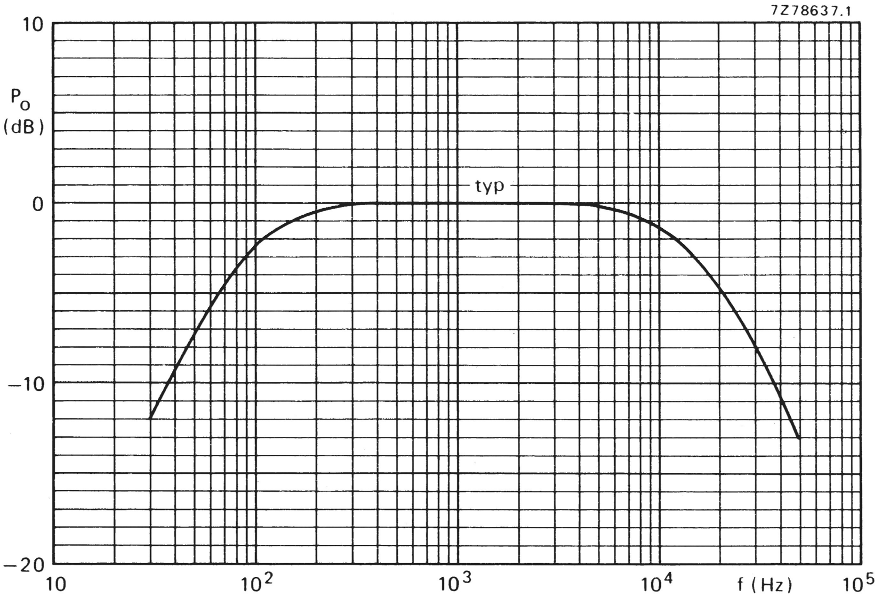


Fig. 8 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

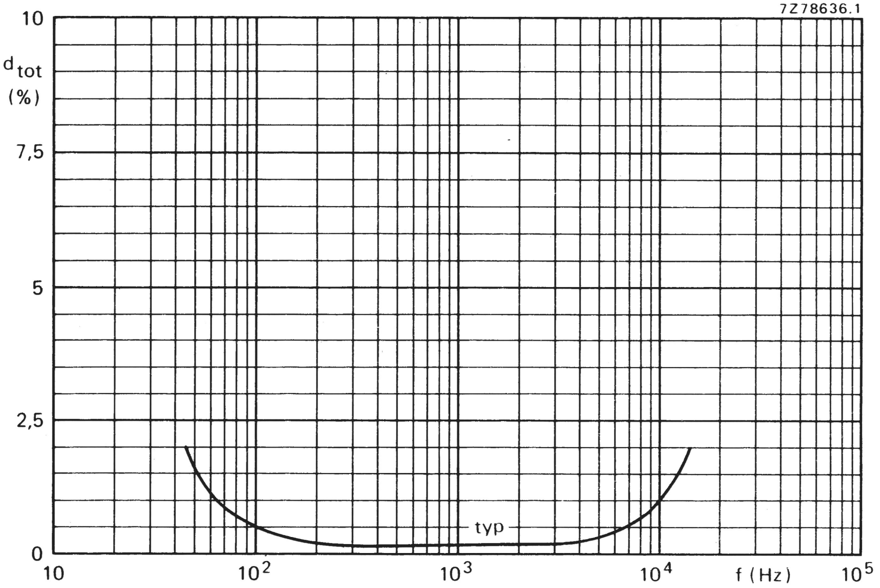


Fig. 9 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

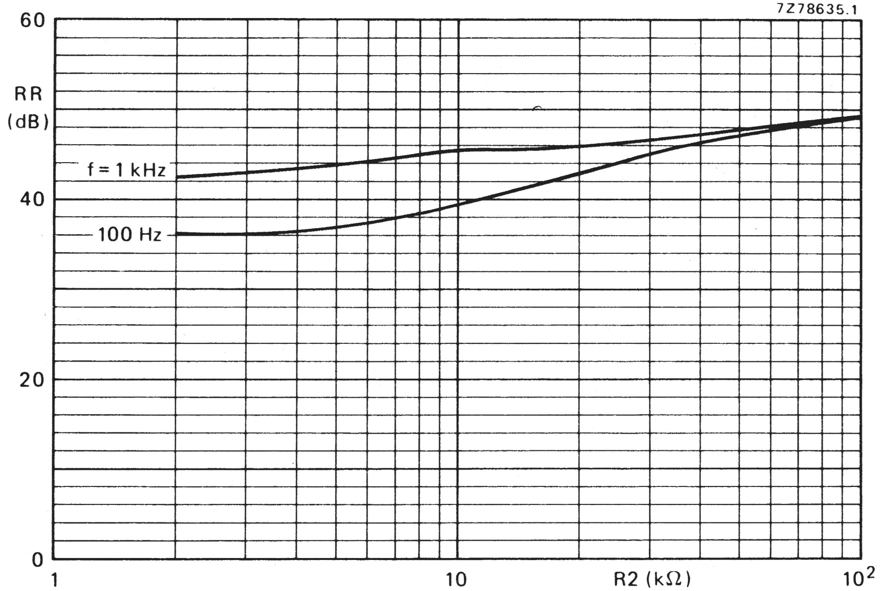


Fig. 10 Ripple rejection as a function of R2 (see Fig. 4); R_S = 0; typical values.

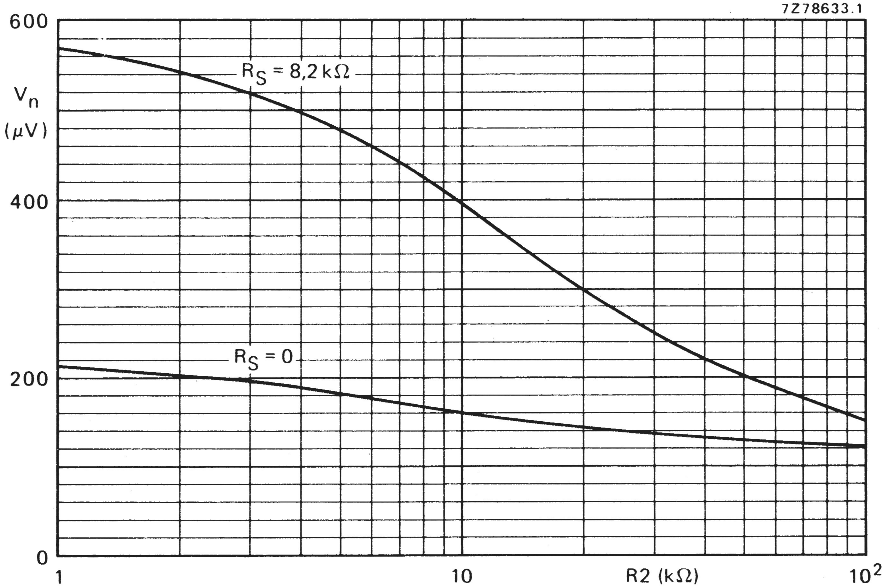


Fig. 11 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

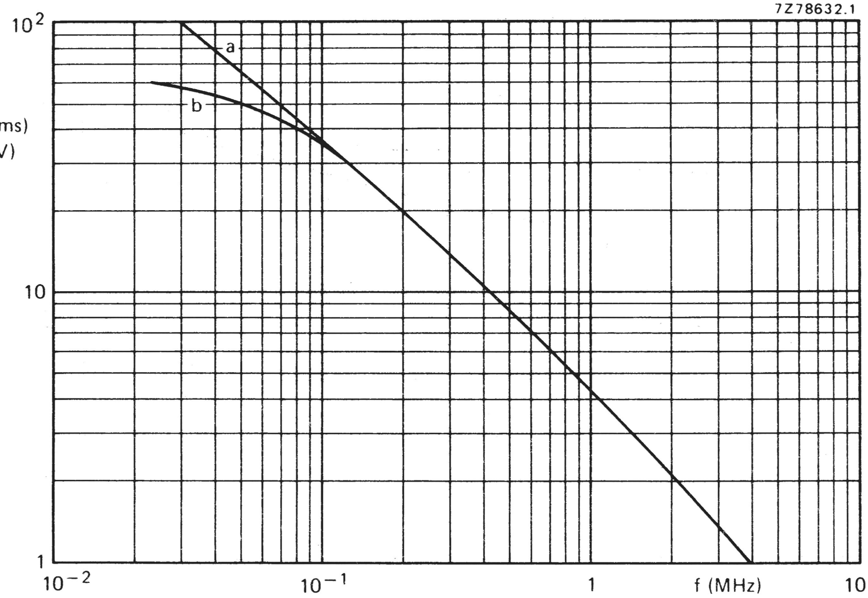


Fig. 12 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

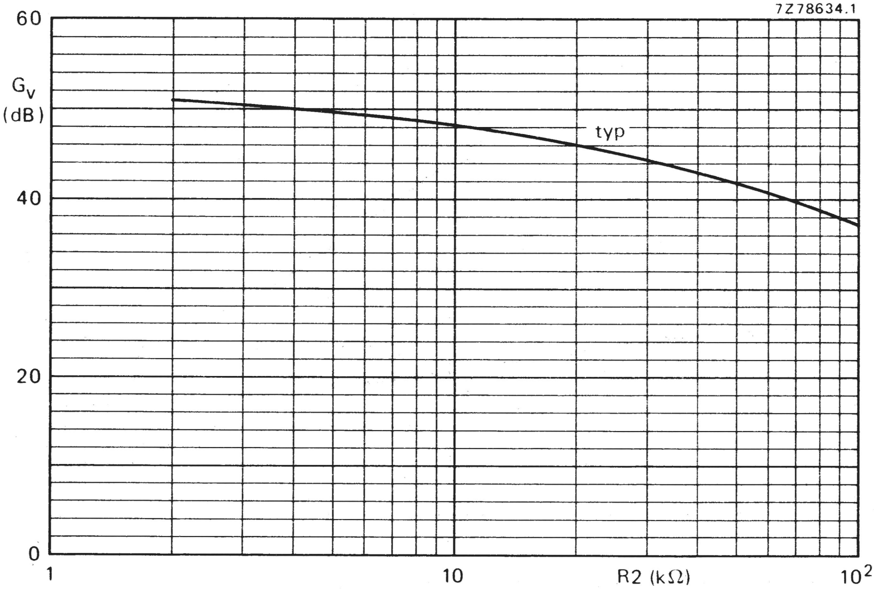


Fig. 13 Voltage gain as a function of R2 (see Fig. 4).

RECORDING/PLAYBACK AND 2 W AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1016 is a monolithic integrated audio power amplifier, preamplifier and A.L.C. circuit designed for applications in radio-recorders and recorders. The wide supply voltage range makes this circuit very suitable for d.c. and a.c. apparatus. The circuit incorporates the following features:

Features

- Power amplifier/monitor amplifier
- Preamplifier/record and playback amplifier
- Automatic Level Control (A.L.C.) circuit
- Voltage stabilizer
- Short-circuit (up to 12 V a.c.) and thermal protection.

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 18	V
Supply current; total quiescent at $V_P = 6$ V	I_{tot}	typ.	10	mA
Operating ambient temperature range	T_{amb}		−25 to 150	°C
Power amplifier				
Output power at $d_{tot} = 10\%$				
$V_P = 6$ V; $R_L = 4\ \Omega$	P_o	typ.	1	W
$V_P = 9$ V; $R_L = 4\ \Omega$	P_o	typ.	2	W
Closed loop gain	G_c	typ.	36	dB
Preamplifier				
Open loop gain	G_o	min.	70	dB
Minimum closed loop voltage gain	$G_{c\,min}$	min.	35	dB
Output voltage at $d_{tot} = 1\%$	V_o	min.	1	V
Automatic Level Control (A.L.C.)				
Gain variation for $\Delta V_i = 40$ dB	ΔG_v	typ.	2	dB
Stabilized supply voltage				
Output voltage	$V_{5\text{-}16}$	typ.	2,6	V

PACKAGE OUTLINE

16-lead DIL; plastic, with internal heat spreader (SOT-38WE-2).

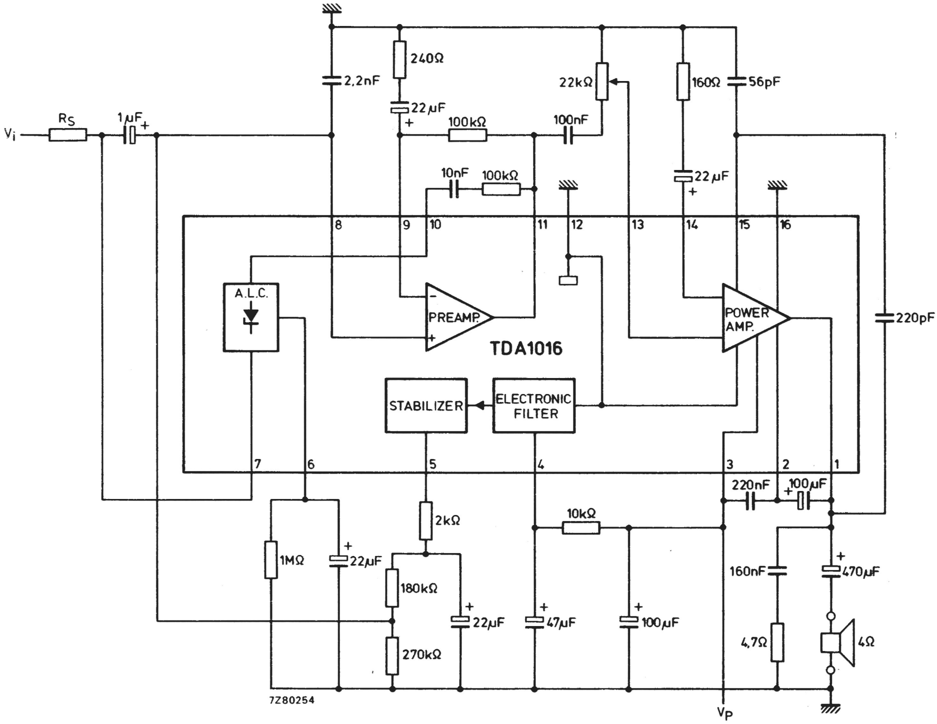

Vi
RS
1 μF
+
2,2nF
240Ω
22 μF
100kΩ
100nF
22kΩ
160Ω
56pF
10nF
100kΩ
22 μF
8
9
10
11
12
13
14
15
16
A.L.C.
PREAMP.
−
+
POWER AMP.
TDA1016
STABILIZER
ELECTRONIC FILTER
220pF
7
6
5
4
3
2
1
220nF
100μF
10kΩ
1MΩ
22μF
2kΩ
180kΩ
270kΩ
22μF
47μF
100μF
160nF
470μF
4,7Ω
4Ω
VP
7Z80254

Fig. 1 Block diagram with external components; also used as test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 3)	V_P	max.	18	V
Repetitive peak output current	I_{ORM}	max.	1	A
Non-repetitive peak output current (pin 1)	I_{OSM}	max.	2	A
Total power dissipation	see derating curve Fig. 2			
A.C. short-circuit duration of load during sinewave drive; V_P = 12 V	t_{sc}	max.	100	hours
Crystal temperature	T_c	max.	150	°C
Storage temperature range	T_{stg}	−55 to + 150		°C
Operating ambient temperature range	T_{amb}	−25 to + 150		°C

THERMAL RESISTANCE

The power derating curve (Fig. 2) is based on the following data

From junction to ambient	$R_{th\,j\text{-}a}$	=	55	K/W

DEVELOPMENT SAMPLE DATA

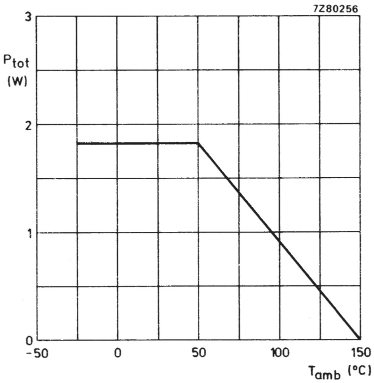


Fig. 2 Power derating curve.

CHARACTERISTICS

$V_P = 6$ V; $R_L = 4\ \Omega$; f = 1 kHz; $T_{amb} = 25\ ^oC$; measured in test circuit Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 3)					
Supply voltage	V_P	3,6	6	18	V
Supply current; total quiescent at $V_P = 6$ V	I_{tot}	–	10	–	mA
Power amplifier					
Output power at $d_{tot} = 10\%$*					
$V_P = 6$ V	P_o	–	1	–	W
$V_P = 9$ V	P_o	–	2	–	W
Closed loop voltage gain	G_c	–	36	–	dB
Total harmonic distortion at $P_o = 0{,}5$ W	d_{tot}	–	–	1	%
Input impedance	$\lvert Z_i \rvert$	0,5	–	–	MΩ
Ripple rejection at f = 100 Hz	RR	40	50	–	dB
Noise output voltage (r.m.s. value) $R_S = 0\ \Omega$; B = 60 Hz to 15 kHz	$V_{n(rms)}$	–	90	200	μV
Noise output voltage at 500 kHz $R_S = 0\ \Omega$; B = 5 kHz	V_n	–	8	–	μV
Preamplifier					
Open loop voltage gain at f = 10 kHz	G_o	70	–	–	dB
Closed loop voltage gain	G_c	–	52	–	dB
Minimum closed loop voltage gain (when changing R_f)	$G_{c\ min}$	35	–	–	dB
Output voltage at $d_{tot} = 1\%$	V_o	1	–	–	V
Output voltage with A.L.C. $V_i = 2$ mV	V_o	–	0,5	–	V
Total harmonic distortion with A.L.C.					
$V_i = 2$ mV	d_{tot}	–	–	1	%
$V_i = 360$ mV	d_{tot}	–	–	3	%
Signal-to-noise ratio related to $V_i = 1{,}2$ mV; $R_S = 1\ k\Omega$; B = 60 Hz to 15 kHz	S/N	–	60	–	dB
Input impedance	$\lvert Z_i \rvert$	100	–	–	kΩ
Ripple rejection at f = 100 Hz; $R_S = 0\ \Omega$	RR	50	54	–	dB
Output impedance **	$\lvert Z_o \rvert$	–	–	50	Ω

---

* Measured with an ideal coupling capacitor connected to the speaker load.

** I_P must not exceed 1,5 mA.

DEVELOPMENT SAMPLE DATA

parameter	symbol	min.	typ.	max.	unit
Automatic Level Control (A.L.C.) (see Fig. 3)					
Gain variation for ΔV_i = 40 dB	ΔG_v	—	2	3	dB
Limiting time*	t_l	—	—	50	ms
Level setting time*	t_s	—	—	50	ms
Recovery time*	t_r	—	100	—	s
Voltage stabilizer					
Output voltage	$V_{11\text{-}15}$	—	2,6	—	V
Load current	I_{11}	—	—	1,5	mA
Ripple rejection at f = 100 Hz	RR	40	—	—	dB

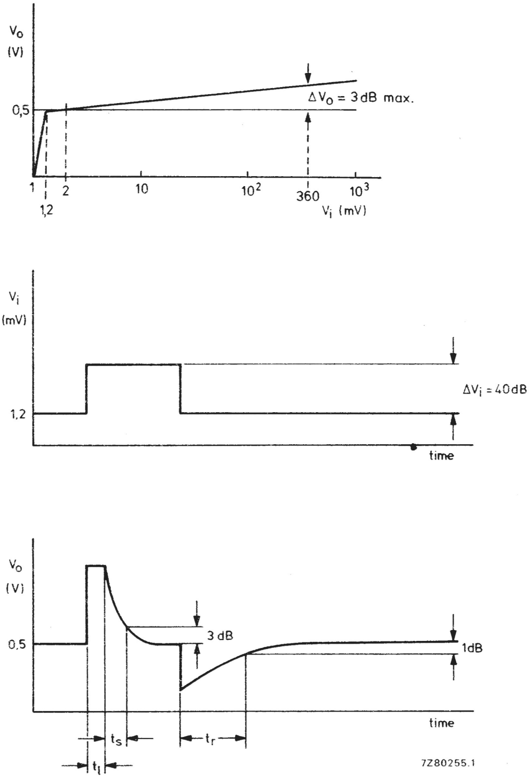


Fig. 3 Typical A.L.C. curve with R_S = 10 kΩ.

* At ΔV_i = 40 dB with respect to V_i = 1,2 mV.

12 W CAR RADIO POWER AMPLIFIER

The TDA1020 is a monolithic integrated 12 W audio amplifier in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a car radio amplifier. At a supply voltage of V_P = 14,4 V, an output power of 7 W can be delivered into a 4 Ω load and 12 W into 2 Ω.

To avoid interferences and car ignition signals coming from the supply lines into the IC, frequency limiting is used beyond the audio spectrum in the preamplifier and the power amplifier.

The maximum supply voltage of 18 V makes the IC also suitable for mains-fed radio receivers, tape recorders or record players. However, if the supply voltage is increased above 18 V ($<$ 45 V), the device will not be damaged (load dump protected). Also a short-circuiting of the output to ground (a.c.) will not destroy the device. Thermal protection is built-in. As a special feature, the circuit has a low stand-by current possibility.

The TDA1020 is pin-to-pin compatible with the TDA1010.

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 18	V
Repetitive peak output current	I_{ORM}	$<$	4	A
Output power at d_{tot} = 10% (with bootstrap)				
V_P = 14,4 V; R_L = 2 Ω	P_o	$>$ typ.	10 12	W W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	7	W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,5	W
Output power at d_{tot} = 10% (without bootstrap)				
V_P = 14,4 V; R_L = 4 Ω	P_o	$>$	4,5	W
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	typ.	40	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	40	kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	30	mA
Stand-by current	I_{sb}	$<$	1	mA
Storage temperature range	T_{stg}		−55 to + 150	°C
Crystal temperature	T_c	max.	150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

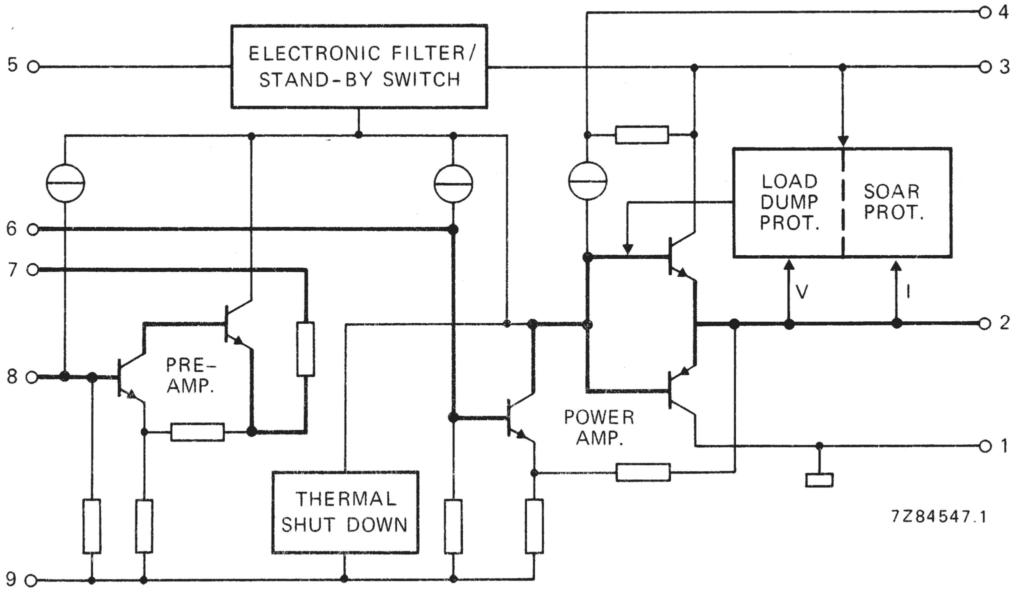

5
ELECTRONIC FILTER/
STAND-BY SWITCH
4
3
LOAD
DUMP
PROT.
SOAR
PROT.
6
7
V
I
2
8
PRE-
AMP.
POWER
AMP.
1
THERMAL
SHUT DOWN
7Z84547.1
9

Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

PINNING

1. Negative supply (substrate)
2. Output power stage
3. Positive supply (V_P)
4. Bootstrap
5. Ripple rejection filter
6. Input power stage
7. Output preamplifier
8. Input preamplifier
9. Negative supply

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 3)	V_P	max.	18 V
Supply voltage; non-operating	V_P	max.	28 V
Supply voltage; load dump	V_P	max.	45 V
Non-repetitive peak output current	I_{OSM}	max.	6 A
Total power dissipation	see derating curves Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150 °C	
Crystal temperature	T_c	max.	150 °C
Short-circuit duration of load behind output electrolytic capacitor at 1 kHz sine-wave overdrive (10 dB); V_P = 14,4 V	t_{sc}	max.	100 hours

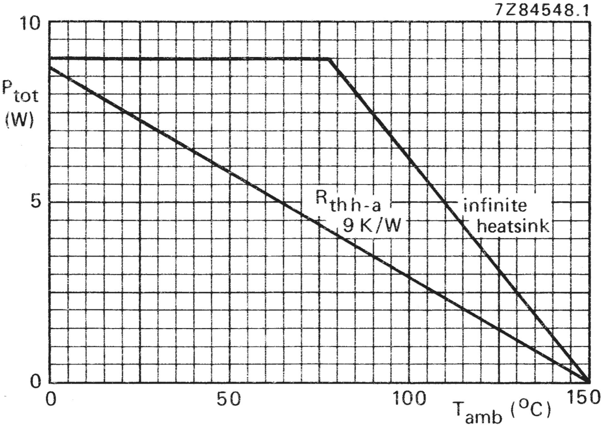


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 8 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

10 W in 2 Ω at V_P = 14,4 V
maximum sine-wave dissipation: 5,2 W
T_{amb} = 60 °C maximum

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150 - 60}{5,2} = 17,3\ \text{K/W}$$

Since $R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} = 8$ K/W, $R_{th\,h\text{-}a} = 17,3 - 8 \approx 9$ K/W.

D.C. CHARACTERISTICS

Supply voltage range (pin 3)	V_P		6 to 18	V
Repetitive peak output current	I_{ORM}	<	4	A
Total quiescent current				
at $V_P = 14,4$ V	I_{tot}	typ.	30	mA
at $V_P = 18$ V	I_{tot}	typ.	40	mA

A.C. CHARACTERISTICS

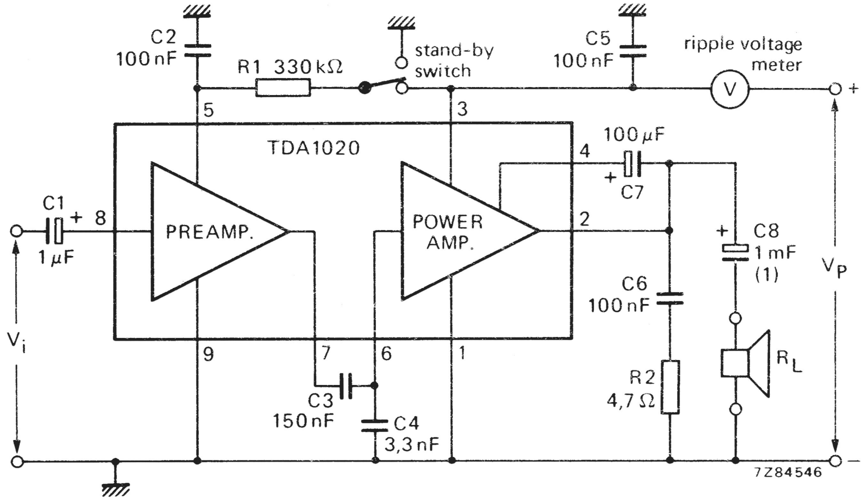
$T_{amb} = 25\ ^{o}C$; $V_P = 14,4$ V; $R_L = 4\ \Omega$; f = 1 kHz; unless otherwise specified; see also Fig. 3

Output power at $d_{tot} = 10\%$; with bootstrap (note 1)				
$V_P = 14,4$ V; $R_L = 2\ \Omega$	P_o	>	10	W
		typ.	12	W
$V_P = 14,4$ V; $R_L = 4\ \Omega$	P_o	>	6	W
		typ.	7	W
$V_P = 14,4$ V; $R_L = 8\ \Omega$	P_o	typ.	3,5	W
Output power at $d_{tot} = 1\%$; with bootstrap (note 1)				
$V_P = 14,4$ V; $R_L = 2\ \Omega$	P_o	typ.	9,5	W
$V_P = 14,4$ V; $R_L = 4\ \Omega$	P_o	typ.	6	W
$V_P = 14,4$ V; $R_L = 8\ \Omega$	P_o	typ.	3	W
Output voltage (r.m.s. value)				
$R_L = 1\ k\Omega$; $d_{tot} = 0,5\%$	$V_{o(rms)}$	typ.	5	V
Output power at $d_{tot} = 10\%$; without bootstrap	P_o	>	4,5	W
Voltage gain				
preamplifier (note 2)	G_{v1}	typ.	17,7	dB
			16,7 to 18,7	dB
power amplifier	G_{v2}	typ.	29,5	dB
			28,5 to 30,5	dB
total amplifier	$G_{v\ tot}$	typ.	47	dB
			46,2 to 48,2	dB
Input impedance				
preamplifier	$\lvert Z_i \rvert$	typ.	40	kΩ
			28 to 52	kΩ
power amplifier	$\lvert Z_i \rvert$	typ.	40	kΩ
			28 to 52	kΩ
Output impedance				
preamplifier	$\lvert Z_o \rvert$	typ.	2,0	kΩ
			1,4 to 2,6	kΩ
power amplifier	$\lvert Z_o \rvert$	typ.	50	mΩ
Output voltage (r.m.s. value) at $d_{tot} = 1\%$				
preamplifier (note 2)	$V_{o(rms)}$	>	1	V
		typ.	1,5	V
Frequency response	B		50 Hz to 25	kHz
Noise output voltage (r.m.s. value; note 3)				
$R_S = 0\ \Omega$	$V_{n(rms)}$	typ.	0,3	mV
		<	0,5	mV
$R_S = 8,2\ k\Omega$	$V_{n(rms)}$	typ.	0,5	mV
		<	1,0	mV

Ripple rejection (note 4) at f = 100 Hz; C2 = 1 μF	RR	typ.	44 dB
at f = 1 kHz to 10 kHz	RR	> typ.	48 dB 54 dB
Bootstrap current at onset of clipping (pin 4) R_L = 4 Ω and 2 Ω	I_4	typ.	40 mA
Stand-by current (note 5)	I_{sb}	<	1 mA
Crystal temperature for −3 dB gain	T_c	>	150 °C

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 40 kΩ.
3. Measured according to IEC curve-A.
4. Maximum ripple amplitude is 2 V; input is short-circuited.
5. Total current when disconnecting pin 5 or short-circuited to ground (pin 9).
6. The tab must be electrically floating or connected to the substrate (pin 9).


C2
100 nF
R1 330 kΩ
stand-by
switch
C5
100 nF
ripple voltage
meter
V
+
5
3
TDA1020
4
100 μF
+
C7
C1
+
8
1 μF
PREAMP.
POWER
AMP.
2
+
C8
1 mF
(1)
V_P
V_i
C6
100 nF
9
7
6
1
R_L
R2
4,7 Ω
C3
150 nF
C4
3,3 nF
−
7Z84546

(1) With R_L = 2 Ω, preferred value of C8 = 2200 μF.

Fig. 3 Test circuit.

SIGNAL-SOURCES SWITCH

The TDA1028 is a quadruple operational amplifier connected as an impedance converter. Each amplifier has 2 switchable inputs which are protected by clamping diodes. The input currents are independent of the switch position and the outputs are short-circuit protected.

The device is intended as an electronic four-channel signal-sources switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 9)	V_P		6 to 23	V
Operating ambient temperature	T_{amb}		−30 to + 80	°C
Supply voltage (pin 9)	V_P	typ.	20	V
Current consumption (pins 4, 5, 12, 13 unloaded)	I_9	typ.	2,9	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Crosstalk	α	typ.	70	dB
Signal-to-noise ratio	S/N	typ.	120	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

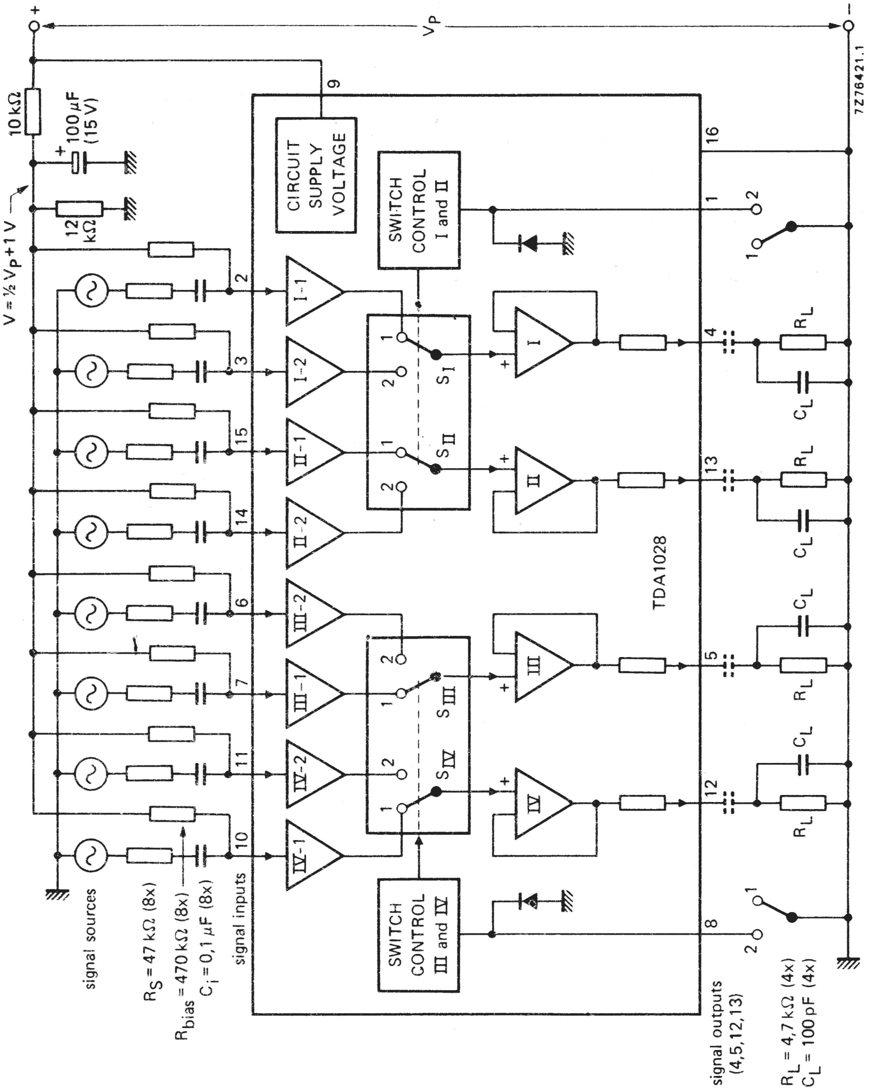

+
–
V_P
7Z76421.1
10 kΩ
100 µF (15 V)
+
12 kΩ
$V = ½ V_P + 1 V$
9
16
CIRCUIT SUPPLY VOLTAGE
SWITCH CONTROL I and II
SWITCH CONTROL III and IV
1
8
2
1
I-1
I-2
II-1
II-2
III-2
III-1
IV-2
IV-1
I
II
III
IV
S_I
S_{II}
S_{III}
S_{IV}
2
3
15
14
6
7
11
10
4
13
5
12
R_L
C_L
TDA1028
signal sources
$R_S = 47 kΩ$ (8x)
$R_{bias} = 470 kΩ$ (8x)
$C_i = 0,1 µF$ (8x)
signal inputs
signal outputs (4,5,12,13)
$R_L = 4,7 kΩ$ (4x)
$C_L = 100 pF$ (4x)

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	V_P	max.	23	V
Input voltages (pins 2, 3, 6, 7, 10, 11, 14, 15)	V_I $-V_I$	max. max.	V_P 0,5	 V
Switch control voltage (pin 1 and 8)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

$V_P = 20$ V; $T_{amb} = 25$ °C; unless otherwise specified

Current consumption without load; $I_{4; 5; 12; 13} = 0$	I_9	typ. 	2,9 1,6 to 4,2	mA mA
Supply voltage range	V_P		6 to 23	V

Signal inputs

Input offset voltage of switched-on inputs ($R_S < 1$ kΩ)	V_{io}	typ. <	2 10	mV mV
Input offset current of switched-on inputs	I_{io}	typ. <	20 200	nA nA
Input offset current of a switched-on input with respect to a non-switched-on input	I_{io}	typ. <	20 200	nA nA
Input bias current independent of switch position	I_i	typ. <	250 950	nA nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S < 10$ kΩ	SVRR	typ.	100	µV/V
Equivalent input noise voltage $R_S \leqslant 1$ kΩ; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	µV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at $R_S < 1$ kΩ; f = 1 kHz	α	typ.	100	dB

Signal amplifier

Voltage gain of a switched-on input at $I_{4; 5; 12; 13} = 0$; $R_L = \infty$	G_v	typ.	1	
Current gain of a switched-on amplifier	G_i	typ.	10^5	

CHARACTERISTICS (continued)

Signal outputs

Output resistance	R_o	typ.	400 Ω
Output current capability (pins 4, 5, 12 and 13)	$\pm I_o$	>	5 mA
Frequency limit of the output voltage at $V_{i(p\text{-}p)} = 1$ V; $R_S < 1$ kΩ; $R_L = 10$ MΩ; $C_L = 10$ pF	f	typ.	1,3 MHz
Slew rate (unity gain) $\Delta V_{4;\,5;\,12;\,13\text{-}16}/\Delta t$ at $R_L = 10$ MΩ; $C_L = 10$ pF	S	typ.	2 V/μs

Switch control

switched-on inputs	interconnected pins	control voltages	
		$V_{1\text{-}16}$	$V_{8\text{-}16}$
I-1, II-1	2-4, 15-13	H	–
I-2, II-2	3-4, 14-13	L	–
III-1, IV-1	7-5, 10-12	–	H
III-2, IV-2	6-5, 11-12	–	L

Control inputs (pins 1 and 8)

Required voltage			
HIGH	V_{SH}	>	3,3 V *
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	200 μA

---

* Or control inputs open; $R_{1\text{-}16}$, $R_{8\text{-}16} > 33$ MΩ.

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5	dB	
D.C. output voltage variation when switching the inputs (pins 4, 5, 12 and 13)	ΔV_o	typ. <	10 100	mV mV	
Total harmonic distortion over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01	%	
at V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02	%	
at V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03	%	
Output signal handling d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 5,3	V V	
Noise output voltage (unweighted) f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5	μV	
Noise output voltage (weighted) f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12	μV	
Amplitude response (pins 4, 5, 12 and 13) V_i = 5 V; f = 20 Hz to 20 kHz	ΔV_o	typ.	0,1	dB	*
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75	dB	**
Crosstalk between switched-on inputs and the outputs of the other channels; at f = 1 kHz	α	typ.	90	dB	**

---

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

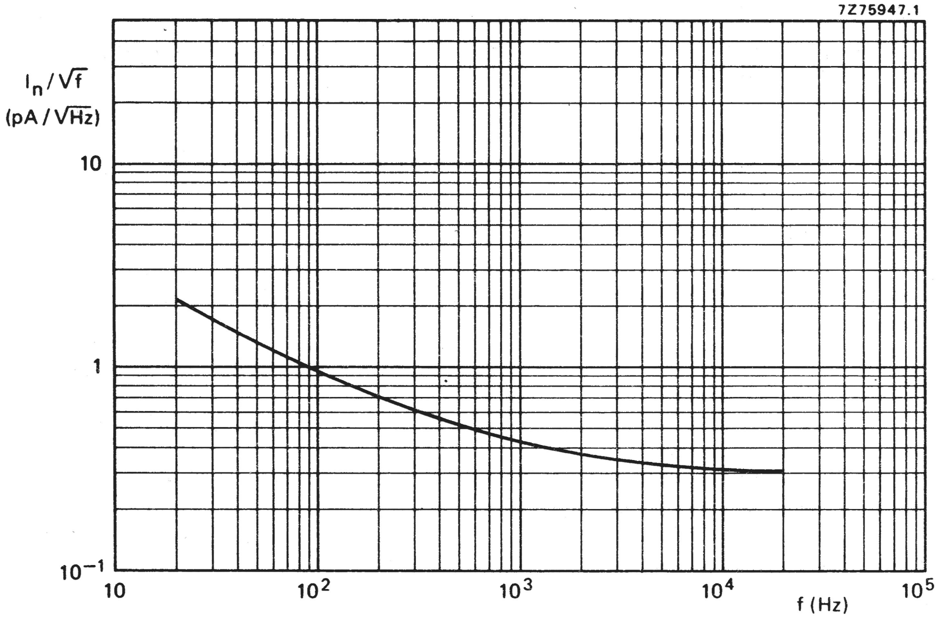


Fig. 2 Equivalent input noise current.

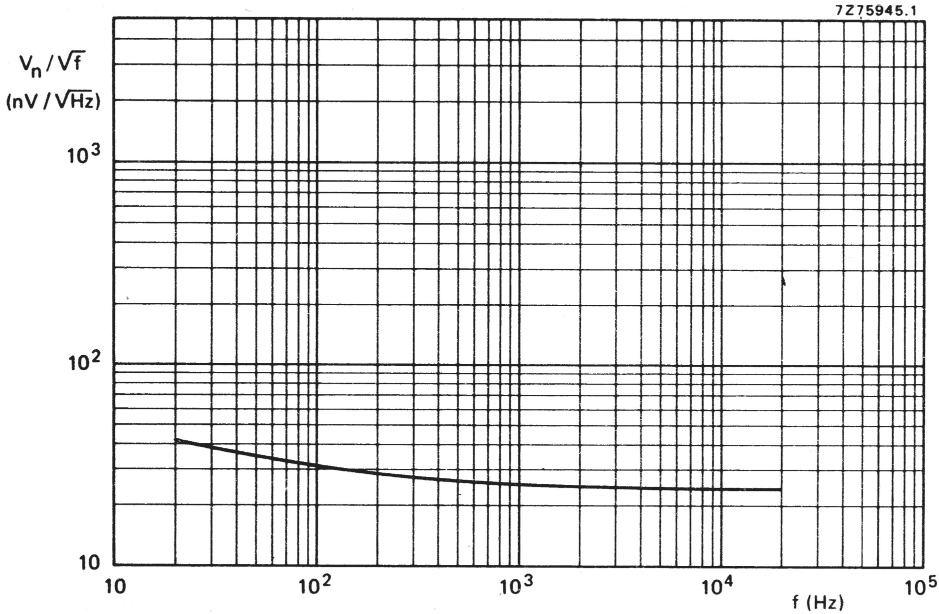


Fig. 3 Equivalent input noise voltage.

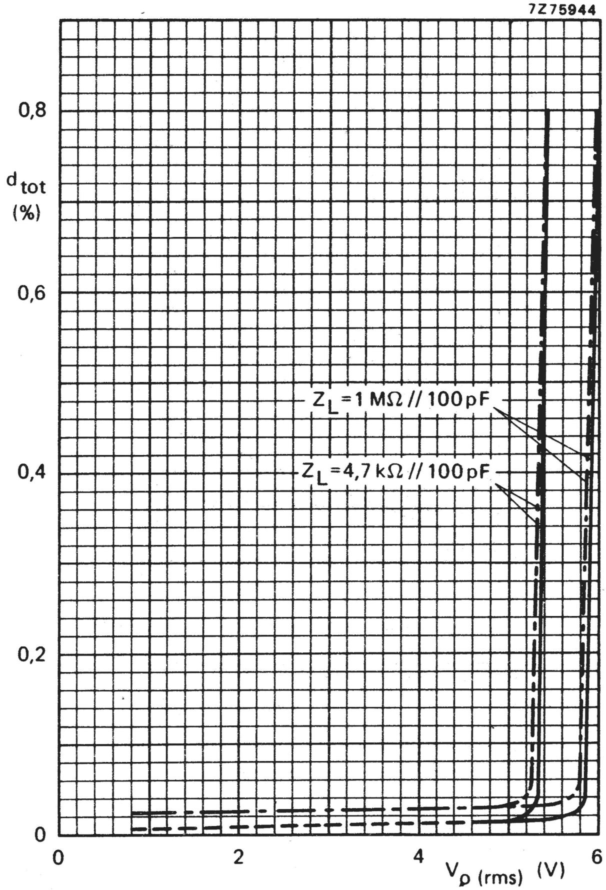


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — · — · f = 20 kHz.

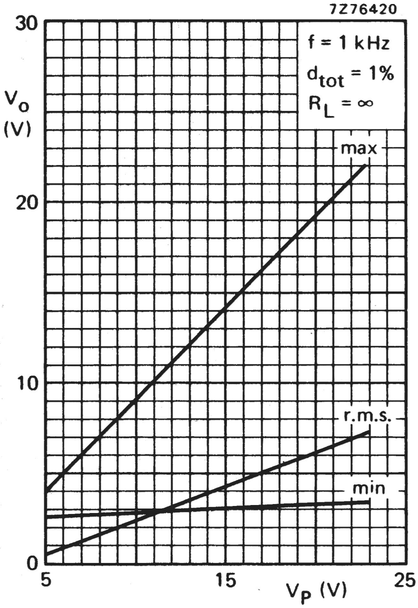


Fig. 5 Output voltage as a function of supply voltage.

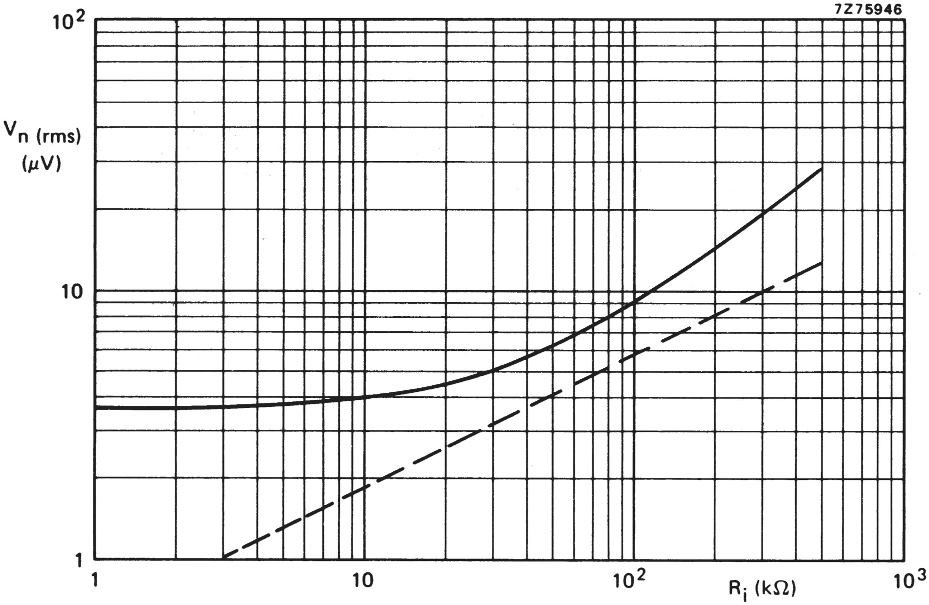


Fig. 6 Noise output voltage as a function of input resistance; $G_v = 1$; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

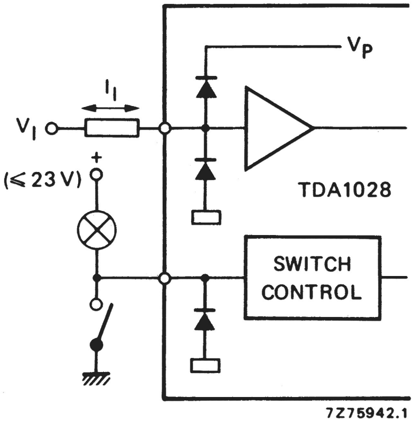


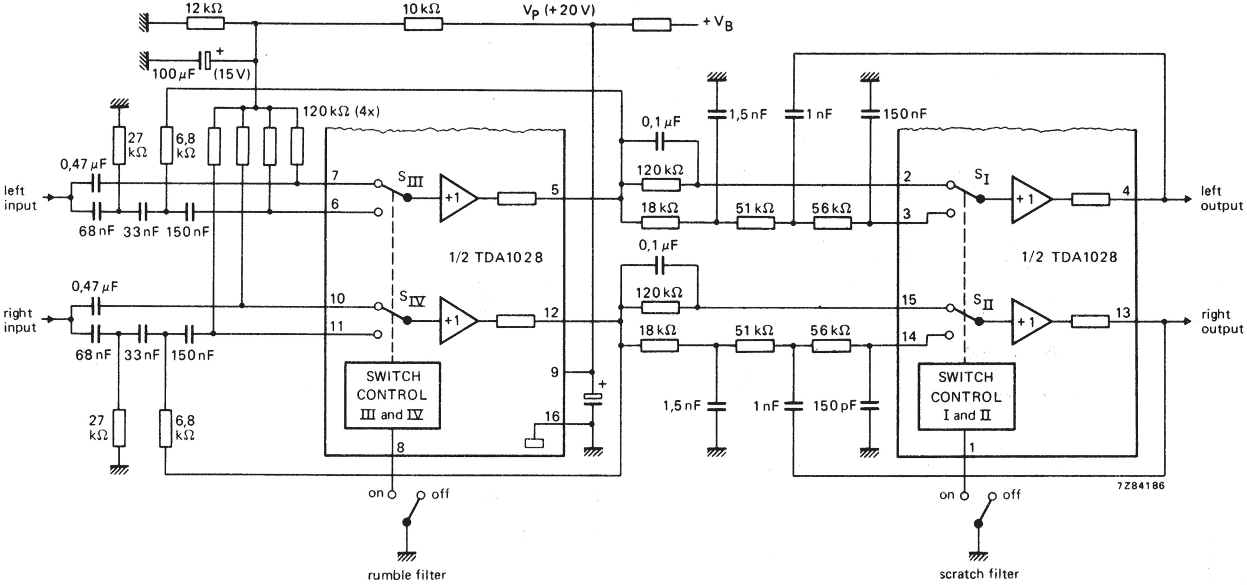
Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range.

Circuits with standby operation

The control inputs (pins 1 and 8) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1$ μA), as well as, when the supply voltage (pin 9) is switched off.



12 kΩ
10 kΩ
V_P (+20 V)
+V_B
100 μF
(15 V)
120 kΩ (4x)
27 kΩ
6,8 kΩ
0,47 μF
left input
68 nF
33 nF
150 nF
right input
7
6
10
11
5
12
9
16
8
S_III
S_IV
+1
1/2 TDA1028
SWITCH CONTROL III and IV
on
off
rumble filter
0,1 μF
120 kΩ
18 kΩ
1,5 nF
1 nF
150 nF
51 kΩ
56 kΩ
150 pF
2
3
15
14
4
13
1
S_I
S_II
SWITCH CONTROL I and II
scratch filter
left output
right output
7Z84186

Fig. 8 Typical application diagram for a switchable scratch/rumble filter.

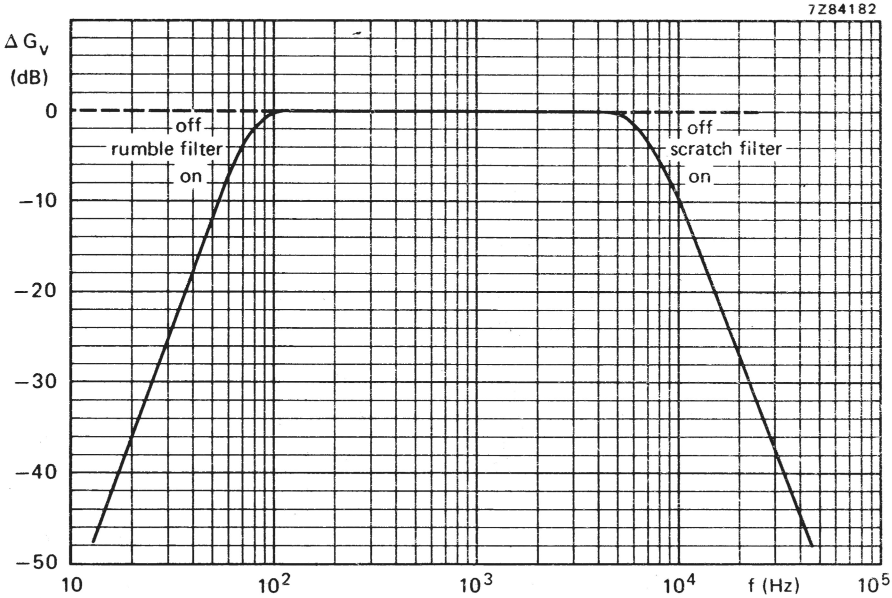


Fig. 9 Frequency response curves for scratch/rumble filters in Fig. 8.

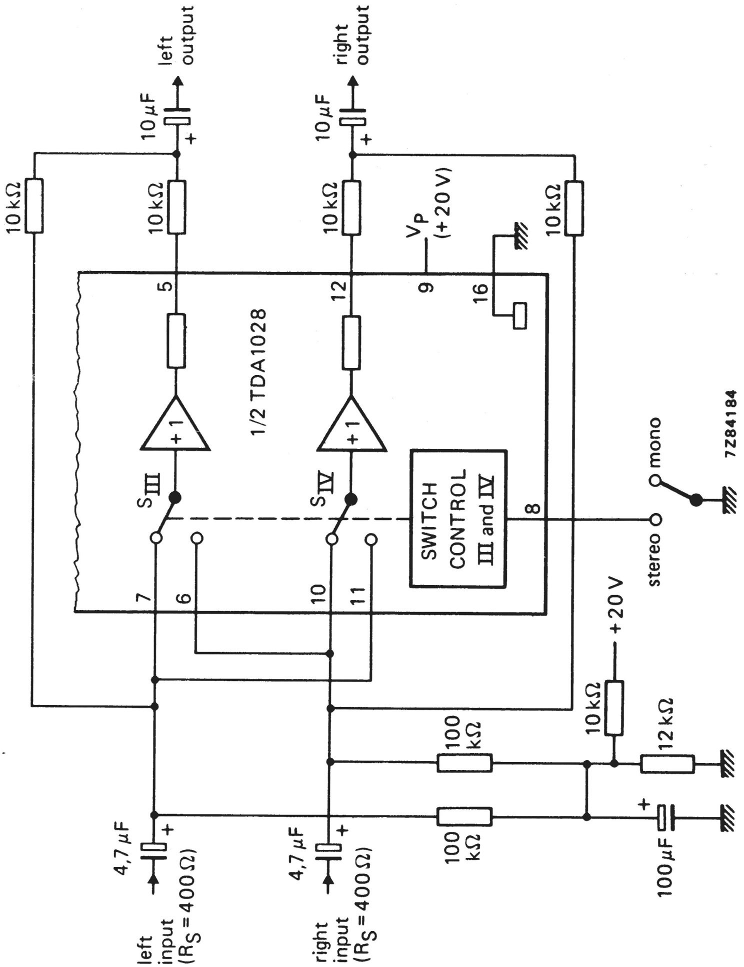

left output
10 μF
+
right output
10 μF
+
10 kΩ
10 kΩ
10 kΩ
10 kΩ
V_P
(+20 V)
5
12
9
16
1/2 TDA1028
+1
+1
S_{III}
S_{IV}
SWITCH CONTROL III and IV
8
7
6
10
11
stereo
mono
7Z84184
+20 V
10 kΩ
12 kΩ
100 kΩ
100 kΩ
100 μF
+
4,7 μF
+
left input (R_S = 400 Ω)
4,7 μF
+
right input (R_S = 400 Ω)

Fig. 10 Half of TDA1028 used as a mono/stereo switch.

SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P		6 to 23	V
Operating ambient temperature	T_{amb}		−30 to + 80	°C
Supply voltage (pin 14)	V_P	typ.	20	V
Current consumption	I_{14}	typ.	3,5	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Crosstalk	α	typ.	70	dB
Signal-to-noise ratio	S/N	typ.	120	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

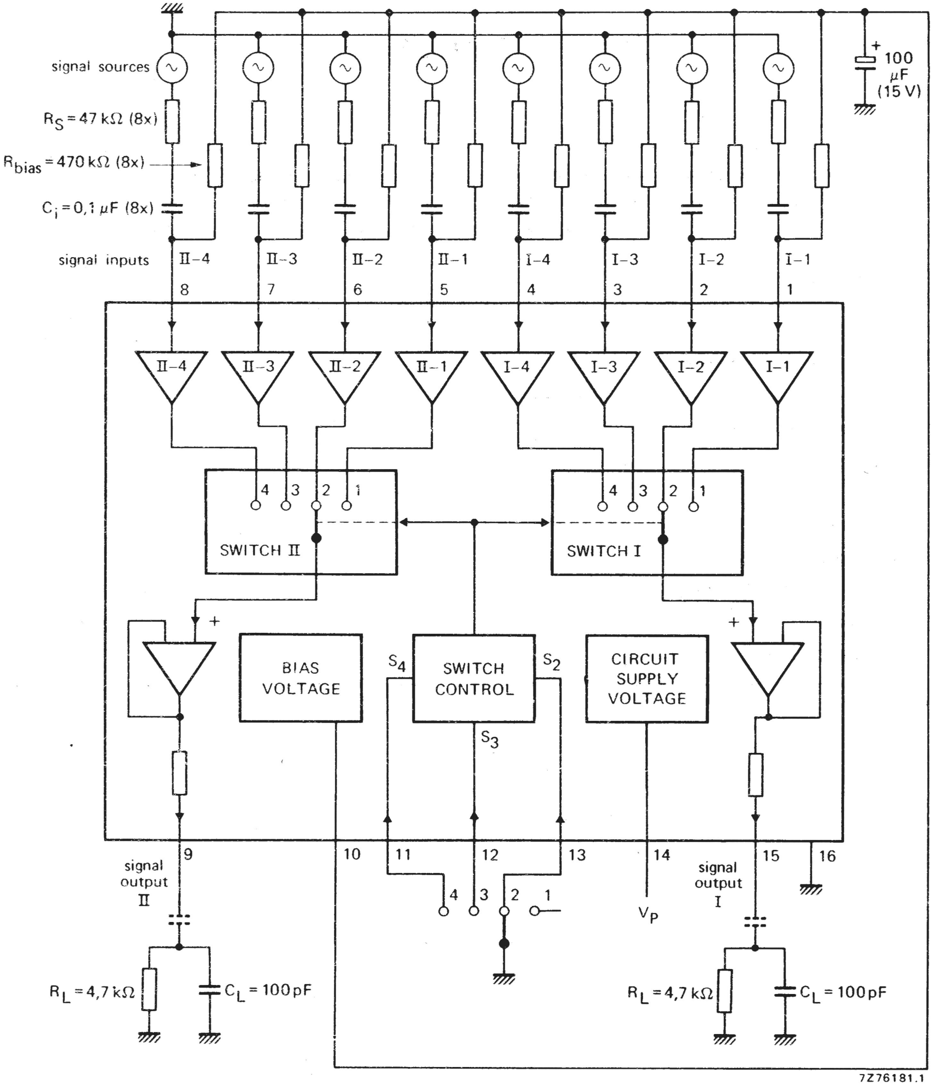

signal sources
RS = 47 kΩ (8x)
Rbias = 470 kΩ (8x)
Ci = 0,1 μF (8x)
signal inputs
II-4
II-3
II-2
II-1
I-4
I-3
I-2
I-1
8
7
6
5
4
3
2
1
100 μF (15 V)
+
SWITCH II
SWITCH I
4
3
2
1
BIAS VOLTAGE
SWITCH CONTROL
CIRCUIT SUPPLY VOLTAGE
S4
S2
S3
9
10
11
12
13
14
15
16
signal output II
signal output I
VP
RL = 4,7 kΩ
CL = 100 pF
RL = 4,7 kΩ
CL = 100 pF
7Z76181.1

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23	V
Input voltage (pins 1 to 8)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to +80	°C

CHARACTERISTICS

$V_P = 20$ V; $T_{amb} = 25$ °C; unless otherwise specified

Current consumption without load; $I_9 = I_{15} = 0$	I_{14}	typ.	3,5 2 to 5	mA mA
Supply voltage range (pin 14)	V_P		6 to 23	V

Signal inputs

Input offset voltage of switched-on inputs $R_S \leqslant 1$ kΩ	V_{io}	typ. <	2 10	mV mV
Input offset current of switched-on inputs	I_{io}	typ. <	20 200	nA nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ. <	20 200	nA nA
Input bias current independent of switch position	I_i	typ. <	250 950	nA nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ	SVRR	typ.	100	µV/V
Equivalent input noise voltage $R_S = 0$; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	µV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at $R_S = 1$ kΩ; f = 1 kHz	α	typ.	100	dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1
Current gain of a switched-on amplifier	G_i	typ.	10^5

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400 Ω
Output current capability at $V_P = 6$ to 23 V	$\pm I_9$; $\pm I_{15}$	typ.	5 mA
Frequency limit of the output voltage $V_{i(p\text{-}p)} = 1$ V; $R_S = 1$ kΩ; $R_L = 10$ MΩ; $C_L = 10$ pF	f	typ.	1,3 MHz
Slew rate (unity gain); $\Delta V_{9\text{-}16}/\Delta t$; $\Delta V_{15\text{-}16}/\Delta t$ $R_L = 10$ MΩ; $C_L = 10$ pF	S	typ.	2 V/μs

Bias voltage

D.C. output voltage	$V_{10\text{-}16}$	typ. 10,2 to	11 V * 11,8 V
Output resistance	$R_{10\text{-}16}$	typ.	8,2 kΩ

Switch control

switched-on inputs	interconnected pins	control voltages		
		$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1,5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage			
HIGH	V_{SH}	>	3,3 V **
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	250 μA

---

* $V_{10\text{-}16}$ is typically $0,5 \cdot V_{14\text{-}16} + 1,5 \cdot V_{BE}$.

** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5	dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ. <	10 100	mV mV
Total harmonic distortion				
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01	%
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02	%
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03	%
Output signal handling d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 5,3	V V
Noise output voltage (unweighted) f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5	μV
Noise output voltage (weighted) f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12	μV
Amplitude response V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1	dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75	dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90	dB **

---

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

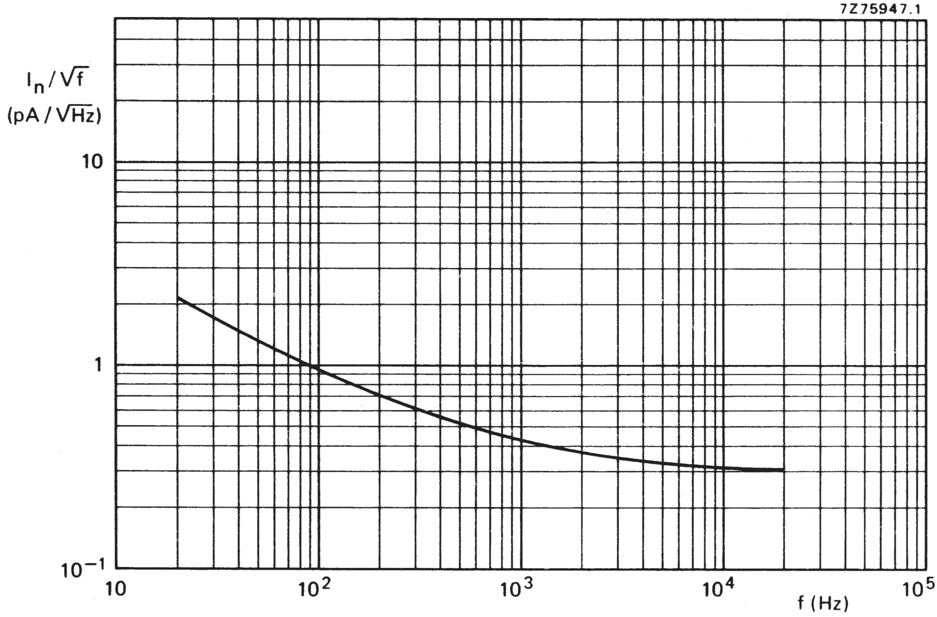


Fig. 2 Equivalent input noise current.

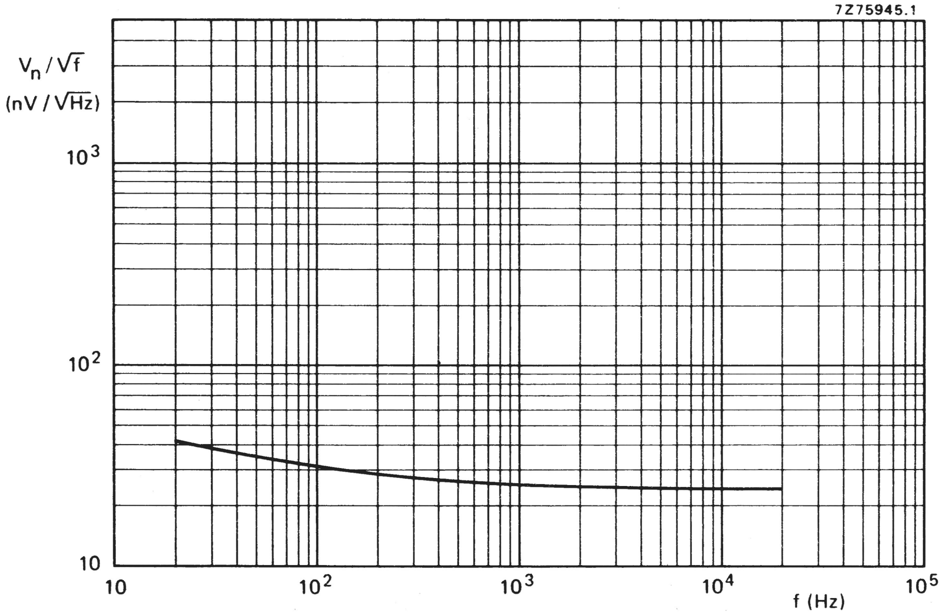


Fig. 3 Equivalent input noise voltage.

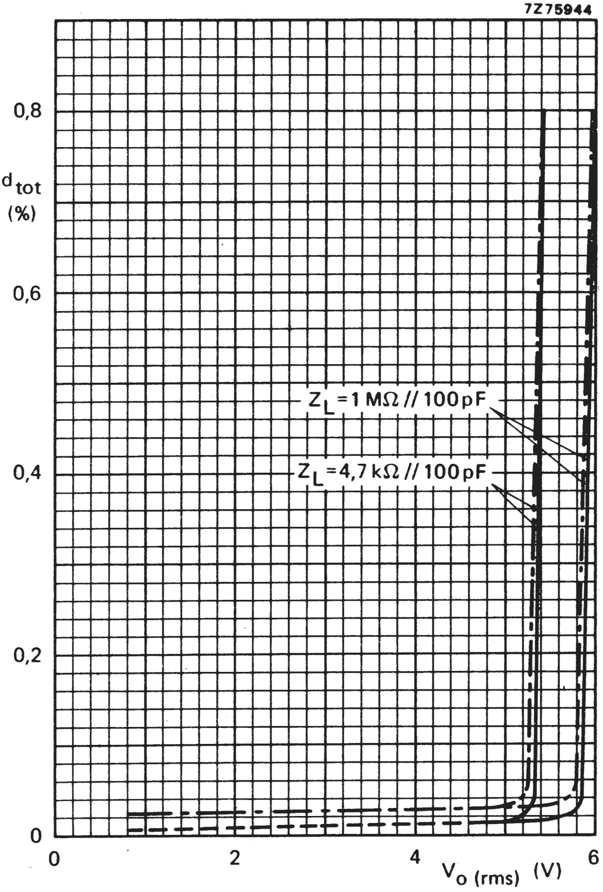


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — - — - f = 20 kHz.

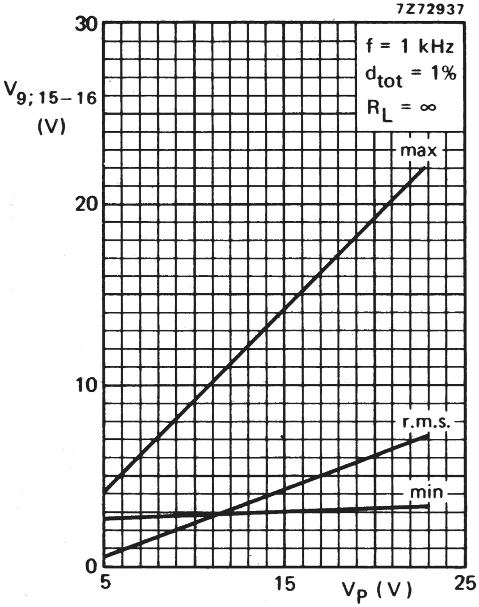


Fig. 5 Output voltage as a function of supply voltage.

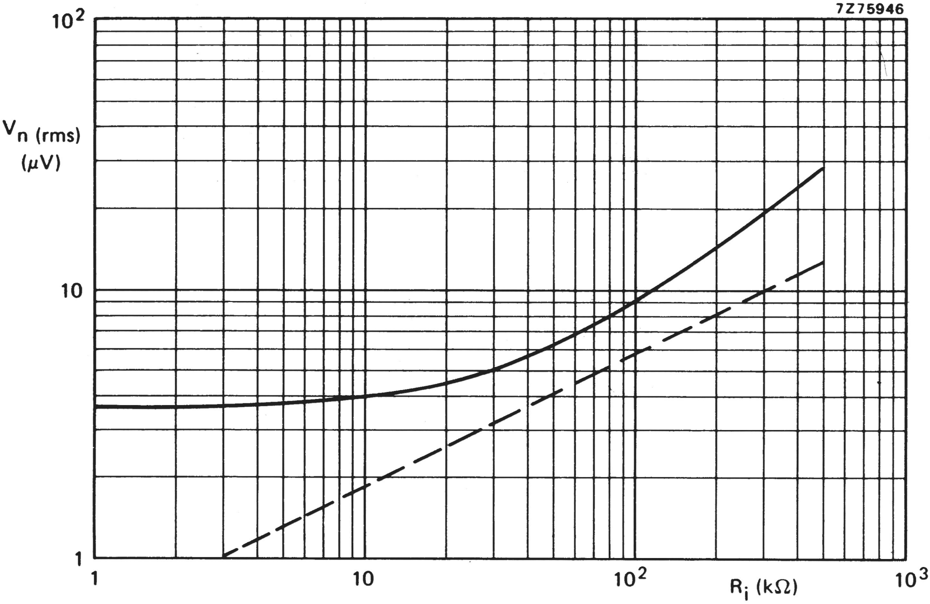


Fig. 6 Noise output voltage as a function of input resistance; $G_v = 1$; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

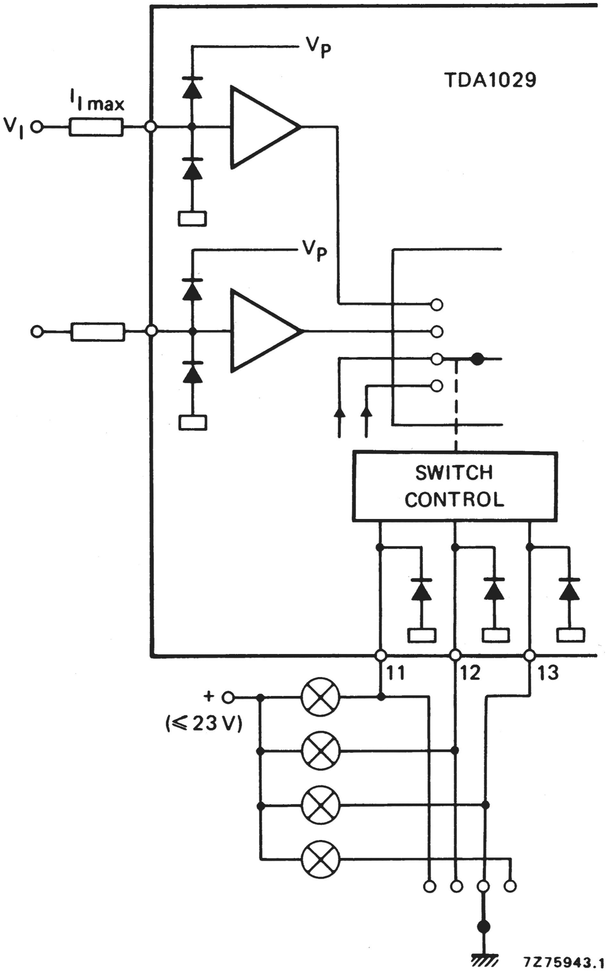

TDA1029
V_P
V_P
I_I max
V_I
SWITCH CONTROL
11
12
13
+
(≤ 23 V)
7Z75943.1

Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leqslant 20$ V ($I_{SH} \leqslant 1$ μA), as well as, when the supply voltage (pin 14) is switched off.

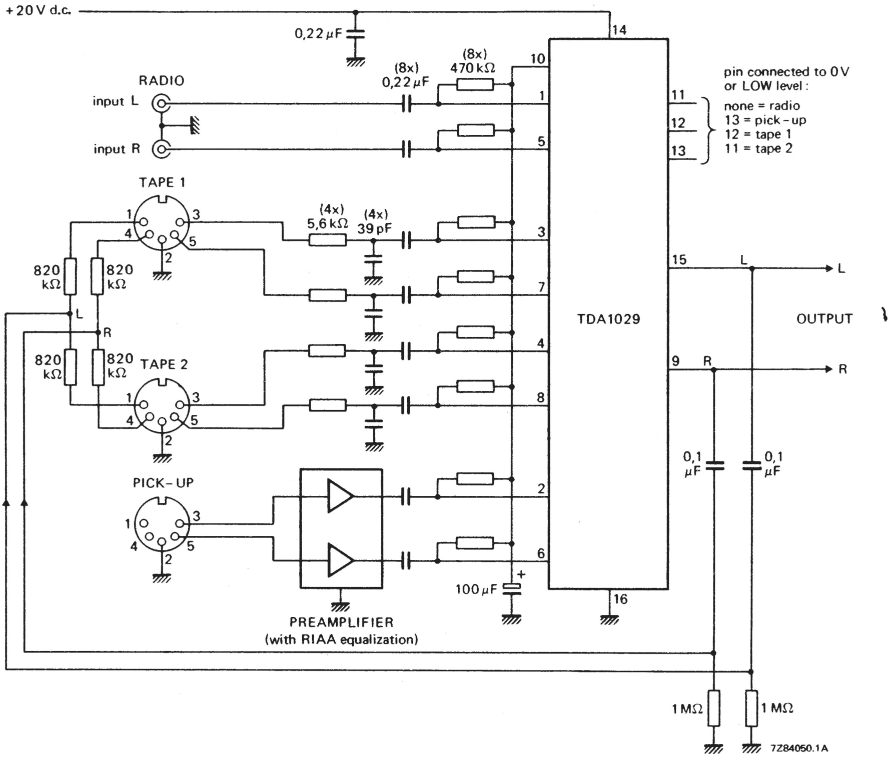

+20 V d.c.
0,22 µF
RADIO
input L
input R
(8x)
0,22 µF
(8x)
470 kΩ
TAPE 1
(4x)
5,6 kΩ
(4x)
39 pF
820 kΩ
820 kΩ
820 kΩ
820 kΩ
L
R
TAPE 2
PICK-UP
PREAMPLIFIER
(with RIAA equalization)
100 µF
TDA1029
14
10
1
5
3
7
4
8
2
6
16
11
12
13
15
9
pin connected to 0 V or LOW level:
none = radio
13 = pick-up
12 = tape 1
11 = tape 2
OUTPUT
L
R
0,1 µF
0,1 µF
1 MΩ
1 MΩ
7Z84050.1A

Fig. 8 TDA1029 connected as a four input stereo source selector.

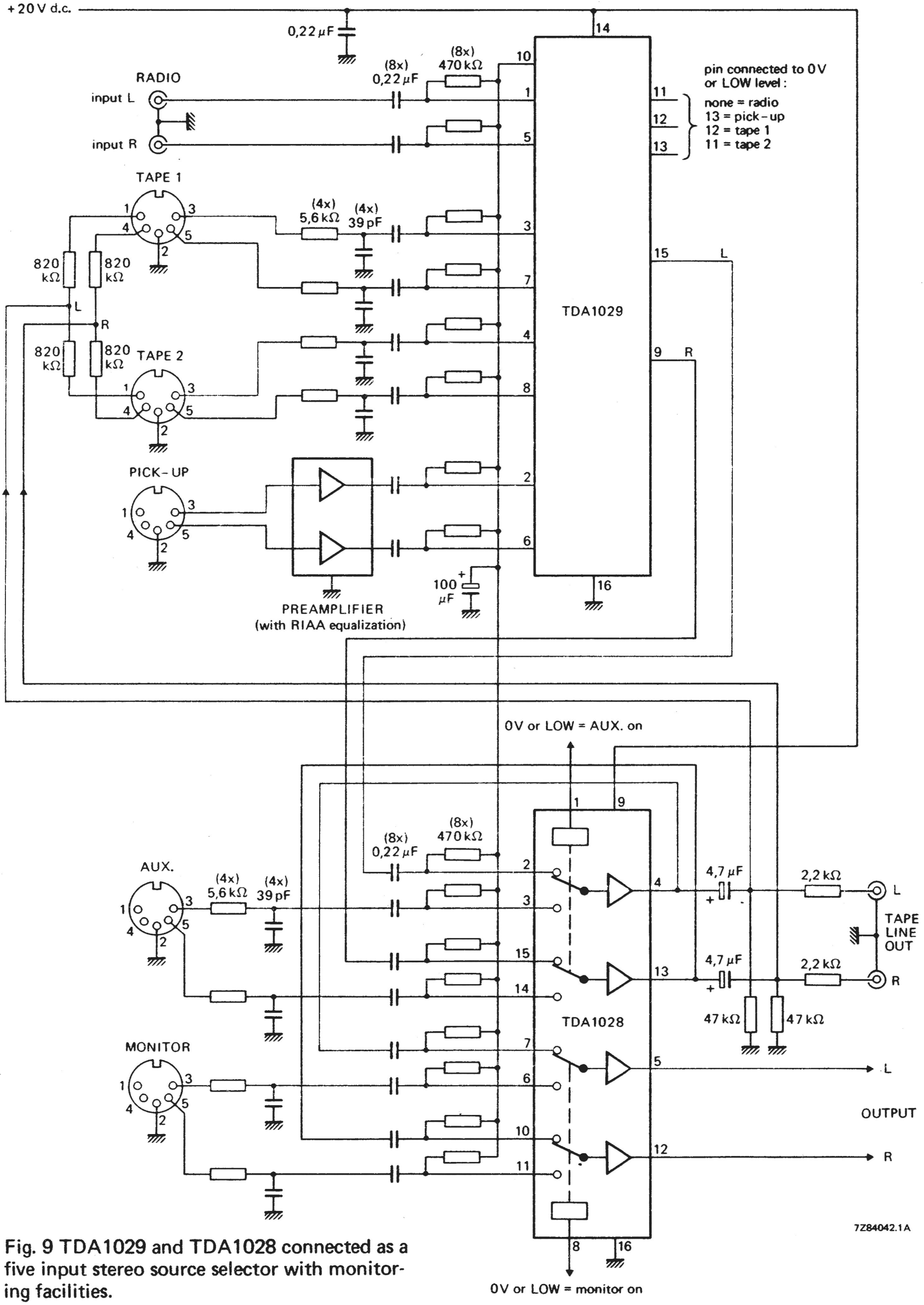

+20 V d.c.
0,22 μF
14
(8x) 0,22 μF
(8x) 470 kΩ
10
RADIO
input L
input R
1
5
pin connected to 0 V or LOW level:
11
12
13
none = radio
13 = pick-up
12 = tape 1
11 = tape 2
TAPE 1
(4x) 5,6 kΩ
(4x) 39 pF
3
7
4
8
820 kΩ
L
R
TAPE 2
15
L
TDA1029
9
R
PICK-UP
2
6
100 μF
16
PREAMPLIFIER (with RIAA equalization)
0V or LOW = AUX. on
1
9
AUX.
MONITOR
(8x) 0,22 μF
(8x) 470 kΩ
(4x) 5,6 kΩ
(4x) 39 pF
2
3
15
14
7
6
10
11
4
13
5
12
4,7 μF
2,2 kΩ
47 kΩ
TAPE LINE OUT
L
R
TDA1028
OUTPUT
L
R
8
16
0V or LOW = monitor on
7Z84042.1A

Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

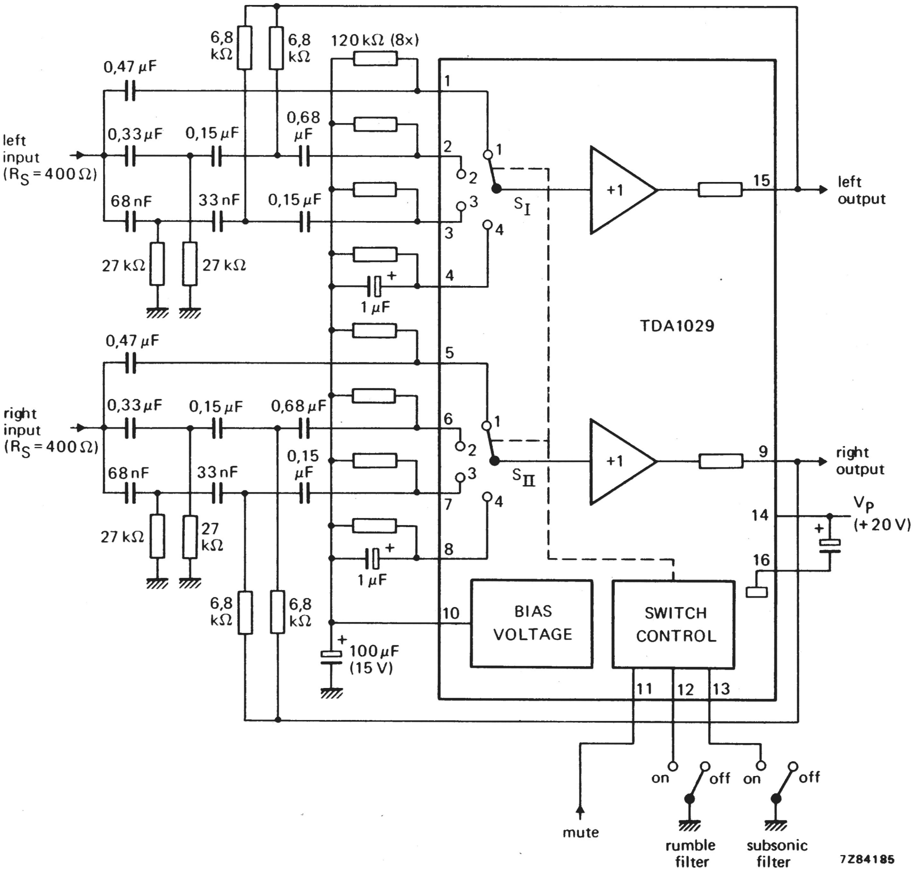

6,8 kΩ
6,8 kΩ
120 kΩ (8x)
0,47 μF
left input
(R_S = 400 Ω)
0,33 μF
0,15 μF
0,68 μF
68 nF
33 nF
0,15 μF
27 kΩ
27 kΩ
1 μF
1
2
3
4
1
2
3
4
S_I
+1
15
left output
TDA1029
0,47 μF
5
right input
(R_S = 400 Ω)
0,33 μF
0,15 μF
0,68 μF
6
1
2
3
4
S_II
+1
9
right output
68 nF
33 nF
0,15 μF
7
27 kΩ
27 kΩ
14
V_P (+20 V)
8
16
1 μF
6,8 kΩ
6,8 kΩ
10
BIAS VOLTAGE
SWITCH CONTROL
100 μF (15 V)
11
12
13
on
off
on
off
mute
rumble filter
subsonic filter
7Z84185

Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

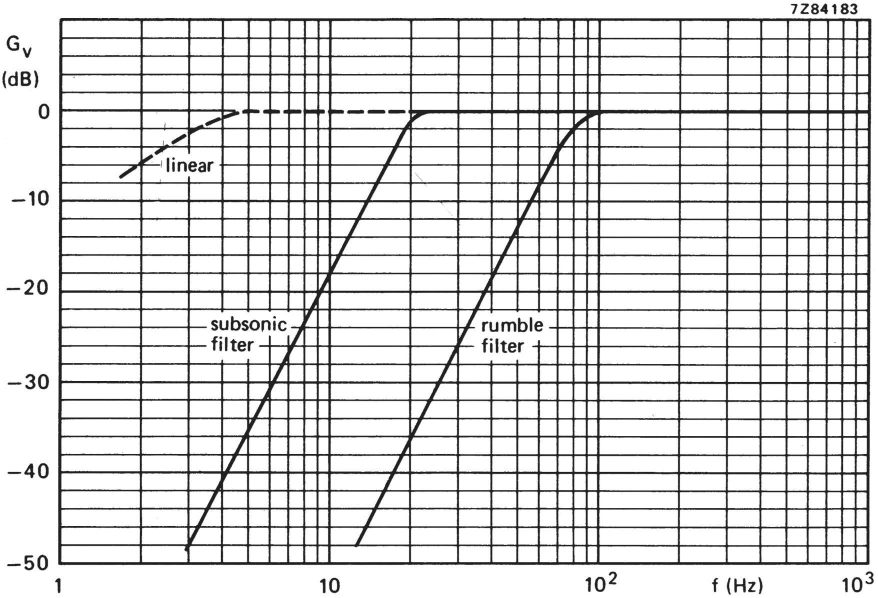


Fig. 11 Frequency response curves for the circuit of Fig. 10.

MOTOR SPEED REGULATOR WITH THERMAL SHUT-DOWN

The TDA1059B is a monolithic integrated circuit with a current limiter and with good thermal characteristics in a TO-126 plastic package for easy mounting. It is intended to regulate the speed of d.c. motors in record players, cassette recorders and car cassette recorders.

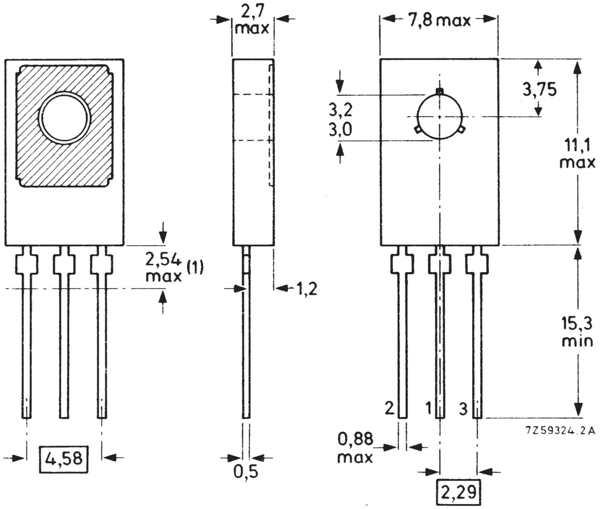
QUICK REFERENCE DATA

Supply voltage	$V_P = V_{2\text{-}1}$	typ.	9	V
			3,3 to 16	V
Internal reference voltage	V_{ref}	typ.	1,3	V
Drop-out voltage	$V_{3\text{-}1}$	typ.	1,8	V
Limited output current	I_{3lim}	typ.	0,6	A
Multiplication coefficient	k	typ.	9	

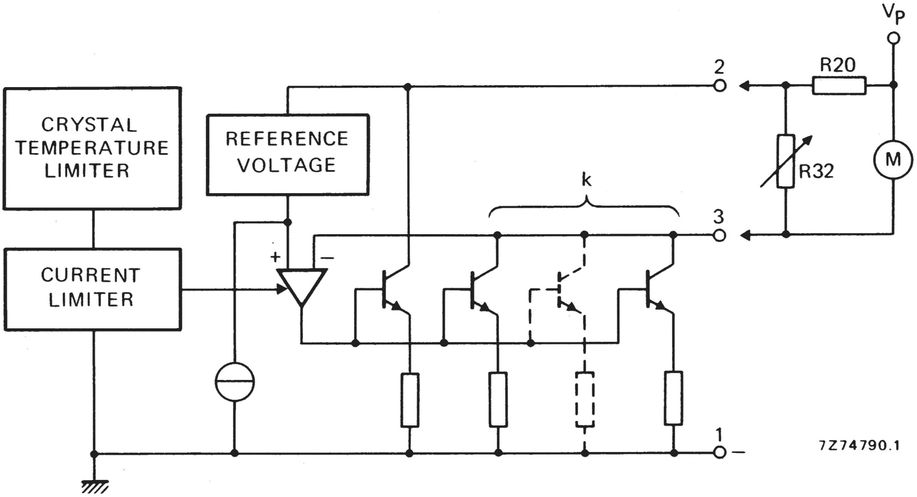
PACKAGE OUTLINE

Dimensions in mm

Fig. 1 TO-126 (SOT-32).
Pin 1 connected to metal part of mounting surface.



(1) Within this region the cross-section of the leads is uncontrolled.



CRYSTAL TEMPERATURE LIMITER
CURRENT LIMITER
REFERENCE VOLTAGE
+
−
k
2
3
1
−
VP
R20
R32
M
7Z74790.1

Fig. 2 Functional diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{2-1}$	max.	16 V
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature (see Fig. 3 and note)	T_{amb}	−25 to + 130	°C

THERMAL RESISTANCE

From junction to case	$R_{th\ j\text{-}c}$	=	10 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	100 K/W

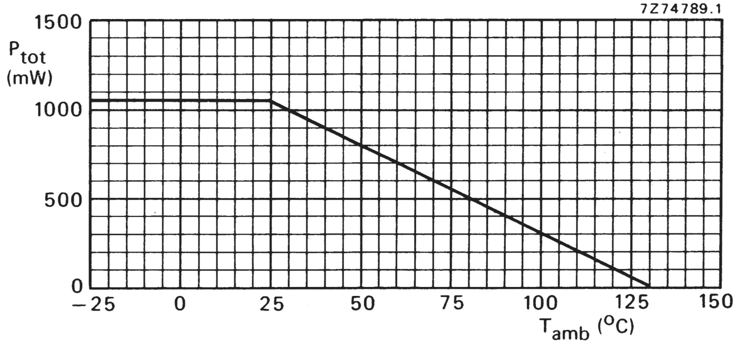


Fig. 3 Power derating curve.

Note
At ambient temperatures above 130 °C, the crystal temperature limiter decreases the internal power consumption.

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; R20 = 0; heatsink with R_{th} = 100 K/W and after thermal stabilization; unless otherwise specified; see test circuit Fig. 4.

		min.	typ.	max.	
Supply voltage	$V_P = V_{2\text{-}1}$	3,3	9	16	V
Internal reference voltage V_P = 3,3 V; I_3 = 80 mA	V_{ref}	1,24	1,3	1,36	V
Drop-out voltage I_3 = 80 mA; ΔV_{ref} = 5%	$V_{3\text{-}1}$	–	1,8	2,06	V
Quiescent current; I_3 = 0	I_q	1,8	2,3	2,8	mA
Limited output current*	I_{3lim}	0,3	0,6	1	A
Multiplication coefficient I_3 = 50 mA ± 10 mA	$k = \frac{\Delta I_3}{\Delta I_2}$	8,5	9	9,5	
Line regulation V_P = 3,3 to 16 V at I_3 = 50 mA					
reference voltage variation	$\frac{\Delta V_{ref}}{V_{ref}} / \Delta V_P$	–0,115	0	+ 0,115	%/V
multiplication coefficient variation I_3 = 50 ± 10 mA	$\frac{\Delta k}{k} / \Delta V_P$	–	0,86	–	%/V
input current variation; I_3 = 50 mA	$\frac{\Delta I_2}{\Delta V_P}$	–15	0	+ 20	µA/V
Load regulation					
reference voltage variation I_3 = 20 to 80 mA	$\frac{\Delta V_{ref}}{V_{ref}} / \Delta I_3$	0	19	38,5	%/A
multiplication coefficient variation I_3 = 30 ± 10 to 70 ± 10 mA	$\frac{\Delta k}{k} / \Delta I_3$	–0,075	0	+ 0,075	%/mA
Temperature coefficient I_3 = 50 mA; T_{amb} = –15 to + 65 °C					
reference voltage variation	$\frac{\Delta V_{ref}}{V_{ref}} / \Delta T_{amb}$	–0,03	0	+ 0,03	%/K
multiplication coefficient variation ΔI_3 = ± 10 mA	$\frac{\Delta k}{k} / \Delta T_{amb}$	–	0,008	–	%/K
input current variation	$\frac{\Delta I_2}{\Delta T_{amb}}$	–2	0	+ 2	µA/K

---

* If the motor is stopped by a mechanical brake, the current limitation is effective in the supply voltage range. If the motor is short-circuited, the TDA1059B will be damaged if the supply voltage is higher than 10 V due to parasitic oscillations.

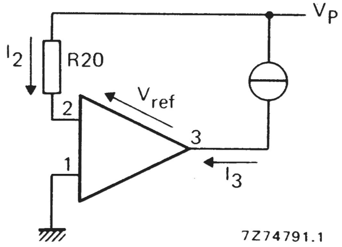
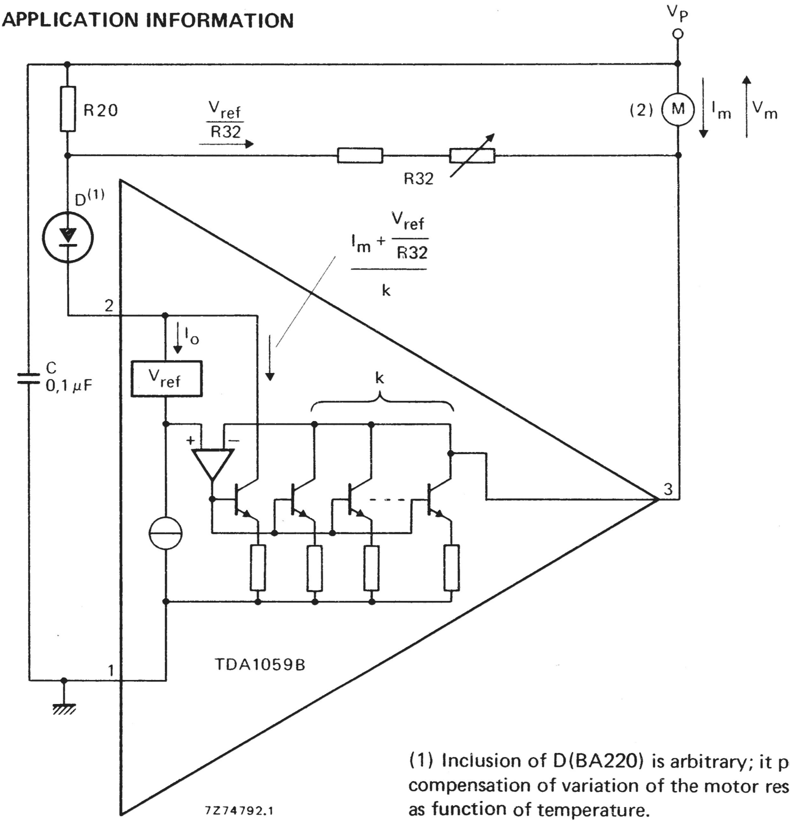

V_P
I_2
R20
2
V_{ref}
3
1
I_3
7Z74791.1

Fig. 4 Test circuit.

Note

For start operation: V_{ref} must start with final V_P = 6,7 V and a time constant of 3τ = 100 ms in which τ = R.C; R = source impedance, C = by-pass capacitor.

APPLICATION INFORMATION


V_P
R20
$\frac{V_{ref}}{R32}$
(2)
M
I_m
V_m
R32
$D^{(1)}$
$\frac{I_m + \frac{V_{ref}}{R32}}{k}$
2
I_o
V_{ref}
C
0,1 µF
k
+
−
3
TDA1059B
1
7Z74792.1

(1) Inclusion of D(BA220) is arbitrary; it permits compensation of variation of the motor resistance as function of temperature.

(2) Motor example (without diode D):

Catalogue no. 9904 120 01806; n = 2000 rev/min; R20 = 180 Ω (± 2%); R32 = 100 Ω + 100 Ω (variable).

Fig. 5 Example of using the TDA1059B in a d.c. motor speed regulation circuit.

Motor equations

$E_m = \alpha_1 n$ where: α_1, α_2 = motor constant

$I_m = \alpha_2 r$

$V_m = E_m + R_m I_m$

n = number of revolutions

r = motor torque

E_m = back electromotive force

R_m = motor resistance

The back electromotive force (E_m) in Fig. 5 can be expressed (excluding diode D) as:

$$E_m = \left(\frac{R20}{k} - R_m\right) I_m + V_{ref} \left\{1 + \frac{R20}{R32}\left(1 + \frac{1}{k}\right)\right\} + R20.I_o$$

and including diode D, as:

$$E_m = \left(\frac{R20}{k} - R_m\right) I_m + \left(V_{ref} + V_D\right) \left\{1 + \frac{R20}{R32}\left(1 + \frac{1}{k}\right)\right\} + R20.I_o$$

Speed regulation is constant when E_m is independent of I_m variations; this will be obtained when $R20 = kR_m$.

E_m, and therefore the motor speed, is regulated by R32. A practical condition for stability is $R20 < kR_m$.

MOTOR SPEED REGULATOR

The TDA1059C is a monolithic integrated circuit with a current limiter and with good thermal characteristics in a TO-126 plastic package for easy mounting. It is intended to regulate the speed of d.c. motors in record players, cassette recorders and car cassette recorders.

QUICK REFERENCE DATA

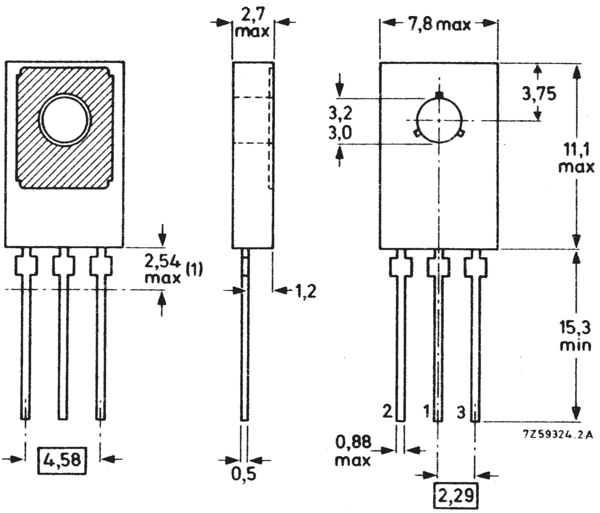
Suppy voltage	$V_P = V_{2\text{-}1}$	typ.	9	V
			2,5 to 16	V
Internal reference voltage	V_{ref}	typ.	1,1	V
Drop-out voltage	$V_{3\text{-}1}$	typ.	1,0	V
Limited output current	I_{3lim}	typ.	0,6	A
Multiplication coefficient	k	typ.	9	

PACKAGE OUTLINE

Dimensions in mm

Fig. 1 TO-126 (SOT-32).

Pin 1 connected to metal part of mounting surface.



(1) Within this region the cross-section of the leads is uncontrolled.

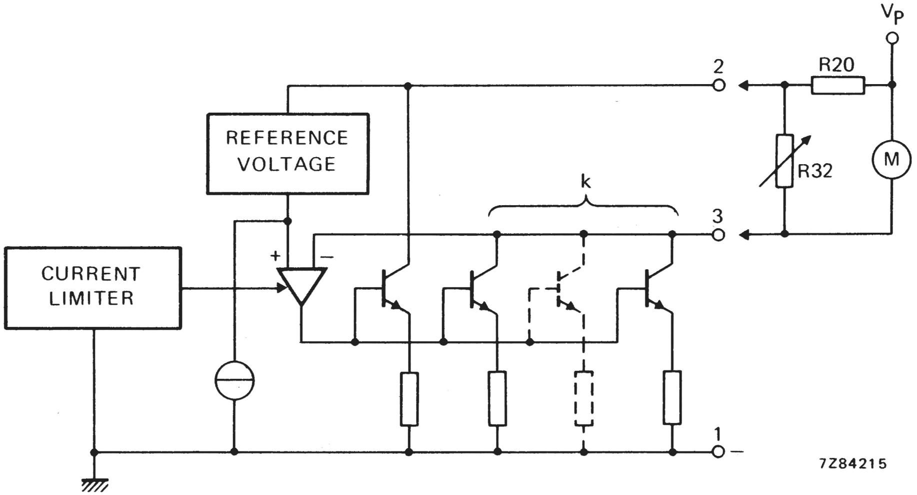

V_P
2
R20
REFERENCE VOLTAGE
k
R32
M
3
CURRENT LIMITER
+
−
1
−
7Z84215

Fig. 2 Functional diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{2\text{-}1}$	max.	16 V
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature (see Fig. 3)	T_{amb}		−25 to + 150 °C

THERMAL RESISTANCE

From junction to case	$R_{th\ j\text{-}c}$	=	10 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	100 K/W

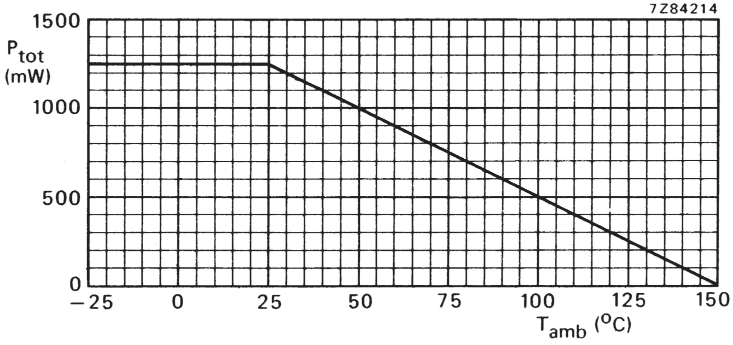
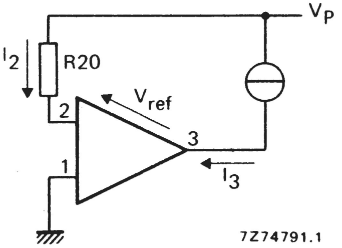


Fig. 3 Power derating curve.

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; R20 = 0; heatsink with R_{th} = 100 K/W and after thermal stabilization; unless otherwise specified; see test circuit Fig. 4

		min.	typ.	max.	
Supply voltage	$V_P = V_{2\text{-}1}$	2,5	9	15	V
Internal reference voltage V_P = 2,5 V; I_3 = 80 mA	V_{ref}	1,05	1,1	1,15	V
Drop-out voltage I_3 = 80 mA; ΔV_{ref} = 2%	$V_{3\text{-}1}$	–	1,03	1,25	V
Quiescent current; I_3 = 0	I_q	2,2	2,7	3,2	mA
Limited output current	I_{3lim}	0,3	0,45	1	A
Multiplication coefficient I_3 = 50 mA ± 10 mA	$k = \frac{\Delta I_3}{\Delta I_2}$	8,5	9	9,5	
Line regulation V_P = 2,5 to 15 V at I_3 = 50 mA					
reference voltage variation	$\frac{\Delta V_{ref}}{V_{ref}}/\Delta V_P$	0,04	0,18	0,22	%/V
multiplication coefficient variation I_3 = 50 ± 10 mA	$\frac{\Delta k}{k}/\Delta V_P$	–	0,86	–	%/V
input current variation; I_3 = 50 mA	$\frac{\Delta I_2}{\Delta V_P}$	0	15	30	µA/V
Load regulation					
reference voltage variation I_3 = 20 to 80 mA	$\frac{\Delta V_{ref}}{V_{ref}}/\Delta I_3$	0	30	45,5	%/A
multiplifaction coefficient variation I_3 = 30 ± 10 to 70 ± 10 mA	$\frac{\Delta k}{k}/\Delta I_3$	–	0,04	–	%/mA
Temperature coefficient I_3 = 50 mA; T_{amb} = –15 to + 65 °C					
reference voltage variation	$\frac{\Delta V_{ref}}{V_{ref}}/\Delta T_{amb}$	–0,036	0	+0,036	%/K
multiplication coefficient variation ΔI_3 = ± 10 mA	$\frac{\Delta k}{k}/\Delta T_{amb}$	–	0,008	–	%/K
input current variation	$\frac{\Delta I_2}{\Delta T_{amb}}$	–	4	–	µA/K



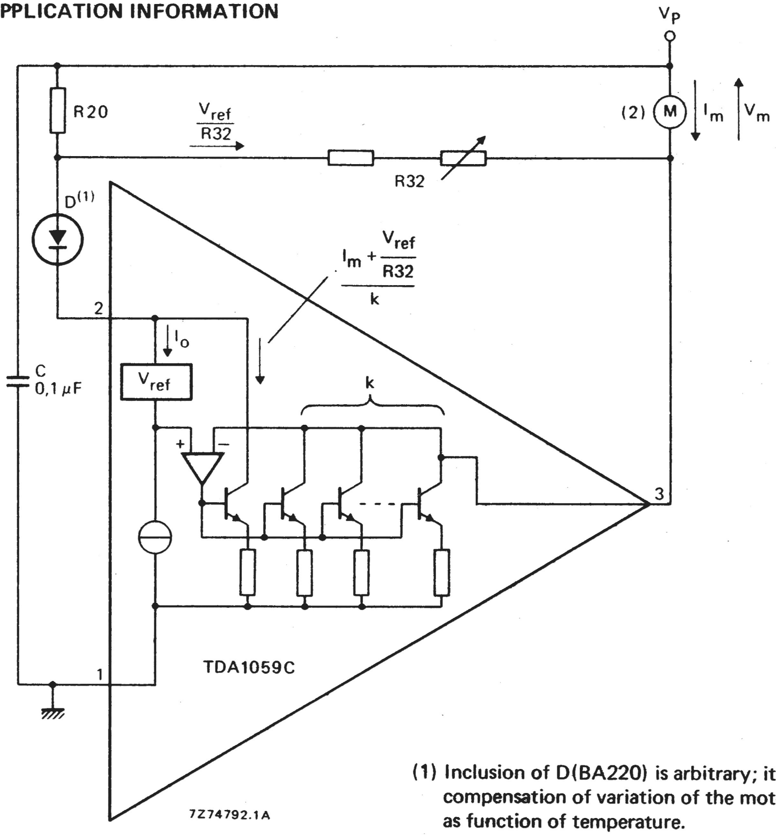
V_P
I_2
R20
V_{ref}
2
3
1
I_3
7Z74791.1

Fig. 4 Test circuit.

Note

For start operation: V_{ref} must start with final $V_P = 6$ V and a time constant of $3\ \tau = 100$ ms in which τ = R.C.; R = source impedance, C = by-pass capacitor.

APPLICATION INFORMATION



V_P
R20
$\frac{V_{ref}}{R32}$
(2)
M
I_m
V_m
R32
$D^{(1)}$
$\frac{I_m + \frac{V_{ref}}{R32}}{k}$
2
I_o
V_{ref}
C
0,1 μF
k
+
−
3
1
TDA1059C
7Z74792.1A

(1) Inclusion of D(BA220) is arbitrary; it permits compensation of variation of the motor resistance as function of temperature.

(2) Motor example (without diode D):

Catalogue no. 9904 120 01806; n = 2000 rev/min; R20 = 180 Ω (± 2%); R32 = 39 Ω + 47 Ω (variable).

Fig. 5 Example of using the TDA1059C in a d.c. motor speed regulation circuit.

Motor equations

$E_m = \alpha_1 n$

$I_m = \alpha_2 r$

$V_m = E_m + R_m I_m$

where: α_1, α_2 = motor constant
n = number of revolutions
r = motor torque
E_m = back electromotive force
R_m = motor resistance

The back electromotive force (E_m) in Fig. 5 can be expressed (excluding diode D) as:

$$E_m = \left(\frac{R20}{k} - R_m\right) I_m + V_{ref}\left\{1 + \frac{R20}{R32}\left(1 + \frac{1}{k}\right)\right\} + R20.I_o$$

and including diode D, as:

$$E_m = \left(\frac{R20}{k} - R_m\right) I_m + \left(V_{ref} + V_D\right)\left\{1 + \frac{R20}{R32}\left(1 + \frac{1}{k}\right)\right\} + R20.I_o$$

Speed regulation is constant when E_m is independent of I_m variations; this will be obtained when $R20 = kR_m$.

E_m, and therefore the motor speed, is regulated by R32. A practical condition for stability is $R20 < kR_m$.

AM RECEIVER CIRCUIT

The TDA1072 is a monolithic integrated AM receiver circuit provided with the following functions:

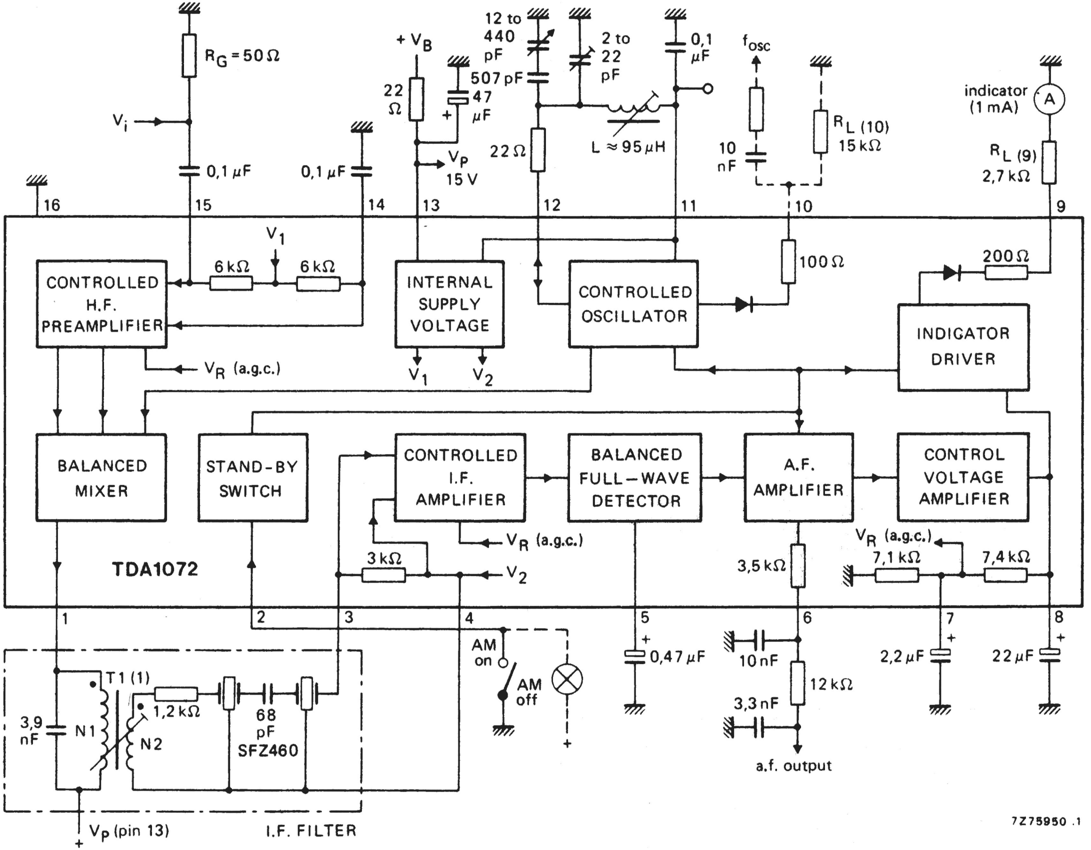
- controlled h.f. preamplifier
- multiplicative balanced mixer
- separate oscillator with amplitude control
- i.f. amplifier with gain control
- balanced full-wave detector
- a.f. preamplifier
- internal a.g.c. voltage
- amplifier for field-strength indication
- electronic stand-by on/off switch

QUICK REFERENCE DATA

Supply voltage (pin 13)	V_P	typ.	15	V
Supply current	I_P	typ.	22	mA
H.F. input voltage				
S + N/N = 6 dB	V_i	typ.	2,2	μV
S + N/N = 26 dB	V_i	typ.	30	μV
H.F. input voltage; d_{tot} = 3%; m = 80%	V_i	typ.	650	mV
A.F. output voltage; V_i = 2 mV	V_o	typ.	340	mV
Total distortion	d_{tot}	typ.	0,5	%
Input voltage range for ΔV_o = 6 dB	ΔV_i	typ.	91	dB
Oscillator frequency range	f_{osc}		0,6 to 31	MHz
Oscillator voltage amplitude	V_{osc}	typ.	140	mV
Field-strength indication range	ΔV_i	typ.	100	dB
Supply voltage range	V_P		7,5 to 18	V
Ambient temperature range	T_{amb}		−30 to + 80	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).


R_G = 50 Ω
V_i
0,1 μF
15
16
0,1 μF
14
+ V_B
22 Ω
47 μF
V_P 15 V
13
12 to 440 pF
507 pF
22 Ω
12
2 to 22 pF
L ≈ 95 μH
0,1 μF
11
f_osc
10 nF
R_L (10) 15 kΩ
10
indicator (1 mA)
A
R_L (9) 2,7 kΩ
9
V_1
6 kΩ
6 kΩ
CONTROLLED H.F. PREAMPLIFIER
V_R (a.g.c.)
INTERNAL SUPPLY VOLTAGE
V_1
V_2
CONTROLLED OSCILLATOR
100 Ω
200 Ω
INDICATOR DRIVER
BALANCED MIXER
STAND-BY SWITCH
CONTROLLED I.F. AMPLIFIER
V_R (a.g.c.)
BALANCED FULL-WAVE DETECTOR
A.F. AMPLIFIER
CONTROL VOLTAGE AMPLIFIER
3 kΩ
V_2
TDA1072
3,5 kΩ
V_R (a.g.c.)
7,1 kΩ
7,4 kΩ
1
2
3
4
5
6
7
8
AM on
AM off
0,47 μF
10 nF
12 kΩ
3,3 nF
a.f. output
2,2 μF
22 μF
T1 (1)
3,9 nF
N1
N2
1,2 kΩ
68 pF
SFZ460
V_P (pin 13)
I.F. FILTER
7Z75950 .1

(1) T1 : N1/N2 = 34/9; $Q_o = 65$; $Q_L = 60$; $Z_{21} = 700\ \Omega$ at $R_{L(3)} = 3\ k\Omega$; $Z_{11} = 5,2\ k\Omega$.

Fig. 1 Block diagram with external components; used as test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13\text{-}16}$	max.	23	V
Voltage on pin 2	$V_{2\text{-}16}$		0 to 23	V

H.F. inputs

Voltages between:				
pins 14 and 15	$\pm V_{14\text{-}15}$	max.	12	V
pins 14 and 16	$V_{14\text{-}16}$	max.	V_P	V
pins 15 and 16	$V_{15\text{-}16}$	max.	V_P	V
Or currents:				
pin 14	$\pm I_{14}$	max.	10	mA
pin 15	$\pm I_{15}$	max.	10	mA
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

V_P = 15 V; T_{amb} = 25 °C; f_i = 1 MHz (h.f.), R_G = 50 Ω; f_m = 0,4 kHz; m = 30%;
i.f. frequency = 460 kHz; unless otherwise specified

Supply voltage range (pin 13)	V_P		7,5 to 18	V
Supply current; without load ($I_{L(11)} = 0$)	I_P	typ.	22	mA
			15 to 30	mA

H.F. preamplifier and mixer

D.C. input voltages	$V_{14\text{-}16}$; $V_{15\text{-}16}$	typ.	2,75 ($4V_{BE}$)	V
Input impedance				
$V_i < 300\ \mu V$	$Z_{i(14\text{-}16)}$; $Z_{i(15\text{-}16)}$	typ.	6	kΩ
		typ.	6	pF
$V_i > 10$ mV	$Z_{i(14\text{-}16)}$; $Z_{i(15\text{-}16)}$	typ.	9	kΩ
		typ.	2,5	pF
Output impedance	$Z_{o(1\text{-}16)}$	>	200	kΩ
		typ.	4	pF
Maximum conversion conductance	S_M	typ.	5,5	mA/V*
Maximum i.f. output voltage (peak-to-peak value)	$V_{o(1)(p\text{-}p)}$	typ.	2,8	V
Output current capability	$I_{o(1)}$	typ.	1	mA
Control range of preamplifier	ΔS_M	typ.	30	dB
Maximum h.f. input voltage (peak-to-peak value)	$V_{i(14\text{-}15)(p\text{-}p)}$	typ.	2,8	V

---

* S_M is defined as $I_{o(1)}/V_i$.

CHARACTERISTICS (continued)

Oscillator

Frequency range	$f_{osc(12)}$		0,6 to 31	MHz
Oscillator impedance range	$Z_{L(12)}$		1 to 200	kΩ
Controlled oscillator amplitude	$V_{osc(12)}$	typ. <	140 200	mV mV
D.C. output voltage ($I_{L(11)} = 0$)	$V_{11\text{-}16}$	typ.	V_P–1,3	V
Output load current range	$-I_{L(11)}$		0 to 15	mA
Output resistance; $I_{L(11)} = 5 \pm 0,5$ mA	$R_{o(11)}$	typ.	7	Ω

Oscillator frequency output (pin 10)

Output voltage (peak-to-peak value) $R_{10\text{-}16} = 15$ kΩ ($R_{L(10)}$)	$V_{o(10)(p\text{-}p)}$	typ.	200	mV
Output resistance	$R_{o(10)}$	typ.	150	Ω
Allowable output current (peak value)	$I_{o(10)M}$	<	2	mA

I.F. amplifier and a.f. stage

D.C. input voltages	$V_{3\text{-}16}$; $V_{4\text{-}16}$	typ.	2	V
Input impedance	$Z_{i(3)}$	typ. typ.	3 2,4 to 3,9 4	kΩ kΩ pF
Max. i.f. input voltage; m = 80%; $d_{tot} = 3\%$	$V_{i(3)}$	typ.	75	mV
Control range; $V_o = -6$ dB	ΔV_i	typ.	62	dB
A.F. output voltage; $V_{i(3)} = 2$ mV; without load	$V_{o(6)}$	typ.	350	mV
A.F. output resistance	$R_{o(6)}$	typ.	3,5	kΩ

Field-strength indication

D.C. indicator voltage $V_i = 0$; $R_{L(9)} = 2,7$ kΩ	$V_{9\text{-}16}$	typ. <	0 140	mV mV
$V_i = 500$ mV; $R_{L(9)} = 2,7$ kΩ	$V_{9\text{-}16}$	typ.	2,8 2,5 to 3,1	V V
Output current capability	$-I_9$	>	1,2	mA
Output resistance; $-I_9 = 0,5$ mA	$R_{o(9)}$	typ.	250	Ω
Leakage voltage at the output; $\pm I_9 \leqslant 1\ \mu A$; at AM switch off ($V_{2\text{-}16} \geqslant 3,5$ V)	$V_{9\text{-}16}$	typ.	6	V

Stand-by switch

Switching voltage	$V_{2\text{-}16}$	typ.	2,6	V
Required control voltage*				
AM on	$V_{2\text{-}16}$	$<$	2	V
AM off	$V_{2\text{-}16}$	$>$	3,5	V**
Input current				
AM on; switching current	$-I_2$	$<$	100	μA
AM off; leakage current ($V_{2\text{-}16} = V_{3\text{-}16}$)	$\pm I_2$	$<$	1	μA

APPLICATION INFORMATION

$V_P = 15$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $f_i = 1$ MHz (h.f.); $f_m = 0{,}4$ kHz; $m = 30\%$; unless otherwise specified

H.F. input voltage				
S + N/N = 6 dB	V_i	typ.	2,2	μV
S + N/N = 10 dB	V_i	typ.	3,5	μV
S + N/N = 26 dB	V_i	typ.	30	μV
S + N/N = 46 dB	V_i	typ.	550	μV
H.F. input voltage for a.g.c. operation	V_i	typ.	14	μV
Control range for $\Delta V_o = 6$ dB				
reference value $V_i = 500$ mV	ΔV_i	typ.	91	dB
Maximum h.f. input voltage				
$d_{tot} = 3\%$; $m = 80\%$	V_i	typ.	0,65	V
$d_{tot} = 3\%$; $m = 30\%$	V_i	typ.	0,9	V
$d_{tot} = 10\%$; $m = 30\%$	V_i	typ.	1,3	V
A.F. output voltage; $V_i = 2$ mV	V_o	typ.	340	mV
Change of a.f. output voltage; $V_i = 2$ mV	ΔV_o	typ.	± 2	dB
H.F. input voltage; $V_o = 60$ mV	V_i	typ.	4	μV
Total distortion of a.f. output voltage				
$V_i = 2$ mV; $m = 80\%$	d_{tot}	typ.	0,5	%
$V_i = 500$ mV; $m = 80\%$	d_{tot}	typ. $<$	1,8 3	% %
Signal plus noise-to-noise ratio of a.f. output voltage				
$V_i = 2$ mV	S + N/N	typ.	50	dB
I.F. bandwidth (−3 dB)	B	typ.	4,6	kHz
I.F. selectivity				
$\Delta f = \pm 9$ kHz	$S_{(9)}$	typ.	30	dB
$\Delta f = \pm 36$ kHz	$S_{(36)}$	typ.	60	dB

---

* At allowable ambient temperature range and supply voltage range.

** Also achieved at open input.

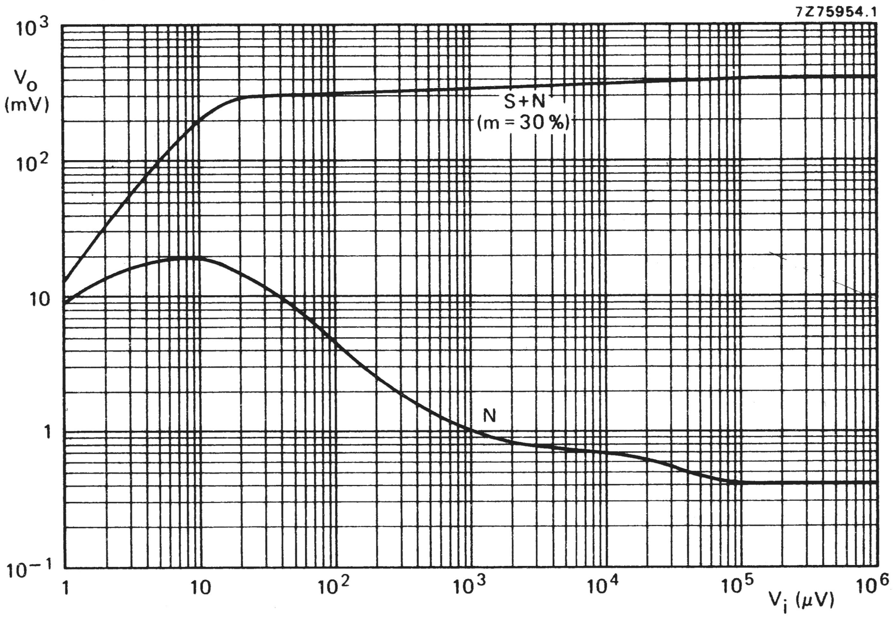


Fig. 2 A.F. output voltage as a function of h.f. input voltage; f_i = 1 MHz (h.f.); R_G = 50 Ω; f_m = 0,4 kHz.

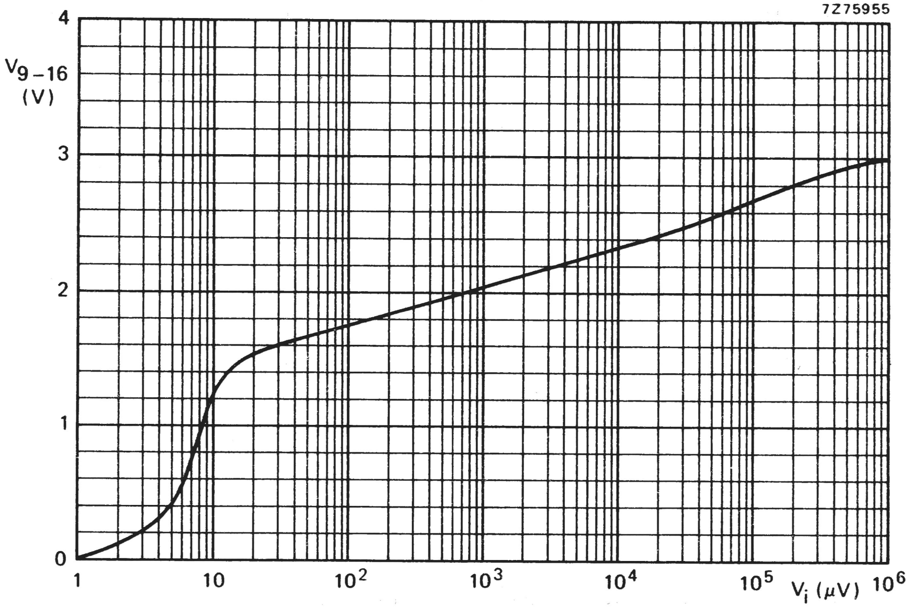


Fig. 3 Indication voltage as a function of h.f. input voltage; R_{9-16} = 2,7 kΩ.

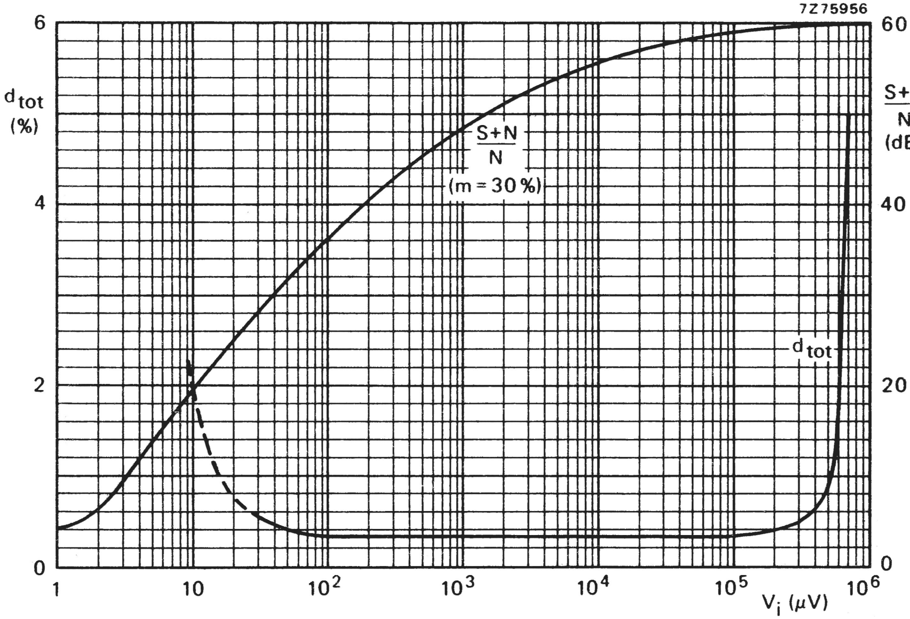


Fig. 4 Total distortion and signal plus noise-to-noise ratio as a function of h.f. input voltage; for d_{tot} : f_m = 0,4 kHz; m = 80%.

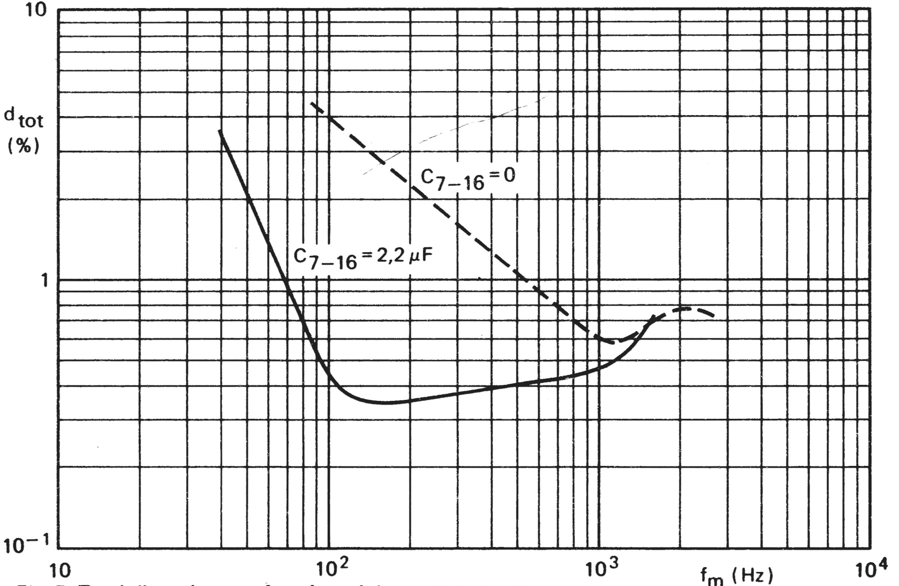


Fig. 5 Total distortion as a function of the modulation frequency; V_i = 10 mV; f_i = 1 MHz; m = 80%. $C_{8\text{-}16}$ = 22 μF.

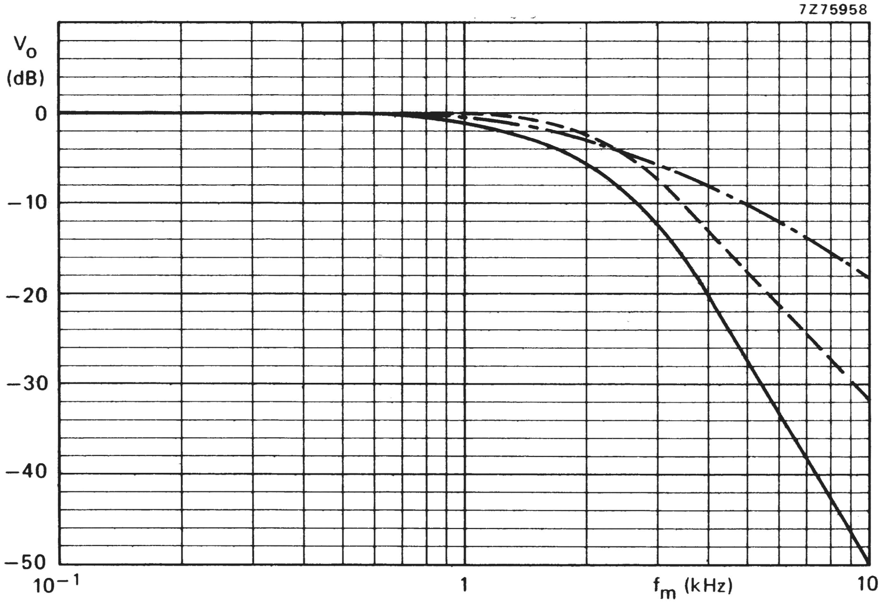
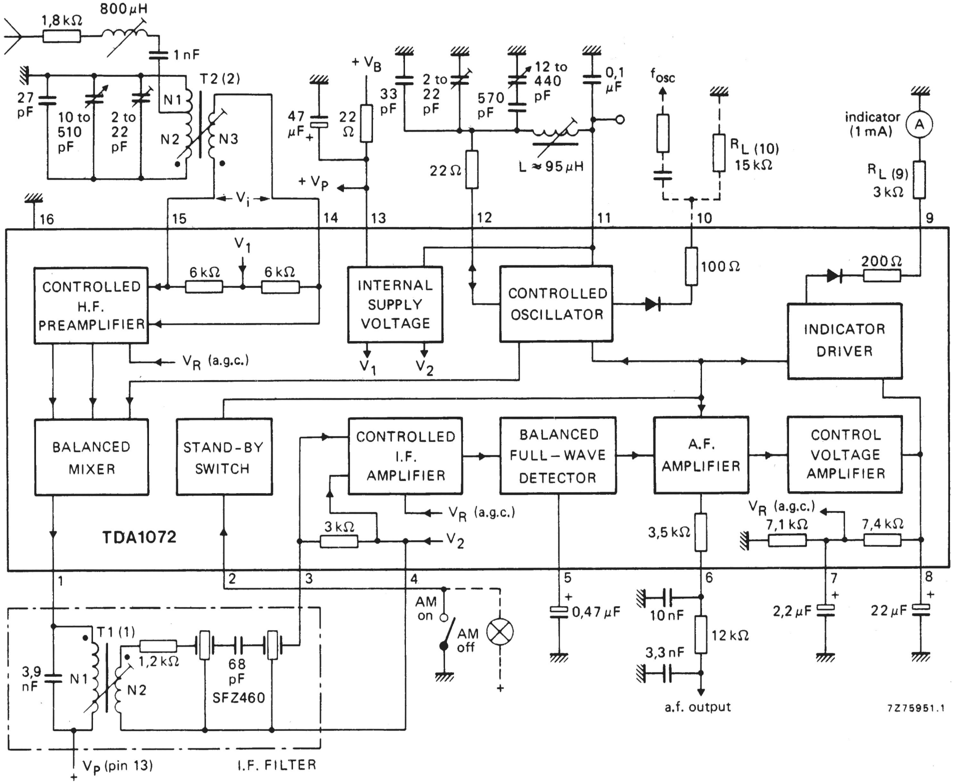


Fig. 6 Frequency responses (wobbled) for various conditions:
——— with a.f. and i.f. filter
– – – with i.f. filter
– · – with a.f. filter


1,8 kΩ
800 μH
1 nF
T2 (2)
N1
N2
N3
27 pF
10 to 510 pF
2 to 22 pF
+ V_B
47 μF
22 Ω
33 pF
2 to 22 pF
570 pF
12 to 440 pF
0,1 μF
22 Ω
L ≈ 95 μH
f_osc
R_L (10) 15 kΩ
indicator (1 mA)
A
R_L (9) 3 kΩ
+ V_P
V_i
16
15
14
13
12
11
10
9
V_1
6 kΩ
6 kΩ
CONTROLLED H.F. PREAMPLIFIER
INTERNAL SUPPLY VOLTAGE
CONTROLLED OSCILLATOR
100 Ω
200 Ω
INDICATOR DRIVER
V_R (a.g.c.)
V_1
V_2
BALANCED MIXER
STAND-BY SWITCH
CONTROLLED I.F. AMPLIFIER
BALANCED FULL-WAVE DETECTOR
A.F. AMPLIFIER
CONTROL VOLTAGE AMPLIFIER
V_R (a.g.c.)
3 kΩ
V_2
3,5 kΩ
V_R (a.g.c.)
7,1 kΩ
7,4 kΩ
TDA1072
1
2
3
4
5
6
7
8
AM on
AM off
0,47 μF
10 nF
12 kΩ
3,3 nF
2,2 μF
22 μF
a.f. output
7Z75951.1
T1 (1)
3,9 nF
N1
N2
1,2 kΩ
68 pF
SFZ460
V_P (pin 13)
I.F. FILTER

(1) T1 : N1/N2 = 34/9; Q_o = 65; Q_L = 60; Z_{21} = 700 Ω at $R_{L(3)}$ = 3 kΩ; Z_{11} = 5,2 kΩ.
(2) T2 : N1/N2/N3 = 14/67/17; L = 175 μH; Q_o = 145; Q_L = 50 (f = 1 MHz); V_i/V_G = –6 dB.

Fig. 7 Application circuit diagram of a AM-MW receiver with two double variable tuning capacitors; f_i = 510 to 1620 kHz (h.f.); f_i = 460 kHz (i.f.).

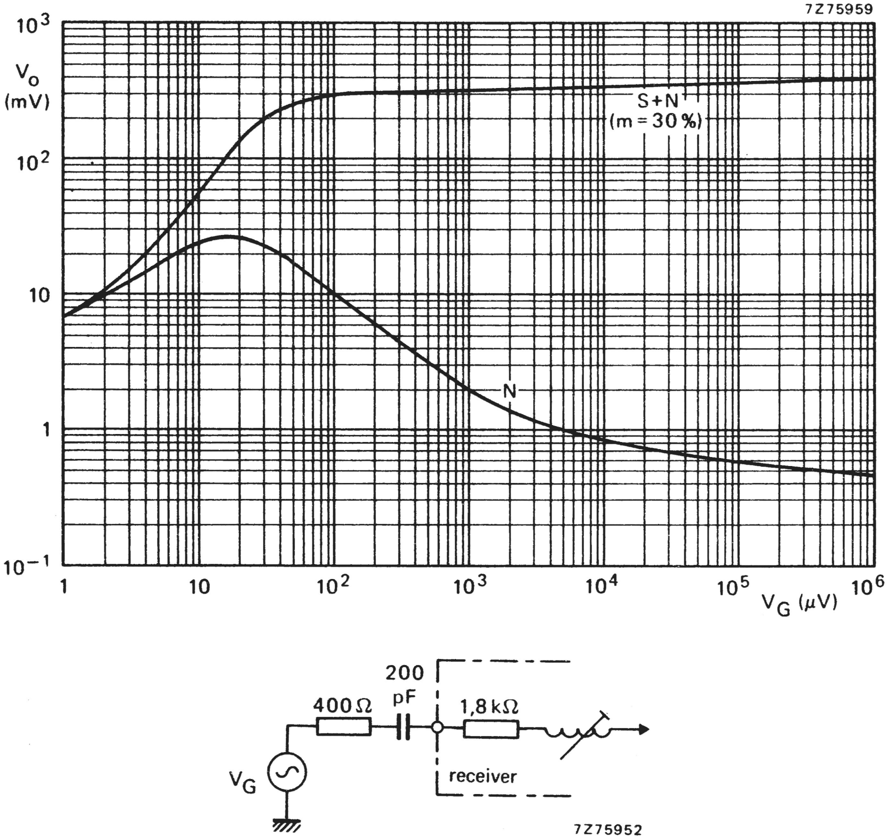


Fig. 8 A.F. output voltage as a function of the h.f. generator input voltage; f_i = 1 MHz (h.f.); f_m = 0,4 kHz.

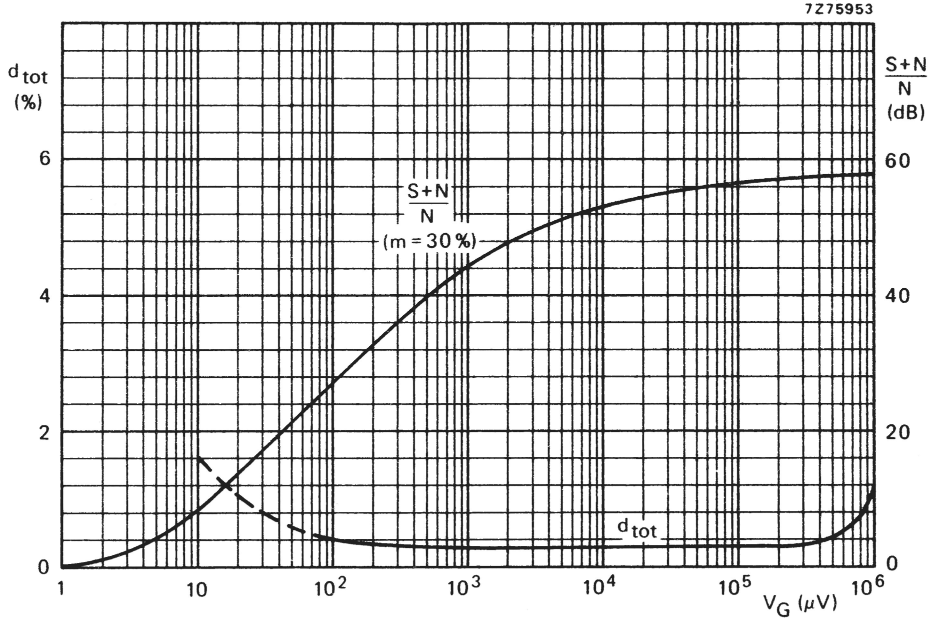


Fig. 9 Total distortion and signal plus noise-to-noise ratio as a function of h.f. generator input voltage; for d_{tot} : f_m = 0,4 kHz; m = 80%.

DUAL TANDEM ELECTRONIC POTENTIOMETER CIRCUIT

GENERAL DESCRIPTION

The TDA1074A is a monolithic integrated circuit designed for use as volume and tone control circuit in stereo amplifiers. This dual tandem potentiometer IC consists of two ganged pairs of electronic potentiometers with the eight inputs connected via impedance converters, and the four outputs driving individual operational amplifiers. The setting of each electronic potentiometer pair is controlled by an individual d.c. control voltage. The potentiometers operate by current division between the arms of cross-coupled long-tailed pairs. The current division factor is determined by the level and polarity of the d.c. control voltage with respect to an externally available reference level of half the supply voltage. Since the electronic potentiometers are adjusted by a d.c. control voltage, each pair can be controlled by single linear potentiometers which can be located in any position dictated by the equipment styling. Since the input and feedback impedances around the operational amplifier gain blocks are external, the TDA1074A can performs bass/treble and volume/loudness control. It also can be used as a low-level fader to control the sound distribution between the front and rear loudspeakers in car radio installations.

Features

- High impedance inputs to both ‘ends’ of each electronic potentiometer
- Ganged potentiometers track within 0,5 dB
- Electronic rejection of supply ripple
- Internally generated reference level available externally so that the control voltage can be made to swing positively and negatively around a well-defined 0 V level
- The operational amplifiers have push-pull outputs for wide voltage swing and low current consumption
- The operational amplifier outputs are current limited to provide output short-circuit protection
- Although designed to operate from a 20 V supply (giving a maximum input and output signal level of 6 V), the TDA1074A can work from a supply as low as 7,5 V with reduced input and output signal levels

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	20	V
Supply current (pin 11)	I_P	typ.	22	mA
Input signal voltage (r.m.s. value)	$V_{i(rms)}$	max.	6	V
Output signal voltage (r.m.s. value)	$V_{o(rms)}$	max.	6	V
Total harmonic distortion	THD	typ.	0,05	%
Output noise voltage (r.m.s. value)	$V_{no(rms)}$	typ.	50	μV
Control range	$\Delta\alpha$	typ.	110	dB
Cross-talk attenuation (L/R)	α_{ct}	typ.	80	dB
Ripple rejection (100 Hz)	α_{100}	typ.	46	dB
Tracking of ganged potentiometers	ΔG_v	typ.	0,5	dB
Supply voltage range	V_P		7,5 to 23	V
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).

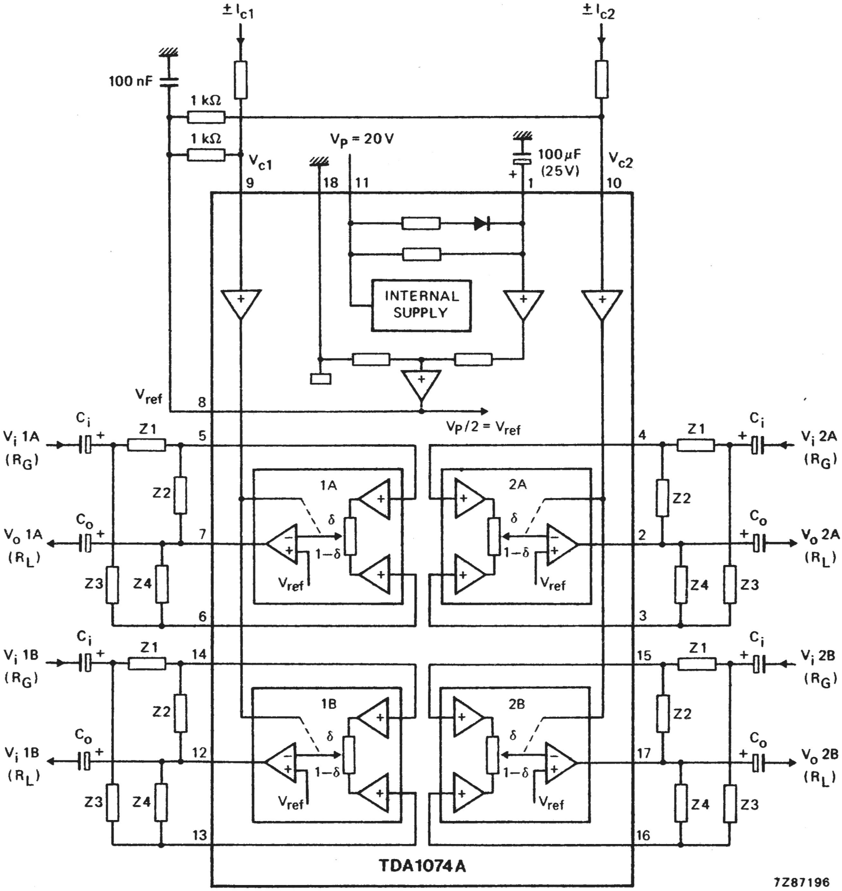

±Ic1
±Ic2
100 nF
1 kΩ
1 kΩ
Vc1
VP = 20 V
100 µF
(25 V)
Vc2
9
18
11
1
10
INTERNAL
SUPPLY
Vref
8
VP/2 = Vref
Ci
Vi 1A
(RG)
Z1
5
4
Vi 2A
Z2
1A
2A
δ
1−δ
Co
Vo 1A
(RL)
7
2
Vo 2A
Z3
Z4
6
3
Vi 1B
14
15
Vi 2B
1B
2B
12
17
Vo 2B
13
16
TDA1074A
7Z87196

Fig. 1 Block diagram and basic external components; I_{c1} (at pin 9) and I_{c2} (at pin 10) are control input currents; V_{c1} (at pin 9) and V_{c2} (at pin 10) are control input voltages with respect to $V_{ref} = V_P/2$ at pin 8; $Z1 = Z2 = Z3 = Z4 = 22\ k\Omega$; the input generator resistance $R_G = 60\ \Omega$; the output load resistance $R_L = 4,7\ k\Omega$; the coupling capacitors at the inputs and outputs are $C_i = 2,2\ \mu F$ and $C_o = 10\ \mu F$ respectively.

DEVELOPMENT SAMPLE DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	V_P	max.	23	V
Control voltages (pins 9 and 10)	$\pm V_{c1}; \pm V_{c2}$	max.	1	V
Input voltage ranges (with respect to pin 18) at pins 3, 4, 5, 6, 13, 14, 15, 16	V_i		0 to V_P	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80	K/W

REMARK

The difference between the TDA1074 and its successor the TDA1074A is shown in Fig. 2 as the different component configuration at pin 8.

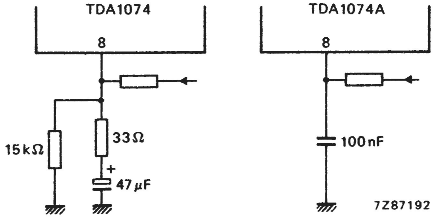


Fig. 2 Component configuration at pin 8 showing the difference between the TDA1074 and the TDA1074A.

APPLICATION INFORMATION

Treble and bass control circuit

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 3; R_G = 60 Ω; $R_L > 4{,}7$ kΩ; $C_L < 30$ pF; f = 1 kHz; with a linear frequency response ($V_{c1} = V_{c2}$ = 0 V); unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply current (without load)	I_P	14	22	30	mA
Frequency response (−1 dB) $V_{c1} = V_{c2}$ = 0 V	f	10	–	20 000	Hz
Voltage gain at linear frequency response ($V_{c1} = V_{c2}$ = 0 V)	G_v*	–	0	–	dB
Gain variation at f = 1 kHz at maximum bass/treble boost or cut at ± V_{c1} = ± V_{c2} = 120 mV	ΔG_v*	–	± 1	–	dB
Bass boost at 40 Hz (ref. 1 kHz) V_{c2} = 120 mV		–	17,5	–	dB
Bass cut at 40 Hz (ref. 1 kHz) $-V_{c2}$ = 120 mV		–	17,5	–	dB
Treble boost at 16 kHz (ref. 1 kHz) V_{c1} = 120 mV		–	16	–	dB
Treble cut at 16 kHz (ref. 1 kHz) $-V_{c1}$ = 120 mV		–	16	–	dB
Total harmonic distortion at $V_{o(rms)}$ = 300 mV f = 1 kHz (measured selectively)	THD	–	0,002	–	%
f = 20 Hz to 20 kHz	THD	–	0,005	–	%
at $V_{o(rms)}$ = 5 V f = 1 kHz	THD	–	0,015	0,1	%
f = 20 Hz to 20 kHz	THD	–	0,05	0,1	%
Signal level at THD = 0,7% (input and output)	$V_{i;\,o(rms)}$	5,5	6,2	–	V
Power bandwidth at reference level $V_{o(rms)}$ = 5 V (−3 dB); THD = 0,1%	B	–	40	–	kHz
Output noise voltages signal plus noise (r.m.s. value); f = 20 Hz to 20 kHz	$V_{no(rms)}$	–	75	–	μV
noise (peak value); weighted to DIN 45 405; CCITT filter	$V_{no(m)}$	–	160	230	μV

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* $G_v = V_o/V_i$.

Treble and bass control circuit

parameter	symbol	min.	typ.	max.	unit
Cross-talk attenuation (stereo)					
f = 1 kHz	α_{ct}	—	86	—	dB
f = 20 Hz to 20 kHz	α_{ct}	—	80	—	dB
Control voltage cross-talk to the outputs at f = 1 kHz; $V_{c1(rms)} = V_{c2(rms)} = 1$ mV	$-\alpha_{ct}$	—	20	—	dB
Ripple rejection at f = 100 Hz; $V_{P(rms)} < 200$ mV	α_{100}	—	46	—	dB

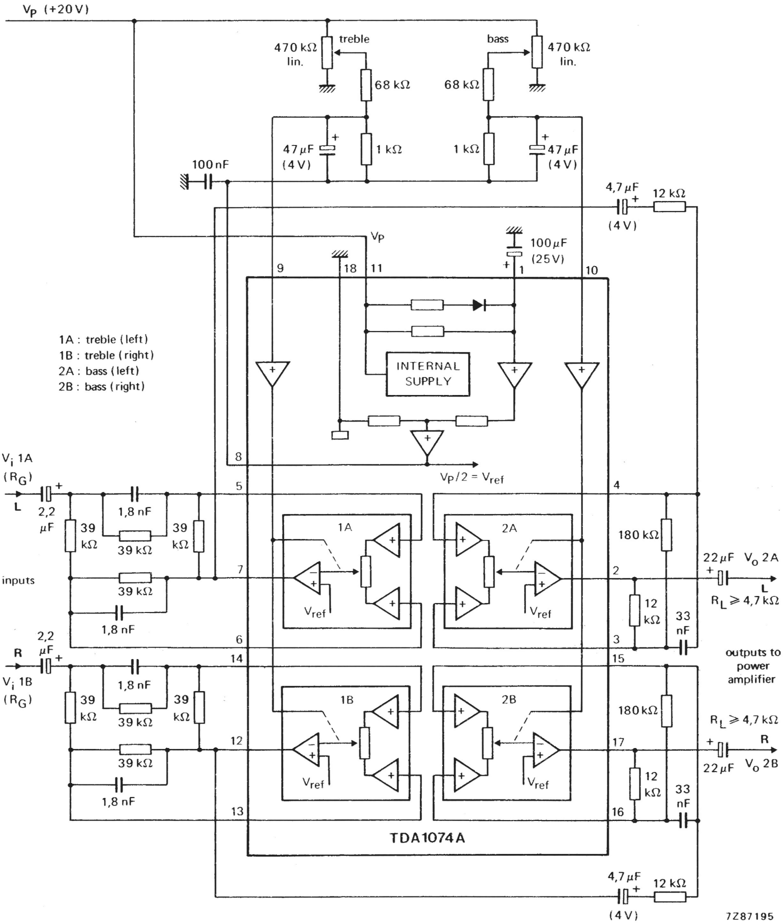

V_P (+20 V)
470 kΩ lin.
treble
68 kΩ
bass
470 kΩ lin.
68 kΩ
47 μF (4 V)
1 kΩ
1 kΩ
47 μF (4 V)
100 nF
4,7 μF (4 V)
12 kΩ
V_P
100 μF (25 V)
9
18
11
1
10
1A : treble (left)
1B : treble (right)
2A : bass (left)
2B : bass (right)
INTERNAL SUPPLY
8
$V_P/2 = V_{ref}$
V_i 1A (R_G)
L
2,2 μF
39 kΩ
1,8 nF
39 kΩ
39 kΩ
5
4
1A
2A
180 kΩ
inputs
39 kΩ
7
2
22 μF
V_o 2A
L
$R_L \geq 4,7$ kΩ
V_{ref}
V_{ref}
12 kΩ
33 nF
1,8 nF
6
3
2,2 μF
R
14
15
outputs to power amplifier
V_i 1B (R_G)
39 kΩ
1,8 nF
39 kΩ
39 kΩ
1B
2B
180 kΩ
$R_L \geq 4,7$ kΩ
R
12
17
22 μF
V_o 2B
39 kΩ
V_{ref}
V_{ref}
12 kΩ
33 nF
1,8 nF
13
16
TDA1074A
4,7 μF (4 V)
12 kΩ
7Z87195

Fig. 3 Application diagram for treble and bass control.

APPLICATION INFORMATION (continued)

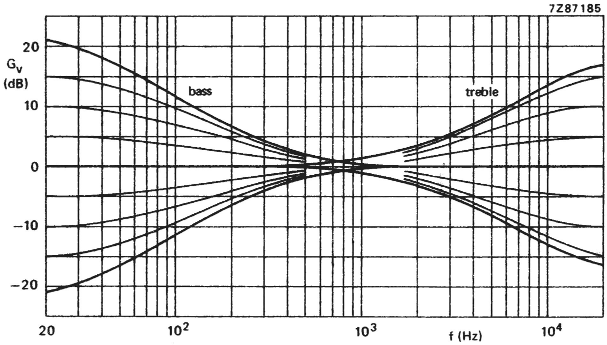


Fig. 4 Frequency response curves; voltage gain (treble and bass) as a function of frequency.

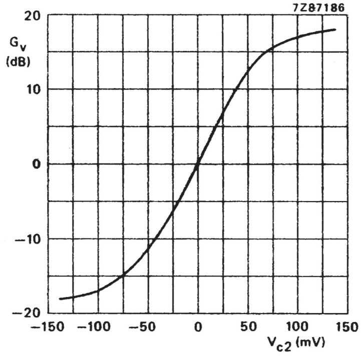


Fig. 5 Control curve; voltage gain (bass) as a function of the control voltage (V_{c2}); f = 40 Hz.

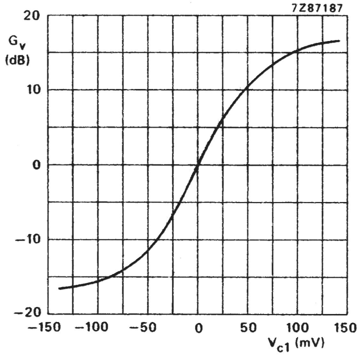
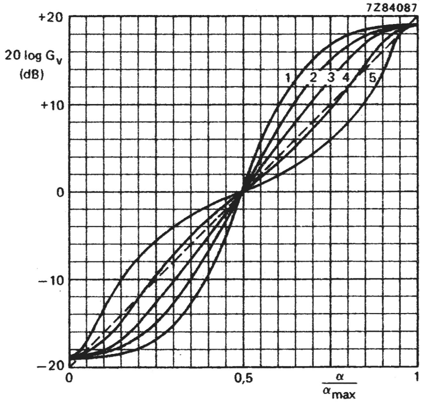


Fig. 6 Control curve; voltage gain (treble) as a function of the control voltage (V_{c1}); f = 16 kHz.



curve no.	value of R
1	10 kΩ
2	100 kΩ
3	220 kΩ
4	470 kΩ
5	1 MΩ

Fig. 7 Voltage gain ($G_V = V_o/V_i$) control curves as a function of the angle of rotation (α) of a linear potentiometer (R); for curve numbers see table above; f = 40 Hz to 16 kHz.

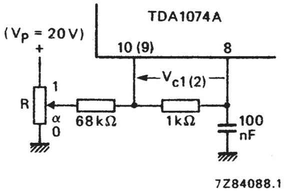

TDA1074A
(V_P = 20 V)
+
10 (9)
8
$V_{c1(2)}$
1
R
α
0
68 kΩ
1 kΩ
100
nF
7Z84088.1

Fig. 8 Circuit diagram for measuring curves in Fig. 7.

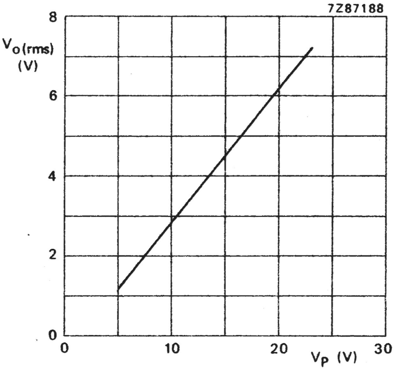


Fig. 9 Output signal level as a function of V_P; THD = 0,7%; f = 1 kHz; $V_{c1} = V_{c2} = 0$ V.

APPLICATION INFORMATION (continued)

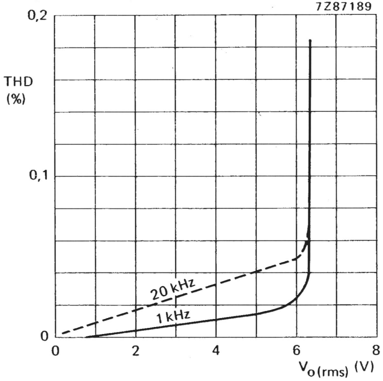


Fig. 10 Total harmonic distortion as a function of the output level; $V_P = 20$ V; $R_L = 4,7$ kΩ; $V_{c1} = V_{c2} = 0$ V (linear, $G_{v\,tot} = 1$). ——— f = 1 kHz; – – – – f = 20 kHz.

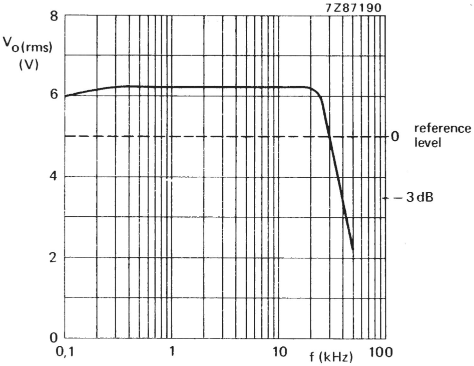


Fig. 11 Power bandwidth at THD = 0,1%; reference level is 5 V (r.m.s.).

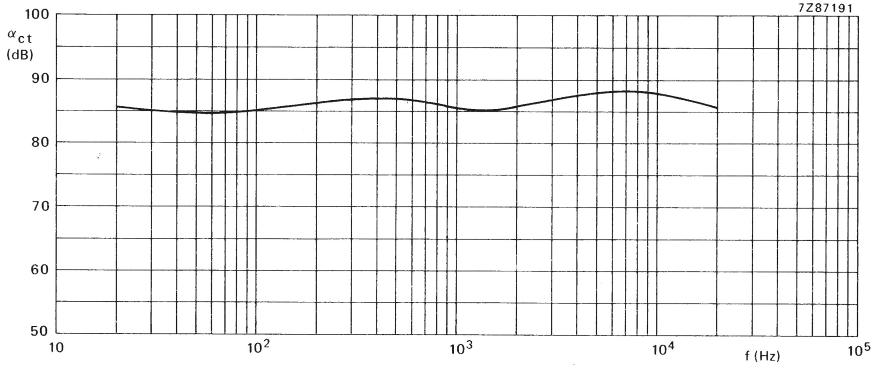
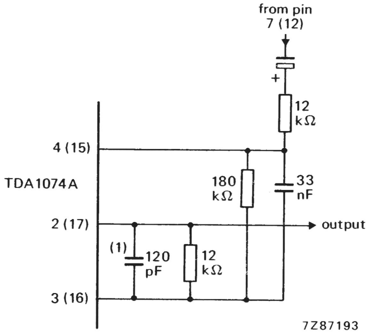


Fig. 12 Cross-talk as a function of frequency; linear treble/bass setting ($V_{c1} = V_{c2} = 0$ V); $V_i = 5$ V; $R_G = 60$ Ω; $R_L = 4,7$ kΩ.

Application recommendations

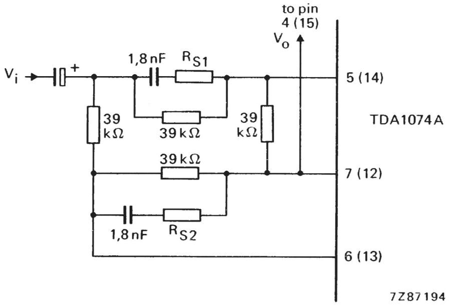
1. If one or more electronic potentiometers in an IC are not used, the following is recommended:
   a. Unused signal inputs of an electronic potentiometer should be connected to the associated output, e.g. pins 3 and 4 to pin 2.
   b. Unused control voltage inputs should be connected directly to pin 8 (V_{ref}).
2. Where more than one TDA1074A IC are used in an application, pins 1 can be connected together; however, pins 8 (V_{ref}) may not be connected together directly.
3. Additional circuitry for limiting the frequency response in the ultrasonic range.


from pin
7 (12)
+
12
kΩ
4 (15)
TDA1074A
180
kΩ
33
nF
2 (17)
output
(1)
120
pF
12
kΩ
3 (16)
7Z87193

(1) $f_{-3\,dB}$ = 110 kHz at linear setting

Fig. 13 Circuit diagram for frequency response limiting.

4. Alternative circuitry for limiting the gain of the treble control circuit in the ultrasonic range.


to pin
4 (15)
V_o
V_i
+
1,8 nF
R_{S1}
5 (14)
39
kΩ
39 kΩ
39
kΩ
TDA1074A
39 kΩ
7 (12)
1,8 nF
R_{S2}
6 (13)
7Z87194

For $R_{S1} = R_{S2}$ = 3,3 kΩ; $f_{-3\,dB} \cong$ 1 MHz at linear setting
For $R_{S1} = R_{S2}$ = 0 Ω; $f_{-3\,dB} \cong$ 100 kHz at linear setting

Fig. 14 Circuit diagram for limiting gain of treble control circuit.

MOTOR REGULATOR AND FUNCTION CONTROLLER FOR CAR CASSETTE SYSTEMS

The TDA1506 is for car radio/casette players. It incorporates the following functions:

- a motor speed regulator with a multiplication coefficient of k = 20,5.
- an electronic motor stop, controlled by commutator pulses;
- protection circuitry to avoid restarting of the motor after the set is switched to radio reception;
- playback indication;
- tape-end indication with intermittent light;
- fast-wind/rewind circuitry;
- two separately stabilized voltage regulators for the playback amplifier stages;
- a stabilized output voltage for the radio part;
- an automatic switch for switching the preamplifier supply outputs to zero and the radio supply output to a high level at tape-end;
- an output signal for auto-reverse;
- short-circuit protection for all pins to ground at T_{amb} = 30 °C maximum and between output and power supply pin;
- load dump protection.

During fast wind (or rewind) the voltage regulator for the second playback preamplifier is switched off. This feature allows application in an A.P.S.S. (Automatic Program Search System) set. At tape-end and at an externally chosen fixed time before motor stop, the automatic replay output gives a d.c. information signal. This signal may, e.g., be used to control the plunger in an automatic-reverse set. Automatic switching, with all switches to ground.

QUICK REFERENCE DATA

Supply voltage range	V_P		10 to 16	V
Operating ambient temperature range				
at V_P = 14,4 V	T_{amb}		−20 to +80	°C
at V_P = 16 V	T_{amb}		−20 to +60	°C
Motor regulator				
Regulator supply voltage range	V_{6-3}		3,2 to 12	V
Internal reference voltage	$V_{ref} = V_{6-5}$	typ.	1,38	V
Drop-out voltage	V_{4-3}	$<$	1,8	V
Multiplication coefficient ($\Delta I_4/\Delta I_6$)	k	typ.	20,5	
Stabilization radio				
Output voltage	V_{11-8}	$>$	8,5	V
Limited output current	$I_{11\ lim}$	$>$	45	mA
Stabilization preamplifier I				
Output voltage	V_{10-8}	$>$	7,7	V
Limited output current	$I_{10\ lim}$	$>$	2	mA
Stabilization preamplifier II				
Output voltage	V_{9-8}	$>$	8,7	V
Limited output current	$I_{9\ lim}$	$>$	20	mA
Lamp driver				
Output voltage	V_{2-8}	$>$	13	V
Limited output current	$I_{2\ lim}$	$>$	20	mA

PACKAGE OUTLINE 16-lead DIL; plastic power (SOT-38).

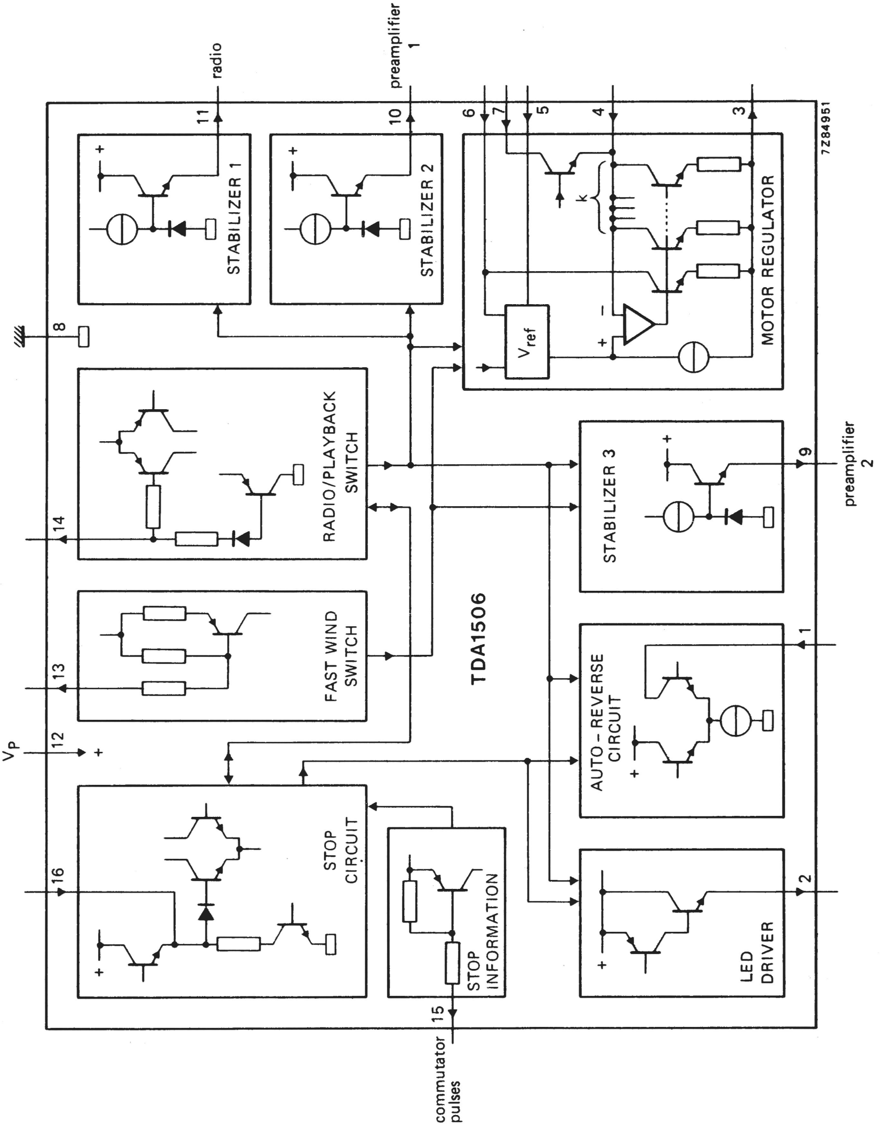

radio
preamplifier 1
11
10
6
7
5
4
3
7Z84951
STABILIZER 1
STABILIZER 2
MOTOR REGULATOR
k
V_{ref}
8
RADIO/PLAYBACK SWITCH
STABILIZER 3
9
preamplifier 2
14
FAST WIND SWITCH
13
TDA1506
AUTO-REVERSE CIRCUIT
1
V_P
12
STOP CIRCUIT
STOP INFORMATION
16
LED DRIVER
2
15
commutator pulses

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Limited output current	$I_{4\,lim}$	max.	1 A
Power dissipation	see Fig. 2		
Storage temperature range	T_{stg}	−65 to + 150	°C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient	$R_{th\,j\text{-}a}$	=	55 K/W

DEVELOPMENT SAMPLE DATA

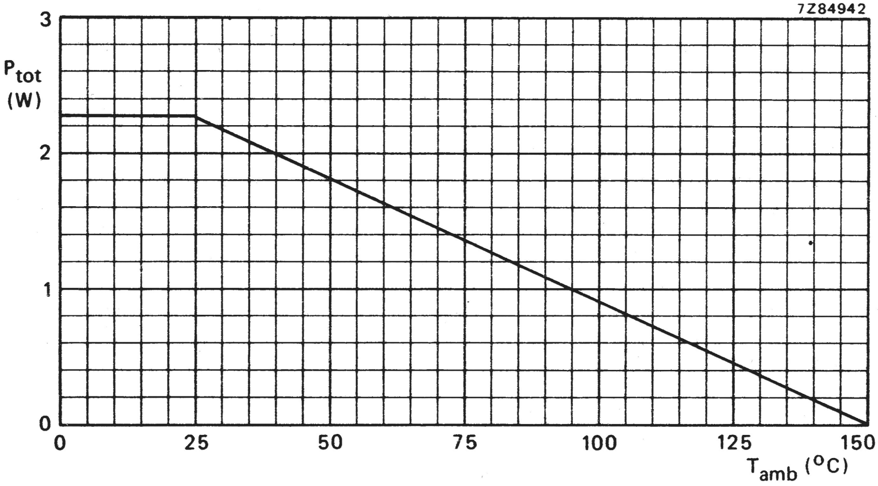


Fig. 2 Power derating curve.

Note to Fig. 2

$$P_{tot} = \frac{T_{j\,max} - T_{amb}}{R_{th\,j\text{-}a}}$$

P_{tot} in playback position (see Figure 3):

$$P_{tot} \approx I_{12} \times V_P + V_{4\text{-}3}\left(I_m + \frac{V_{ref}}{R_2}\right) + \left(V_{4\text{-}3} + V_{ref}\right)\left(\frac{I_4}{k} + I_q\right) - I_2 \times V_{2\text{-}8} - I_9 \times V_{9\text{-}8} - I_{10} \times V_{10\text{-}8}$$

P_{tot} in radio reception is much lower than P_{tot} in playback.

CHARACTERISTICS

V_P = 14,4 V; T_{amb} = 25 °C; I_4 = 70 mA; I_{11} = 45 mA; I_{10} = 0,3 mA; I_2 = 18 mA; I_9 = 2 mA; unless otherwise specified; see test circuit Fig. 3.

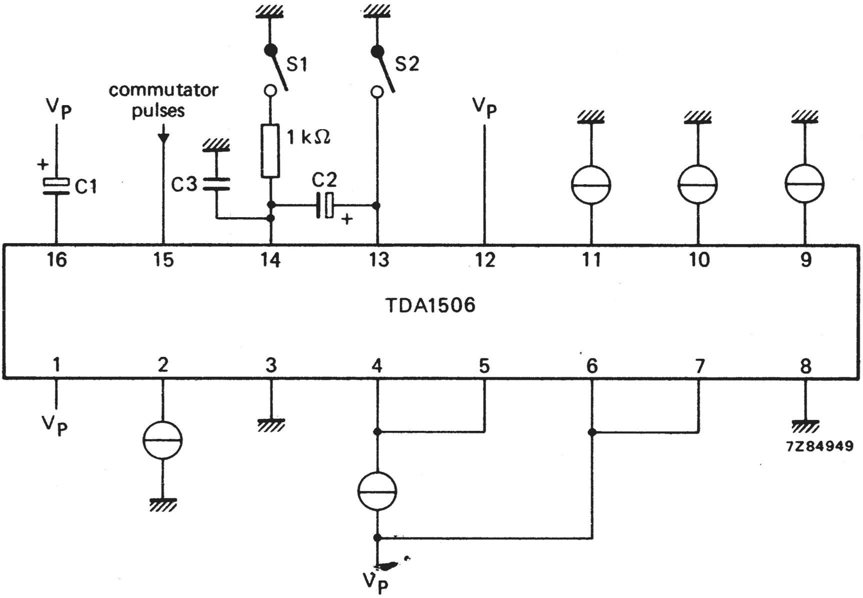
	symbol	min.	typ.	max.	unit	conditions
General						
Supply voltage	V_P	10 *	–	16	V	
Current consumption						
at playback	I_{12}	–	–	38	mA	$I_4 = 0$
at radio	I_{12}	–	–	64	mA	
Motor regulator						
Supply voltage	$V_{6\text{-}3}$	3,2	–	12	V	
Drop-out voltage	$V_{4\text{-}3}$	–	–	1,8	V	$\Delta V_{ref} = \pm$ 2%
Internal reference voltage	$V_{ref} = V_{6\text{-}5}$	1,32	1,38	1,44	V	$V_{6\text{-}3}$ = 8,7 V
Quiescent current	I_q	–	1,5	2,5	mA	$I_4 = 0$; $V_{6\text{-}3}$ = 8,7 V
Limited output current	$I_{4\ lim}$	0,5	–	–	A	$V_{6\text{-}3}$ = 8,7 V
Multiplication coefficient	$k = \Delta I_4/\Delta I_6$	18,5	20,5	22,5		$V_{6\text{-}3}$ = 8,7 V; $\Delta I_4 = \pm$ 10 mA
Line regulation variation						
V_{ref} versus V_P	$\frac{\Delta V_{ref}}{\Delta V_P} \times \frac{100\%}{V_{ref}}$	0	0,05	0,09	%/V	V_P = 3,2 to 12 V
k versus V_P	$\frac{\Delta k}{\Delta V_P} \times \frac{100\%}{k}$	0	0,3	0,6	%/V	V_P = 3,2 to 12 V $\Delta I_4 = \pm$ 10 mA
I_q versus V_P	$\frac{\Delta I_q}{\Delta V_P} \times \frac{100\%}{I_q}$	–	1,25	–	%/V	V_P = 3,2 to 12 V $I_4 = 0$
Load regulation variation						
V_{ref} versus I_4	$\frac{\Delta V_{ref}}{\Delta I_4} \times \frac{100\%}{V_{ref}}$	–0,037	–0,018	–	%/mA	I_4 = 20 to 150 mA
k versus I_4	$\frac{\Delta k}{\Delta I_4} \times \frac{100\%}{k}$	–0,02	0	+0,02	%/mA	I_4 = 20 to 150 mA $\Delta I_4 = \pm$ 10 mA
Temperature coefficient variation						
V_{ref} versus T_{amb}	$\frac{\Delta V_{ref}}{\Delta T_{amb}} \times \frac{100\%}{V_{ref}}$	0	0,025	0,045	%/K	T_{amb} = –20 to +80 °C $V_{6\text{-}3}$ = 8,7 V
k versus T_{amb}	$\frac{\Delta k}{\Delta T_{amb}} \times \frac{100\%}{k}$	–0,016	0,008	0,032	%/K	T_{amb} = –20 to +80 °C $V_{6\text{-}3}$ = 8,7; $\Delta I_4 = \pm$10 mA
I_q versus T_{amb}	$\frac{\Delta I_q}{\Delta T_{amb}} \times \frac{100\%}{I_q}$	–	0,13	–	%/K	T_{amb} = –20 to +80 °C $V_{6\text{-}3}$ = 8,7 V; $I_4 = 0$
Saturation voltage fast winding	$V_{7\text{-}4\ sat}$	–	0,18	–	V	I_7 = 10 mA (max. 50 mA)
Input current (pin 5)	I_5	–	19	–	μA	$V_{6\text{-}3}$ = 8,7 V

* For starting conditions: min. 6 V.

	symbol	min.	typ.	max.	unit	conditions
Automatic motor stop						
Output current (pin 15)	I_{15}	0,4	–	0,9	mA	
Time constant	t_{st}	–	700	–	ms	C1 = 47 μF ± 1%; Fig. 4
Switching level	$V_{16\text{-}8}$	–	9	–	V	
Stabilization radio						
Output voltage	$V_{11\text{-}8}$	8,5	8,9	9,3	V	
Limited output current	$I_{11\ lim}$	45	–	–	mA	
Variation of $V_{11\text{-}8}$	$\Delta V_{11\text{-}8}$	–	–	200	mV	V_P = 10,5 to 16 V
		–	100	–	mV/V	V_P = 10 to 10,5 V
Leakage current	I_{11}	–	–	0,5	μA	$R_{11\text{-}8}$ = 100 kΩ
	I_{11}	–	–	4	μA	$R_{11\text{-}8}$ = 100 kΩ T_{amb} = 80 °C
Temperature coefficient	$\Delta V_{11\text{-}8}/\Delta T_{amb}$	–2	0	+2	mV/K	T_{amb} = –20 to +80 °C
Stabilization preamp. I						
Output voltage	$V_{10\text{-}8}$	7,7	8,1	–	V	
Limited output current	$I_{10\ lim}$	2	–	–	mA	
Variation $V_{10\text{-}8}$ versus V_P	$\Delta V_{10\text{-}8}/\Delta V_P$	–	–	12	mV/V	V_P = 10,5 to 16 V
	$\Delta V_{10\text{-}8}/\Delta V_P$	–	5	–	mV/V	V_P = 10 to 10,5 V
Stabilization preamp. II						
Output voltage	$V_{9\text{-}8}$	8,5	9,1	–	V	
Output voltage	$V_{9\text{-}8}$	–	0	0,5	V	fast rewind
Limited output current	$I_{9\ lim}$	20	–	–	mA	
Variation $V_{9\text{-}8}$ versus V_P	$\Delta V_{9\text{-}8}/\Delta V_P$	–	–	12	mV/V	V_P = 10,5 to 16 V
	$\Delta V_{9\text{-}8}/\Delta V_P$	–	10	–	mV/V	V_P = 10 to 10,5 V
Lamp driver						
Output voltage	$V_{2\text{-}8}$	13	13,4	–	V	
Limited output current	$I_{2\ lim}$	20	–	–	mA	
Blinking time	t_b	–	0,5	–	s	C1 = 47 μF; Fig. 4
Rejection voltage supply	ΔV_P	–	0,3	–	V	
Automatic replay output						
Output current; playback	I_1	–	–	10	μA	$V_{1\text{-}8} = V_P$
Output current; radio	I_1	300	500	–	μA	$V_{1\text{-}8} \geqslant 5$ V
Delay time	t_d	–	380	–	ms	C1 = 47 μF; Fig. 4

CHARACTERISTICS (continued)

	symbol	min.	typ.	max.	unit	conditions
Radio playback switch						
Switching levels						
to playback	$V_{14\text{-}8}$	–	–	2	V	V_P = 10 to 16 V
to radio	$V_{14\text{-}8}$	3,5	–	–	V	T_{amb} = –20 to +80 °C
Input impedance	$\lvert Z_{14\text{-}8}\rvert$	–	20	–	kΩ	
Output current	I_{14}	–	200	–	µA	$V_{14\text{-}8} = 0$
Fast wind switch						
Switching levels						
normal to fast	$V_{13\text{-}8}$	–	–	2	V	V_P = 10 to 16 V
fast to normal	$V_{13\text{-}8}$	6	–	–	V	T_{amb} = –20 to +80 °C
Output voltage; playback	$V_{13\text{-}8}$	–	6,8	–	V	
Output current; fast wind	I_{13}	–	500	–	µA	$V_{13\text{-}8} = 0$
Output impedance	$\lvert Z_{13\text{-}8}\rvert$	–	13	–	kΩ	


S1
S2
VP
commutator pulses
1 kΩ
C1
C3
C2
+
+
VP
16
15
14
13
12
11
10
9
TDA1506
1
2
3
4
5
6
7
8
VP
7Z84949
VP

S1 closed: playback
S1 open: radio reception
S2 closed: fast speed
S2 open: normal speed

C2 is only used with sets on which a fast rewind key is available (C2 = 2,2 µF).
C1 is 200 µF maximum (typ. 47 µF).
C3 = 100 nF.

Fig. 3 Test circuit.

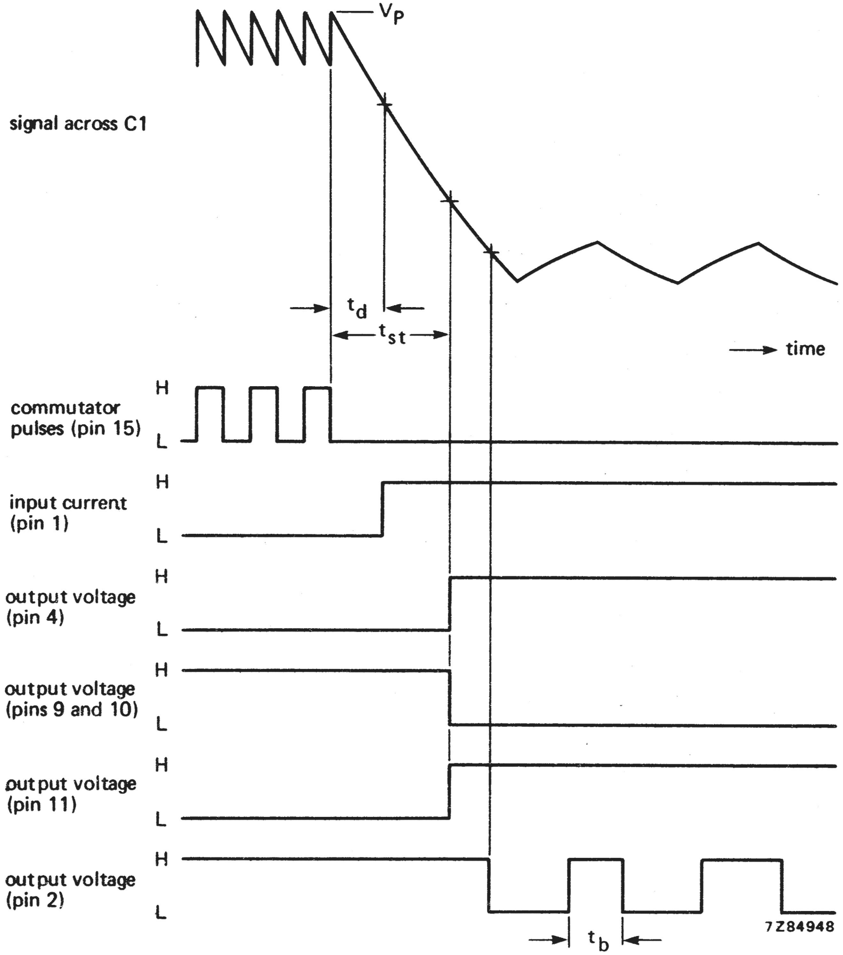

V_P
signal across C1
t_d
t_st
→ time
H
commutator pulses (pin 15)
L
H
input current (pin 1)
L
H
output voltage (pin 4)
L
H
output voltage (pins 9 and 10)
L
H
output voltage (pin 11)
L
H
output voltage (pin 2)
L
t_b
7Z84948

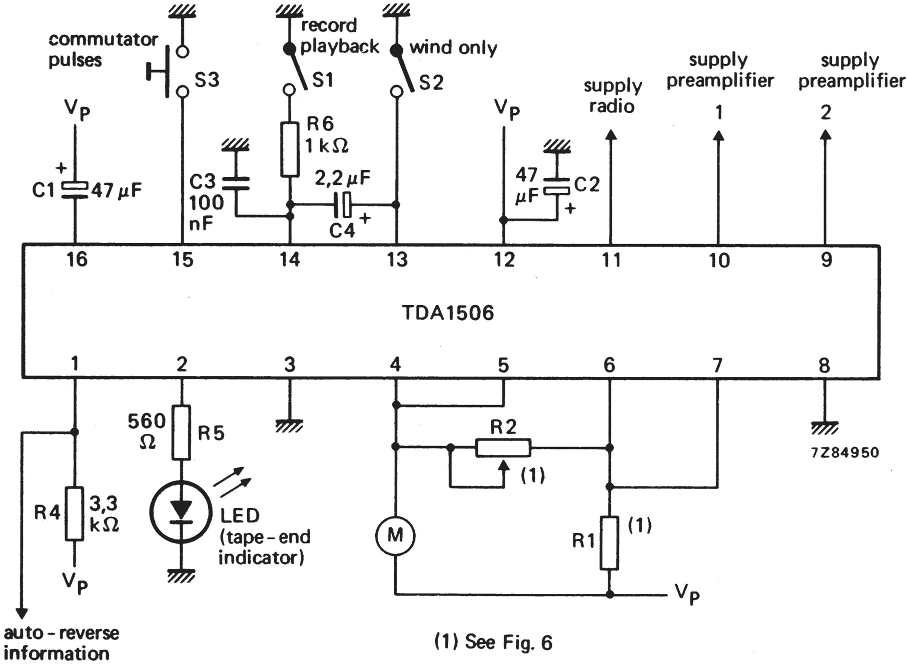
Fig. 4 Waveforms showing signal levels and time constants.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

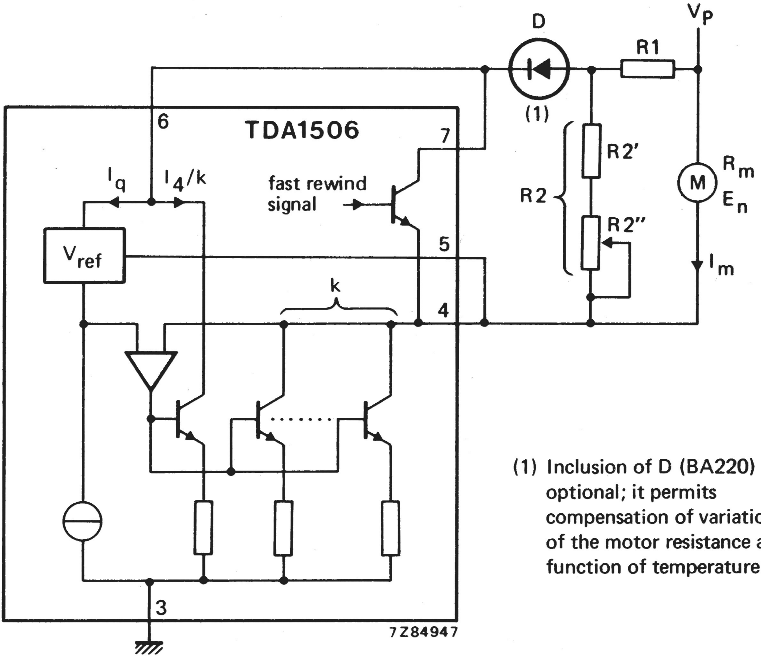
DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION


commutator pulses
S3
record
playback
S1
wind only
S2
VP
C1
47 µF
C3
100 nF
R6
1 kΩ
2,2 µF
C4
47 µF
C2
supply radio
supply preamplifier 1
supply preamplifier 2
16
15
14
13
12
11
10
9
TDA1506
1
2
3
4
5
6
7
8
560 Ω
R5
R2
(1)
R4
3,3 kΩ
LED (tape-end indicator)
M
R1
auto-reverse information
7Z84950

(1) See Fig. 6

Fig. 5 Typical simplified application circuit diagram.



(1) Inclusion of D (BA220) is optional; it permits compensation of variation of the motor resistance as function of temperature.

Fig. 6 Example of using the TDA1506 (only the motor regulation part is shown) in a d.c. motor speed regulation circuit.

Notes to Fig. 6

$R2 = R2' + R2''$

$E_n = n \times C \times \phi$

$I_m = T \times \frac{2\pi}{60} \times \frac{1}{C.\phi}$

where: n = speed in revolutions per minute
C = motor constant
ϕ = magnetic flux
E_n = electromotive force
T = motor torque
R_m = motor resistance

Example:

$E_n = E_{2400} = 5{,}24$ V(±12,2%)
$R_m = 25{,}6\ \Omega(\pm 10\%)$
n = 2400 rev/min
T = 1,3 mNm
R1 = 430 Ω
R2' = 110 Ω
R2'' = 220 Ω

E_n can be expressed (excluding diode D) as:

$$E_n = I_m \left(\frac{R1}{k} - R_m\right) + V_{ref}\left\{1 + \frac{R1}{R2}\left(1 + \frac{1}{k}\right)\right\} + R1 \times I_q$$

For optimal regulation (dn/dT = 0), $\left(\frac{R1}{k} - R_m\right)$ should be zero.

However, if $R1 = k \times R_m$, the regulator will be oscillating, so for stability always $R1 < k \times R_m$.

R2 is determined by:

$$R2 = \frac{V_{ref} \times R1 \times \left(1 + \frac{1}{k}\right)}{E_n - (R1 \times I_q) - V_{ref} - I_m\left(\frac{R1}{k} - R_m\right)}$$

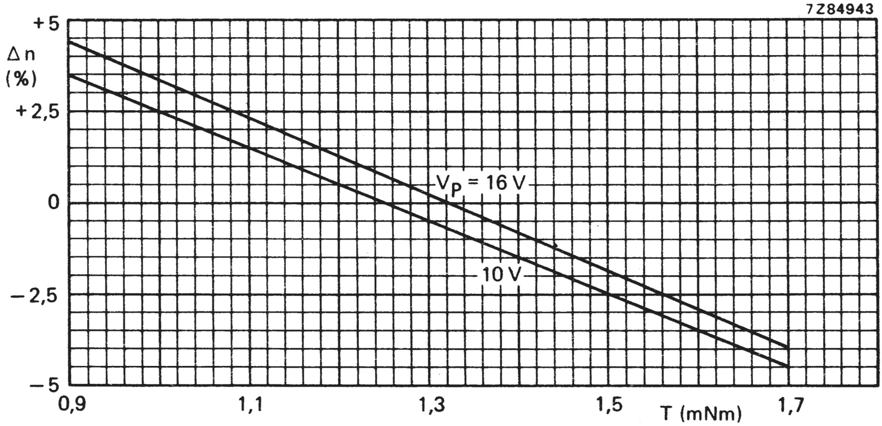


Fig. 7 Variation in motor speed (n is revolutions per minute) as a function of the applied motor torque at T_{amb} = 25 °C.

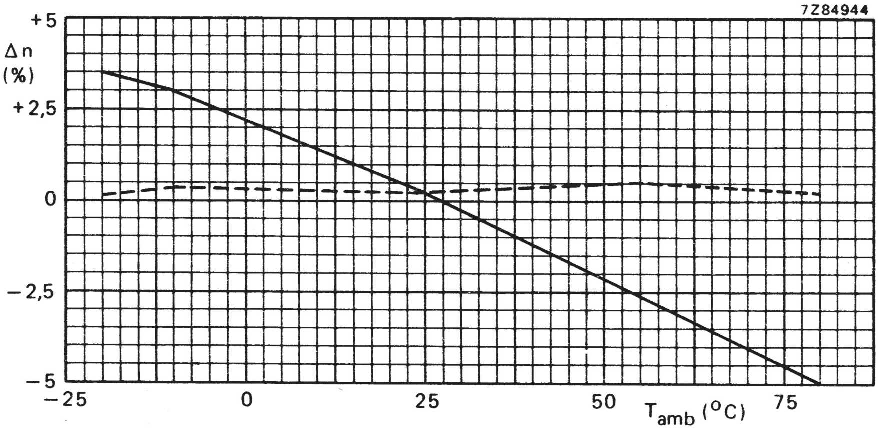


Fig. 8 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature at T = 1,3 mNm nominal and V_P = 16 V.

―――――――: with diode D (see Fig. 6).

– – – – – – – : without diode.

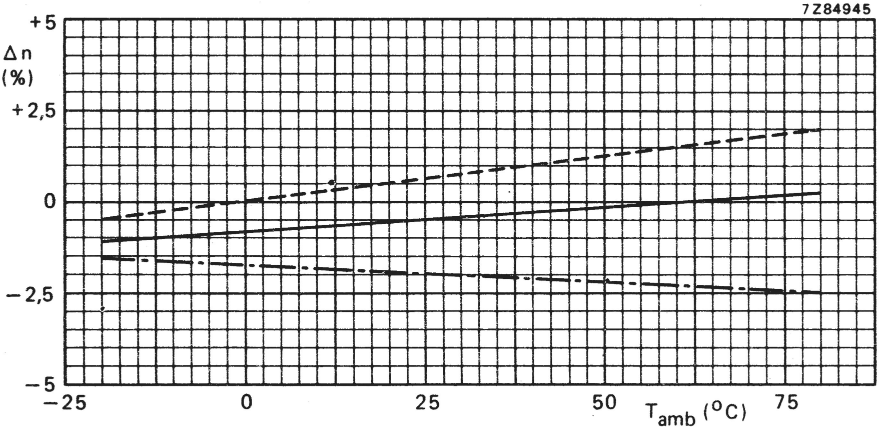


Fig. 9a V_P = 10 V.

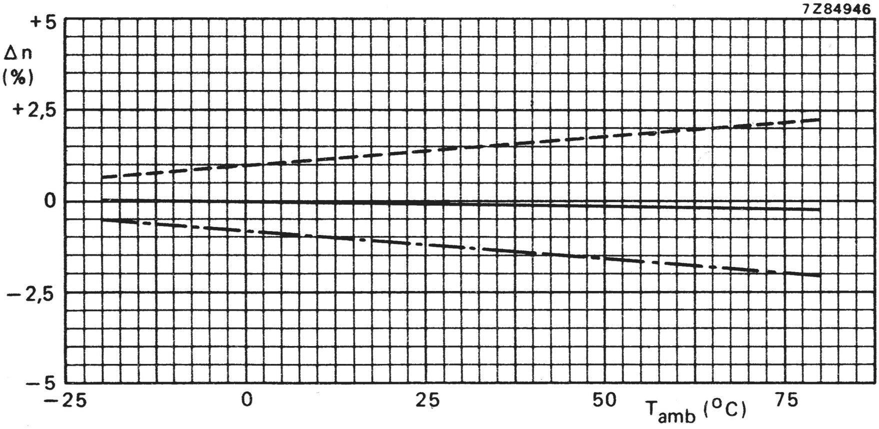


Fig. 9b V_P = 16 V.

Fig. 9 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature without diode (see Fig. 6).

— — — — — -: T = 1,17 mNm
——————: T = 1,30 mNm
—· —· —·-: T = 1,43 mNm

AUTO–REVERSE CAR RADIO CASSETTE–DECK STEERING CIRCUIT

GENERAL DESCRIPTION

The TDA1508 is a monolithic integrated circuit generating the steering signals needed for an auto-reverse car radio cassette-deck.

The TDA1508 incorporates the following functions:

- RC-oscillator generating the 250 kHz system clock
- Logic block (I^2L)
- Power-on-reset circuit
- Input interface circuits
- Output interface circuits
- Two output voltage stabilizers
- 4 ms motor-pause-pulse
- Fast wind pulse
- Muting pulse
- 1024 ms clock pulse for cassette rotation control.

QUICK REFERENCE DATA

Supply voltage range (pin 7)	V_P		10 to 18	V
Supply voltage range, standby (pin 12)	V_{SB}		3,5 to 18	V
Operating ambient temperature range	T_{amb}		−30 to +85	°C
Supply current (pin 7)	I_P	max.	15	mA
Supply current standby (pin 12)	I_{SB}	typ.	1,5	mA

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102).

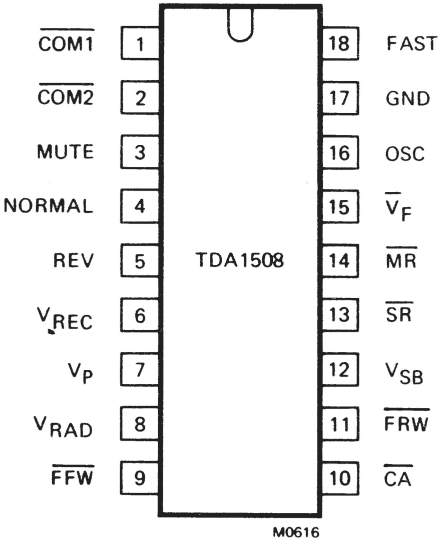

COM1
COM2
MUTE
NORMAL
REV
VREC
VP
VRAD
FFW
1
2
3
4
5
6
7
8
9
TDA1508
18
17
16
15
14
13
12
11
10
FAST
GND
OSC
VF
MR
SR
VSB
FRW
CA
M0616

Fig.1 Pinning diagram

PINNING

1.	$\overline{\text{COM1}}$	commutator logic input 1
2.	$\overline{\text{COM2}}$	commutator logic input 2
3.	MUTE	audio mute output
4.	NORMAL	motor control output
5.	REV	motor control output
6.	V_{REC}	recording power supply
7.	V_P	linear part power supply
8.	V_{RAD}	radio power supply
9.	$\overline{\text{FFW}}$	fast forward wind input
10.	$\overline{\text{CA}}$	cassette contact input
11.	$\overline{\text{FRW}}$	fast rewind input
12.	V_{SB}	standby supply control input
13.	$\overline{\text{SR}}$	tape-end input
14.	$\overline{\text{MR}}$	manual reverse input
15.	$\overline{V_F}$	radio mode input
16.	OSC	oscillator RC input
17.	GND	ground
18.	FAST	motor control output

DEVELOPMENT SAMPLE DATA

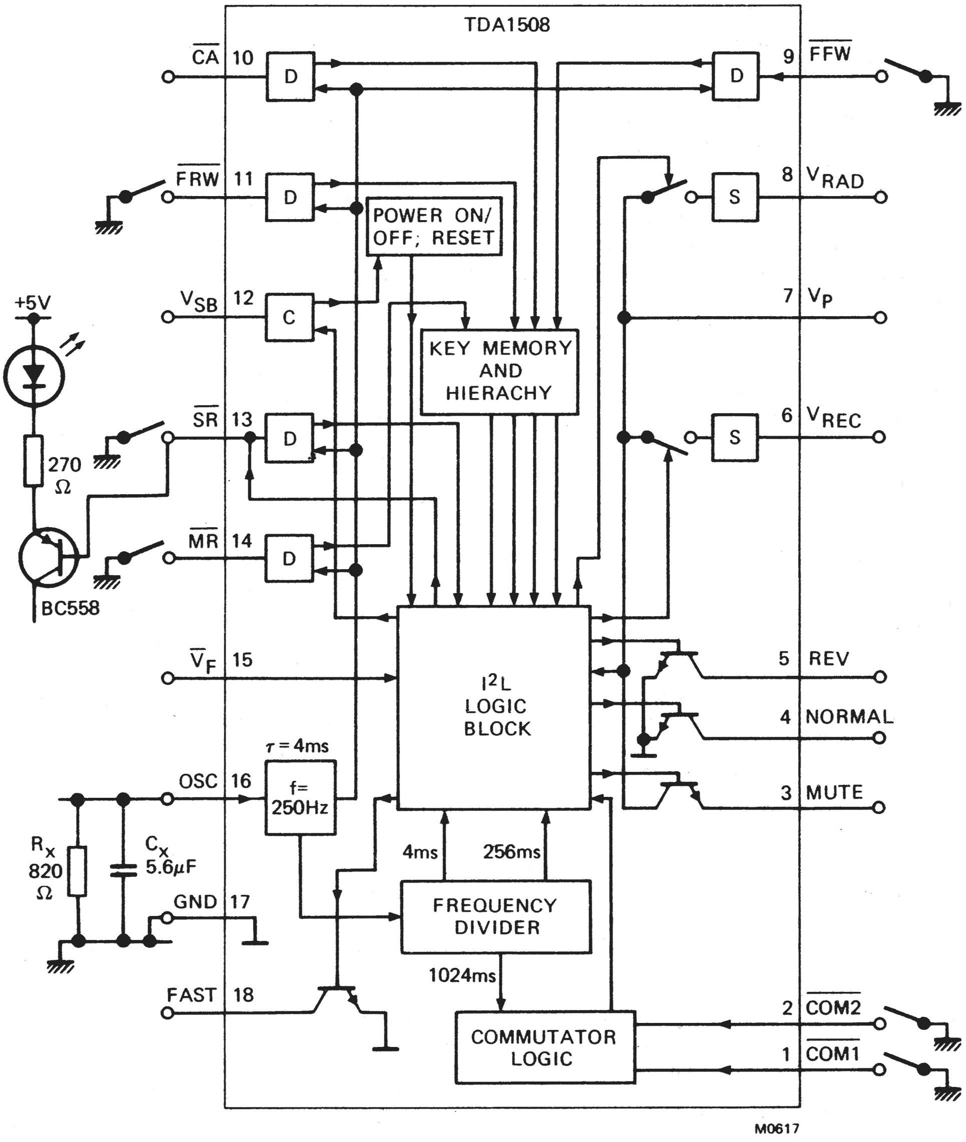

TDA1508
CA 10
D
9 FFW
D
FRW 11
D
POWER ON/ OFF; RESET
8 VRAD
S
+5V
VSB 12
C
7 VP
KEY MEMORY AND HIERACHY
270 Ω
SR 13
D
6 VREC
S
MR 14
D
BC558
VF 15
I2L LOGIC BLOCK
5 REV
4 NORMAL
τ = 4ms
OSC 16
f= 250Hz
3 MUTE
Rx 820 Ω
Cx 5.6μF
4ms
256ms
GND 17
FREQUENCY DIVIDER
1024ms
FAST 18
COMMUTATOR LOGIC
2 COM2
1 COM1
M0617

Fig.2 Block diagram

C = control for standby supply; D = debounce circuit; S = voltage stabilizer

FUNCTIONAL DESCRIPTION

General

The circuit incorporates an I^2L logic block which generates any specific control signal and delay time needed in the auto-reverse car radio cassette-deck. A power-on reset element resets the I^2L logic block when the standby supply V_{SB} is connected to the logic block. This standby voltage maintains the state of the logic part of the IC after the supply voltage for the linear part of the IC, V_P, has been switched off. The circuit uses an external RC network with an on-chip oscillator to generate a 250 Hz system clock.

Input interface circuits convert the $\overline{V_F}$, $\overline{\text{COM1}}$, $\overline{\text{COM2}}$, $\overline{\text{MR}}$, $\overline{\text{FRW}}$, $\overline{\text{FFW}}$, $\overline{\text{SR}}$ and $\overline{\text{CA}}$ information to I^2L logic levels; output interface circuits activate the open-collector outputs REV, NORMAL, FAST and $\overline{\text{SR}}$. The n-p-n transistor at the MUTE output is switched by logic levels from the I^2L logic block. Two output voltage stabilizers, supplied from V_P provide supply voltages for the radio part, V_{RAD}, and for the cassette deck pre-amplifiers, V_{REC}, respectively.

Function

Each commutation applied to the cassette deck motor is preceded by a 4 ms motor-pause pulse. After any change in the direction of motor rotation a fast wind (FW) pulse (1020 ms) is generated. During the period of the FW pulse the motor supply voltage is increased, the motor speed also increasing at the same time.

Input signals

Signal 'bounce' is suppressed by means of a 32 ms control pulse.

$\overline{V_F}$ (pin 15). A LOW at this input causes the deck to enter the radio mode, where it provides traffic information. The cassette motor stops in the radio mode.

$\overline{\text{SR}}$ (pin 13) A LOW at the $\overline{\text{SR}}$ input sets a latch and activates a 2-bit counter. Pulses from $\overline{\text{COM1}}$ and COM2 enable the end of tapeside A to be recognized. When the end of tapeside A has been recognized the motor will reverse and tapeside B will be played. When both tapesides have been played the deck will revert to the radio mode. A HIGH at the $\overline{\text{SR}}$ input initiates the endless auto-reverse playback mode. The $\overline{\text{SR}}$ input can be used to indicate the operating mode (single or auto-reverse). If an external transistor is used in conjunction with a suitable LED indicator, the LED will light up when the $\overline{\text{SR}}$ input goes LOW in the single playback mode.

$\overline{\text{MR}}$ (pin 14) manual reverse. A LOW at the $\overline{\text{MR}}$ input reverses the direction of the cassette.

$\overline{\text{FRW}}$ (pin 11) fast rewind. A LOW at the input causes the cassette to go into the fast rewind mode. When the $\overline{\text{FRW}}$ key has been released (HIGH at pin 11) the cassette player continues in the playback mode.

$\overline{\text{FFW}}$ (pin 9) fast forward wind. A LOW at this pin starts the fast forward wind; releasing the $\overline{\text{FFW}}$ key causes the cassette to re-enter the playback mode.

$\overline{\text{CA}}$ (pin 10) cassette contact. Inserting a cassette into the player gives a LOW at this input. The player will always start in the playback mode playing the sound track of the cassette which corresponds to the upper label of the cassette.

$\overline{\text{COM1}}$ (pin 1) and $\overline{\text{COM2}}$ (pin 2). The impulses at these inputs arise from the rotation of the cassette turntables. In conjunction with signals at $\overline{\text{SR}}$ the end of a tapeside can be recognized. The minimum rotational speed of the cassette turntables is also controlled using impulses at these pins. During a period of 1024 ms a minimum count of pulses has to be detected for continuous operation.

V_P (pin 7) supply voltage for linear part. When V_P is LOW the output functions (V_{REC}, V_{RAD}, NORMAL, REV, FAST, $\overline{\text{SR}}$-indication) are inactive. The switching levels for V_P are shown in Fig. 5. The MUTE transistor remains active independent of the value of V_P, when the audio mute is required.

Output signals

FAST (pin 18), NORMAL (pin 4), REV (pin 5). These open-collector outputs steer the motor control of the cassette deck.

MUTE (pin 3). The audio output of the cassette is muted in the radio mode and during any change in motor rotation (reverse, fast forward wind, etc). The n-p-n transistor (Fig.2) is switched to V_P when muting is required. The audio frequency is muted up to 128 ms after the change of mode or motor rotation.

V_{REC} (pin 6), V_{RAD} (pin 8). These stabilized supply voltages are derived from V_P and provide power for the recording and radio part of the cassette system respectively When V_{RAD} is active V_{REC} is switched off and when V_{REC} is active V_{RAD} is switched off.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage linear (pin 7)	$V_P = V_{7-17}$	max.	24	V
Supply voltage standby (pin 12)	$V_{SB} = V_{12-17}$	max.	24	V
All inputs (pins 1,2,9,10,11,13,14 and 15)	$V_{1,2,9,10,11,13,14,15-17}$	max.	24	V
All inputs (pins 3,4,5,6,8,13 and 18)	$V_{3,4,5,6,8,13,18-17}$	max.	24	V
Storage temperature range	T_{stg}		−55 to +150	°C
Operating ambient temperature range	T_{amb}		−30 to +85	°C

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS

Supply voltage V_P = 14 V; V_{SB} = 18 V; T_{amb} = 25 °C

parameter	symbol	min.	typ.	max.	unit
Linear supply (pin 7)					
Supply voltage linear	V_P	10	14	18	V
Supply current linear for $I_{(V_{RAD})}$ and $I_{(V_{REC})}$ = 0	I_P	–	–	15	mA
Supply standby (pin 12)					
Supply voltage standby	V_{SB}	3,5	–	18	V
Supply current standby	I_{SB}	–	1,5	2,5	mA
Power-on-reset			see Fig.3		
Power-off-reset			see Fig.4		
Time constant of RC-combination at V_{SB} for power-on-reset	τ	300	–	–	μs
Oscillator					
Oscillator frequency (R_x = 820 kΩ; C_x = 5,6 nF)	f_{osc}	–	250	–	Hz
Oscillator frequency drift over temperature and supply voltage range	$\Delta f_{osc}/f_{osc}$	–20	–	+20	%
External components	R_x	680	820	–	kΩ
	C_x	–	5,6	22	nF
Oscillator a.c. voltage (peak-to-peak value)	$V_{osc(p\text{-}p)}$	–	–	1,0	V
Inputs					
$\overline{\text{COM1}}$, $\overline{\text{FFW}}$, $\overline{\text{FRW}}$, $\overline{\text{MR}}$ $\overline{\text{COM2}}$, $\overline{V_F}$ and $\overline{\text{SR}}$ $\overline{\text{CA}}$					
HIGH (inactive)	V_{IH}	2,5	–	V_P	V
(for $V_{IH} < V_P - 1.5$ V)	$-I_{IH}$	50	100	200	μA
LOW (active)	V_{IL}	–	–	0,6	V
	$-I_{IL}$	50	100	200	μA

parameter	symbol	min.	typ.	max.	unit
Outputs					
NORMAL, REV (open collector)					
Output active saturation voltage ($I_{sat} < 7$ mA)	$V_{4-17sat}$	–	–	0,3	V
	$V_{5-17sat}$	–	–	0,3	V
FAST					
Output active saturation voltage ($I_{sat} < 25$ mA)	$V_{18-17sat}$	–	–	0,3	V
MUTE					
Output voltage (n-p-n transistor switched to V_P)	V_{3-17}	–	V_P-2	–	V
Output current external resistor	$-I_3$	5	–	–	mA
MUTE					
Output inactive voltage	V_{3-17}	0	–	–	V
Output inactive current	$-I_3$	–	0	10	μA
$\overline{SR}$ as output stage (open collector)					
Saturation voltage at $I_{sat} = 1$ mA	$V_{13-17sat}$	–	–	0,4	V
Inactive current	$-I_{13}$	–	–	10	μA
Stabilized output voltages					
V_{RAD} voltage	V_{6-17}	8,1	8,5	8,9	V
V_{REC} voltage	V_{8-17}	8,1	8,5	8,9	V
Output current (foldback)	I_6	45	–	–	mA
	I_8	45	–	–	mA
Ripple rejection, f = 100 Hz $V_P = 10$ to 18 V	$\frac{V_{6-17}}{V_{7-17}}$	–	–	20	mV/V
	$\frac{V_{8-17}}{V_{7-17}}$	–	–	20	mV/V
Temperature drift	$\frac{V_{6-17}}{T_{amb}}$	−2	–	+2	mV/K
	$\frac{V_{8-17}}{T_{amb}}$	−2	–	+2	mV/K
Input resistance (I = 50 mA)	R_i	–	1	–	Ω
Stabilizer inactive currents	$-I_{RAD}$	100	–	–	μA
	$-I_{REC}$	100	–	–	μA

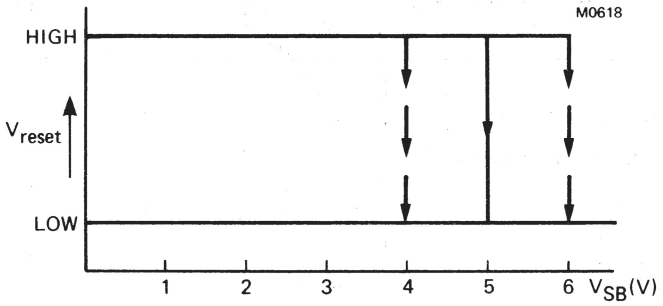


Fig.3 Power-on-reset.

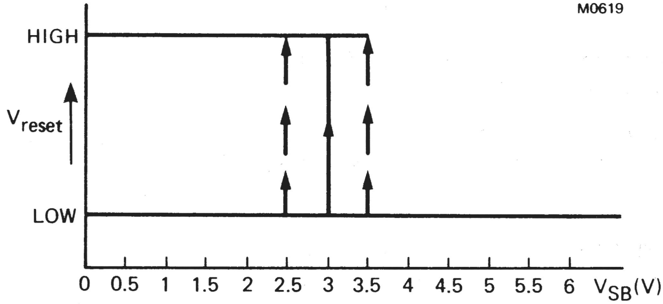


Fig.4 Power-off-reset.

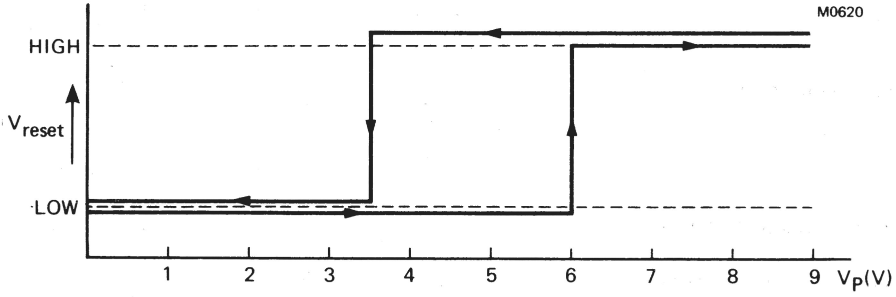


Fig.5 Switching levels for supply voltage monitoring.

24 W BTL OR 2 x 12 W STEREO CAR RADIO POWER AMPLIFIER

The TDA1510 is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1,6 Ω). At a supply voltage V_P = 14,4 V, an output power of 24 W can be delivered into a 4 Ω BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Special features are:

- flexibility in use — stereo as well as mono BTL
- high output power
- low offset voltage at the output (important for BTL)
- large useable gain variation
- very good ripple rejection
- load dump protection
- a.c. short-circuit safe to ground
- thermal protection
- internal limited bandwidth for high frequencies
- low stand-by current possibility, to simplify required switches
- low number and small sized external components
- high reliability

QUICK REFERENCE DATA

Supply voltage range (operating)	V_P		6 to 18	V
Supply voltage (non-operating)	V_P	max.	28	V
Supply voltage (non-operating; load dump protection)	V_P	max.	45	V
Repetitive peak output current	I_{ORM}	max.	4	A
Total quiescent current	I_{tot}	typ.	75	mA
Stand-by current	I_{sb}	<	2	mA
Switch-on current	I_{so}	typ.	0,35	mA
Input impedance	$\lvert Z_i \rvert$	>	1	MΩ
Storage temperature range	T_{stg}		−55 to + 150	°C
Crystal temperature	T_c	max.	150	°C

Bridge tied load application (BTL)	V_P	=	14,4	13,2	V
Output power at R_L = 4 Ω (with bootstrap)					
d_{tot} = 0,5%	P_o	typ.	18	15	W
d_{tot} = 10%	P_o	typ.	24	20	W
Ripple rejection; R_S = 0; f = 1 kHz	RR	typ.	50	50	dB
D.C. output offset voltage between the outputs	$\lvert \Delta V_{5\text{-}9} \rvert$	<	50	50	mV
Stereo application					
Output power at d_{tot} = 10% (with bootstrap)					
R_L = 4 Ω	P_o	typ.	7	6	W
R_L = 2 Ω	P_o	typ.	12	10	W
Output power at **d_{tot} = 0,5%** (with bootstrap)					
R_L = 4 Ω	P_o	typ.	5,5	4,5	W
R_L = 2 Ω	P_o	typ.	9,0	7,5	W
Channel separation	α	>	40	40	dB
Noise output voltage; R_S = 10 kΩ; according to IEC curve-A	V_n	typ.	0,3	0,2	mV

PACKAGE OUTLINE

13-lead SIL; plastic power (SOT-141B).

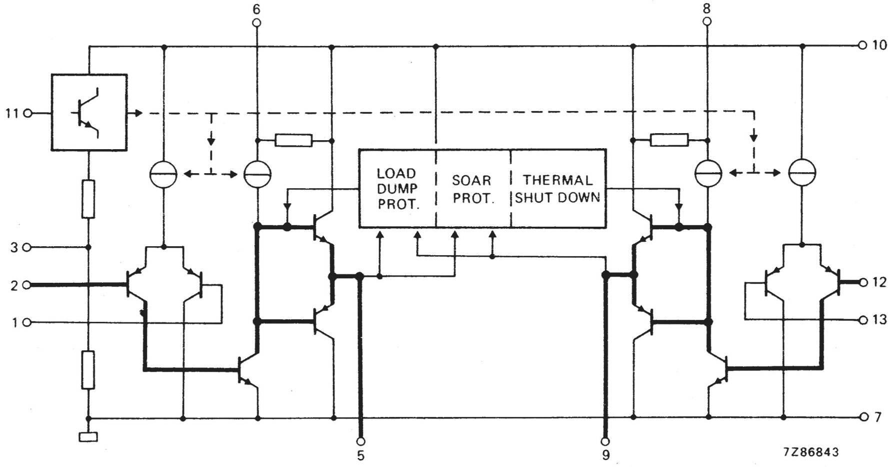

6
8
10
11
3
2
1
12
13
7
5
9
LOAD DUMP PROT.
SOAR PROT.
THERMAL SHUT DOWN
7Z86843

Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.
Pin 4 is internally connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 10)	V_P	max.	18	V
Supply voltage; non-operating	V_P	max.	28	V
Supply voltage; during 50 ms (load dump protection)	V_P	max.	45	V
Peak output current	I_{OM}	max.	6	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature range	T_{stg}	−55 to + 150		°C
Crystal temperature	T_c	max.	150	°C

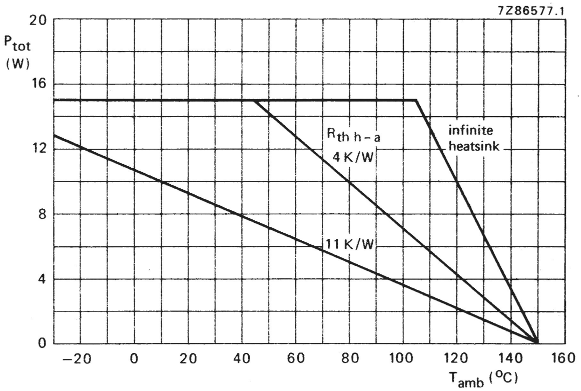


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω)

maximum sine-wave dissipation: 12 W

T_{amb} = 65 °C maximum

$$R_{th\ h\text{-}a} = \frac{150 - 65}{12} - 3 = 4\ \text{K/W}.$$

2 x 7 W stereo (4 Ω)

maximum sine-wave dissipation: 6 W

T_{amb} = 65 °C maximum

$$R_{th\ h\text{-}a} = \frac{150 - 65}{6} - 3 = 11\ \text{K/W}.$$

D.C. CHARACTERISTICS

Supply voltage range (pin 10)	V_P		6 to 18	V
Repetitive peak output current	I_{ORM}	<	4	A
Total quiescent current	I_{tot}	typ. <	75 150	mA mA
Stand-by current	I_{sb}	<	2	mA
Switch-on current (pin 11) at $V_{11} \leqslant V_{10}$ (note 1)	I_{so}	typ. <	0,35 0,8	mA mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; f = 1 kHz; unless otherwise specified

Bridge tied load application (BTL); see Fig. 3

Output power at R_L = 4 Ω (with bootstrap)				
V_P = 14,4 V; **d_{tot} = 0,5%**	P_o	> typ.	15,5 18,0	W W
V_P = 14,4 V; d_{tot} = 10%	P_o	> typ.	20 24	W W
V_P = 13,2 V; **d_{tot} = 0,5%**	P_o	typ.	15	W
V_P = 13,2 V; d_{tot} = 10%	P_o	typ.	20	W
Open loop voltage gain	G_o	typ.	75	dB
Closed loop voltage gain (note 2)	G_c	typ.	40 39,5 to 40,5	dB dB
Frequency response (note 3)	B		20 Hz to 20	kHz
Input impedance (note 4)	$\|Z_i\|$	>	1	MΩ
Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,2	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. <	0,35 0,8	mV mV
R_S = 10 kΩ; according to IEC curve A	V_n	typ.	0,25	mV
Ripple rejection (note 5)				
f = 100 Hz	RR	> typ.	42 50	dB dB
f = 1 to 10 kHz	RR	typ.	50	dB
D.C. output offset voltage between the outputs	$\|\Delta V_{5-9}\|$	<	50	mV
Loudspeaker protection (if one of the 2 outputs is short-circuited)				
maximum d.c. voltage (across the load)	$\|\Delta V_{5-9}\|$	<	1	V
Power bandwidth; –3 dB; **d_{tot} = 0,5%**	B		63 Hz to 12,5	kHz
Bootstrap current at onset of clipping	I_b	typ.	40	mA

Stereo application; see Fig. 4

Output power at d_{tot} = 10%; with bootstrap (note 6)			
V_P = 14,4 V; R_L = 4 Ω	P_o	>	6 W
		typ.	7 W
V_P = 14,4 V; R_L = 2 Ω	P_o	>	10 W
		typ.	12 W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	6 W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	10 W
Output power at **d_{tot} = 0,5%**; with bootstrap (note 6)			
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	5,5 W
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	9,0 W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	4,5 W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	7,5 W
Output power at d_{tot} = 10%; without bootstrap			
V_P = 14,4 V; R_L = 4 Ω (notes 6 and 8)	P_o	typ.	6 W
Frequency response (note 3)	B		40 Hz to 20 kHz
Supply voltage ripple rejection ripple voltage V_i = 200 mV; R_S = 0 Ω			
f = 1 kHz	RR	typ.	50 dB
Channel separation; R_S = 10 kΩ; f = 1 kHz	α	>	40 dB
		typ.	50 dB
Closed loop voltage gain (note 7)	G_c	typ.	40 dB
Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,15 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,25 mV
R_S = 10 kΩ; according to IEC curve A	V_n	typ.	0,2 mV
Bootstrap current at onset of clipping			
R_L = 4 Ω and 2 Ω	I_b	typ.	40 mA

Notes

1. If $V_{11} > V_{10}$, then I_{11} must be $\leqslant$ 10 mA.
2. Closed loop voltage gain can be chosen between 26 and 56 dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 20 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 to reach symmetrical clipping.

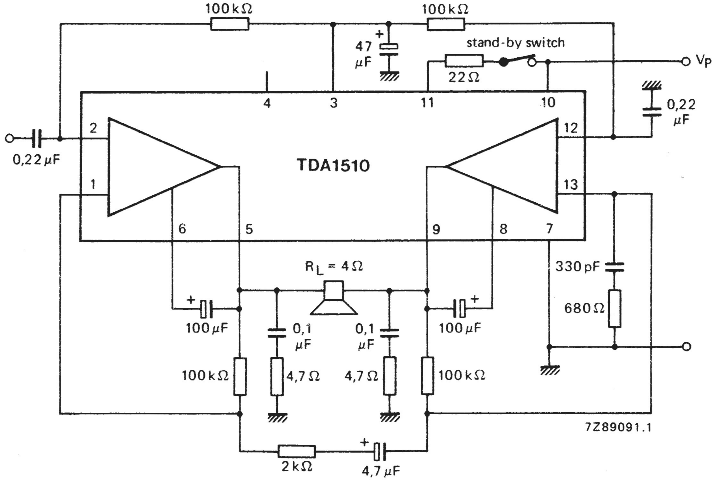

100 kΩ
100 kΩ
47 μF
stand-by switch
22 Ω
Vp
4
3
11
10
2
12
0,22 μF
0,22 μF
TDA1510
1
13
6
5
9
8
7
RL = 4 Ω
330 pF
680 Ω
100 μF
100 μF
0,1 μF
0,1 μF
100 kΩ
4,7 Ω
4,7 Ω
100 kΩ
7Z89091.1
2 kΩ
4,7 μF

Fig. 3 Test circuit bridge tied load (BTL).

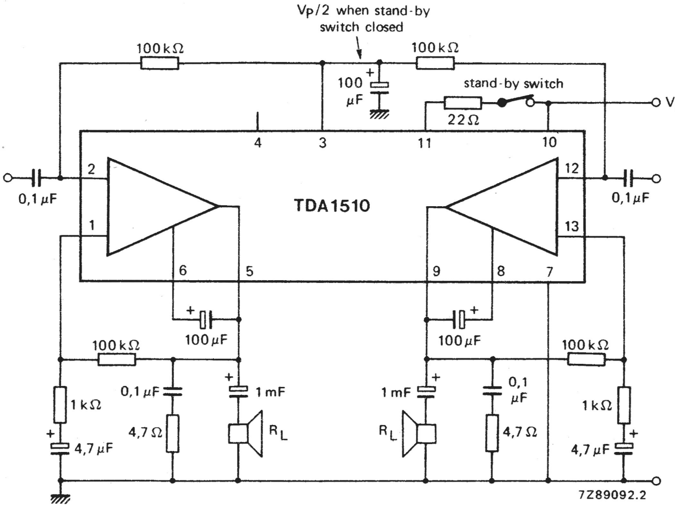

Vp/2 when stand-by switch closed
100 kΩ
100 kΩ
100 μF
stand-by switch
22 Ω
Vp
4
3
11
10
2
12
0,1 μF
0,1 μF
TDA1510
1
13
6
5
9
8
7
100 μF
100 μF
100 kΩ
100 kΩ
1 kΩ
4,7 μF
0,1 μF
4,7 Ω
1 mF
RL
1 mF
RL
0,1 μF
4,7 Ω
1 kΩ
4,7 μF
7Z89092.2

Fig. 4 Test circuit stereo application.

12 TO 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35	V
Total quiescent current at $V_P = 25$ V	I_{tot}	typ.	65	mA
Output power at $d_{tot} = 0{,}7\%$				
sine-wave power				
$V_P = 25$ V; $R_L = 4\ \Omega$	P_o	typ.	13	W
$V_P = 25$ V; $R_L = 8\ \Omega$	P_o	typ.	7	W
music power				
$V_P = 32$ V; $R_L = 4\ \Omega$	P_o	typ.	21	W
$V_P = 32$ V; $R_L = 8\ \Omega$	P_o	typ.	12	W
Closed-loop voltage gain (externally determined)	G_c	typ.	30	dB
Input resistance (externally determined)	R_i	typ.	20	kΩ
Signal-to-noise ratio at $P_o = 50$ mW	S/N	typ.	72	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	50	dB

PACKAGE OUTLINES

TDA1512: 9-lead SIL; plastic power (SOT-131B).
TDA1512Q: 9-lead SIL-bent-to-DIL; plastic power (SOT-157B).

PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Ground potential
5. Output
6. Positive supply (V_P)
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

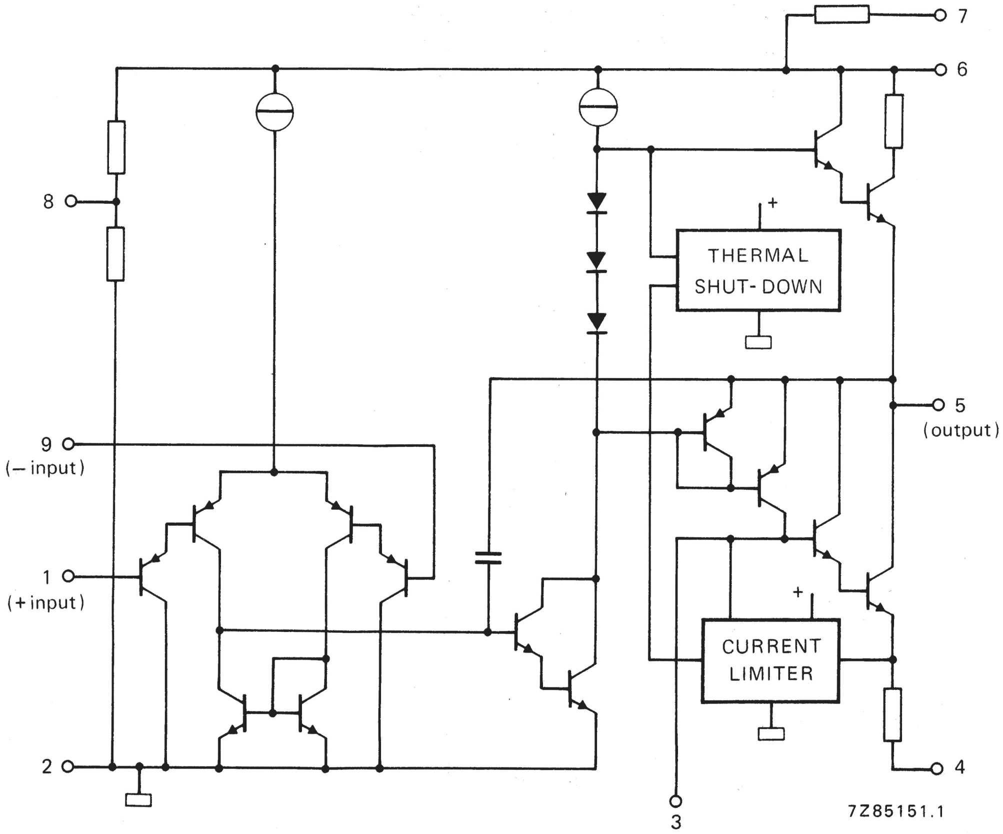
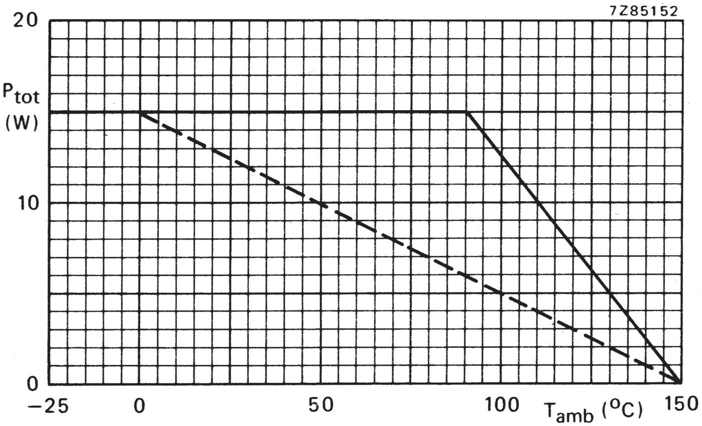

7
6
8
9
(– input)
1
(+ input)
2
THERMAL
SHUT-DOWN
+
5
(output)
CURRENT
LIMITER
+
3
4
7Z85151.1

Fig. 1 Simplified internal circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Repetitive peak output current	I_{ORM}	max.	3,2 A
Non-repetitive peak output current	I_{OSM}	max.	5 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 30$ V with $R_i = 4\ \Omega$	t_{sc}	max.	100 hours



——— mounted on infinite heatsink.

– – – – mounted on heatsink of 6 K/W.

Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	typ.	3 K/W
		$\leqslant$	4 K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 35	V
Total quiescent current at $V_P = 25$ V	I_{tot}	typ.	65	mA

A.C. CHARACTERISTICS

$V_P = 25$ V; $R_L = 4\ \Omega$; f = 1 kHz; $T_{amb} = 25\ ^{\circ}C$; measured in test circuit of Fig. 3; unless otherwise specified

Output power				
sine-wave power at $d_{tot} = 0,7$ %				
$R_L = 4\ \Omega$	P_o	typ.	13	W
$R_L = 8\ \Omega$	P_o	typ.	7	W
music power at $V_P = 32$ V				
$R_L = 4\ \Omega$; $d_{tot} = 0,7$ %	P_o	typ.	21	W
$R_L = 4\ \Omega$; $d_{tot} = 10$ %	P_o	typ.	25	W
$R_L = 8\ \Omega$; $d_{tot} = 0,7$ %	P_o	typ.	12	W
$R_L = 8\ \Omega$; $d_{tot} = 10$ %	P_o	typ.	15	W
Power bandwidth; −1,5 dB; $d_{tot} = 0,7$%	B		40 Hz to 16	kHz
Voltage gain				
open-loop	G_o	typ.	74	dB
closed-loop	G_c	typ.	30	dB
Input resistance (pin 1)	R_i	>	100	kΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20	kΩ
Input sensitivity				
for $P_o = 50$ mW	V_i	typ.	16	mV
for $P_o = 10$ W	V_i	typ.	210	mV
Signal-to-noise ratio				
at $P_o = 50$ mW; $R_S = 2\ k\Omega$; f = 20 Hz to 20 kHz; unweighted	S/N	>	68	dB
weighted; measured according to IEC 173 (A-curve)	S/N	typ.	76	dB
Ripple rejection at f = 100 Hz	RR	typ.	50	dB
Total harmonic distortion at $P_o = 10$ W	d_{tot}	typ. <	0,1 0,3	% %
Output resistance (pin 5)	R_o	typ.	0,1	Ω

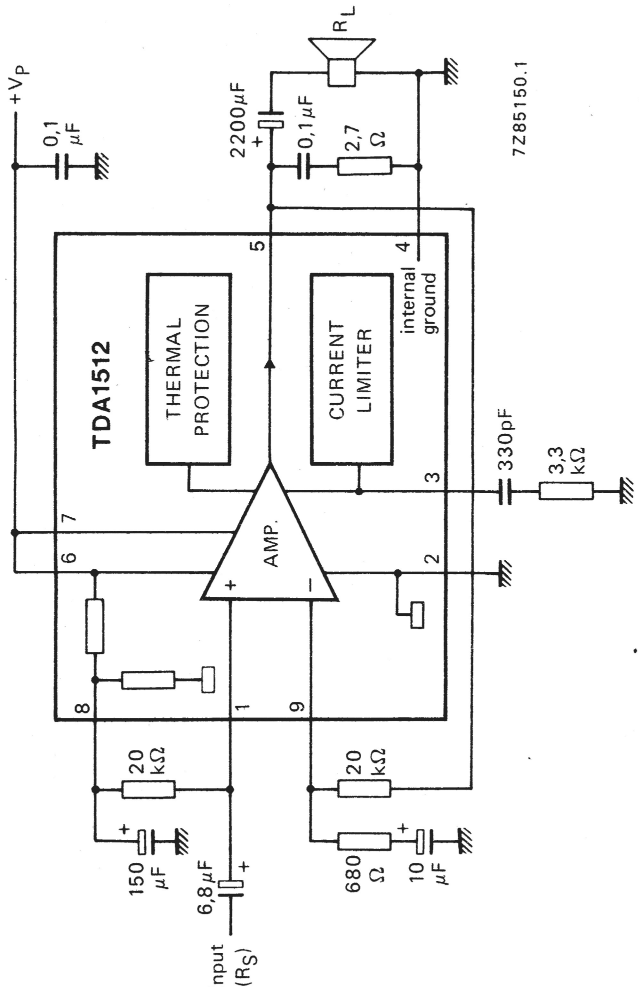

+V_P
0,1 μF
2200μF
0,1 μF
2,7 Ω
R_L
7Z85150.1
TDA1512
THERMAL PROTECTION
CURRENT LIMITER
AMP.
internal ground
330pF
3,3 kΩ
1
2
3
4
5
6
7
8
9
+
−
20 kΩ
20 kΩ
150 μF
6,8 μF
680 Ω
10 μF
input (R_S)

Fig. 3 Test circuit.

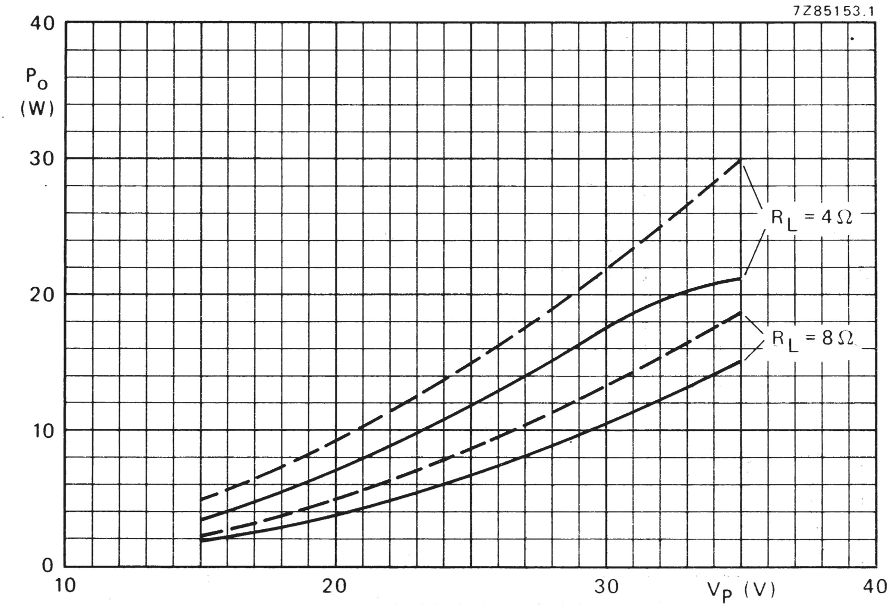


Fig. 4 Output power as a function of the supply voltage; f = 1 kHz; ——— d_{tot} = 0,7 %; – – – d_{tot} = 10 %.

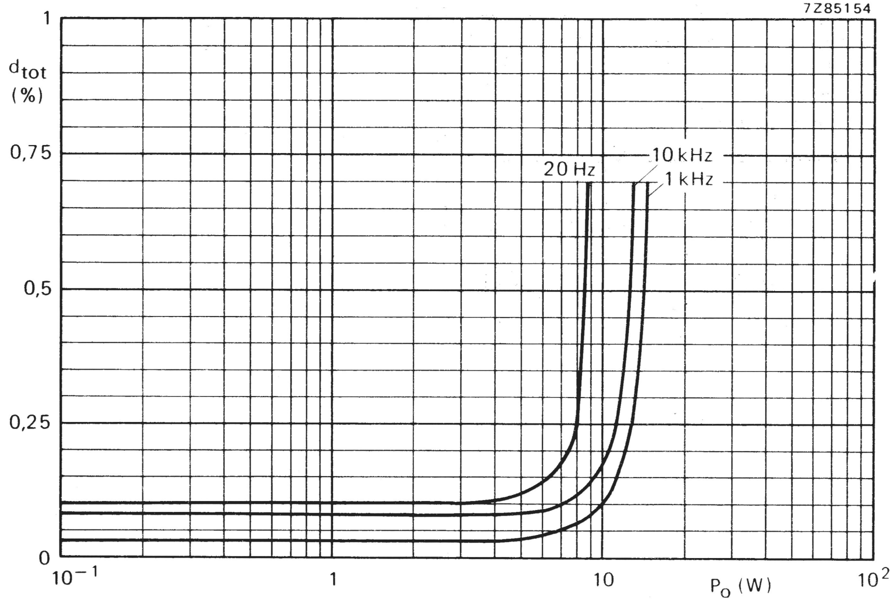


Fig. 5 Total harmonic distortion as a function of the output power.

24 W BTL OR 2 x 12 W STEREO CAR RADIO POWER AMPLIFIER

The TDA1515 is a monolithic integrated class-B output amplifier in a 13-lead single in-line (SIL) plastic power package. The device is primarily developed for car radio applications, and also to drive low-impedance loads (down to 1,6 Ω). At a supply voltage V_P = 14,4 V, an output power of 24 W can be delivered into a 4 Ω BTL (Bridge Tied Load), or, when used as stereo amplifier, it delivers 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Special features are:

- flexibility in use — mono BTL as well as stereo
- high output power
- low offset voltage at the output (important for BTL)
- large usable gain variation
- very good ripple rejection
- internal limited bandwidth for high frequencies
- low stand-by current possibility (typ. 0 μA), to simplify required switches; TTL drive possible
- low number and small sized external components
- high reliability

The following currently required protections are incorporated in the circuit. These protections also have positive influence on reliability in the applications.

- load dump protection
- **a.c. and d.c. short-circuit safe to ground up to V_P = 18 V**
- thermal protection
- speaker protection in bridge configuration
- complete SOAR protection
- outputs short-circuit safe in BTL

QUICK REFERENCE DATA

Supply voltage range (operating)	V_P		6 to 18	V
Supply voltage (non-operating)	V_P	max.	28	V
Supply voltage (non-operating; load dump protection)	V_P	max.	45	V
Repetitive peak output current	I_{ORM}	max.	4	A
Total quiescent current	I_{tot}	typ.	75	mA
Stand-by current	I_{sb}	typ.	0	μA
Switch-on current	I_{so}	<	100	μA
Input impedance	$\lvert Z_i \rvert$	>	1	MΩ
Storage temperature range	T_{stg}		−55 to + 150	°C
Crystal temperature	T_c	max.	150	°C

Bridge tied load application (BTL)	V_P	=	14,4	13,2	V
Output power at R_L = 4 Ω (with bootstrap)					
d_{tot} = 0,5%	P_o	typ.	18	15	W
d_{tot} = 10%	P_o	typ.	24	20	W
Ripple rejection; R_S = 0; f = 100 Hz to 15 kHz	RR	typ.	50	50	dB
D.C. output offset voltage between the outputs	$\lvert \Delta V_{5-9} \rvert$	<	50	50	mV
Stereo application					
Output power at d_{tot} = 10% (with bootstrap)					
R_L = 4 Ω	P_o	typ.	7	6	W
R_L = 2 Ω	P_o	typ.	12	10	W
Output power at **d_{tot} = 0,5%** (with bootstrap)					
R_L = 4 Ω	P_o	typ.	5,5	4,5	W
R_L = 2 Ω	P_o	typ.	9,0	7,5	W
Channel separation	α	>	40	40	dB
Noise output voltage; R_S = 10 kΩ; according to IEC curve-A	V_n	typ.	0,25	0,25	mV

PACKAGE OUTLINE 13-lead SIL; plastic power (SOT-141B).

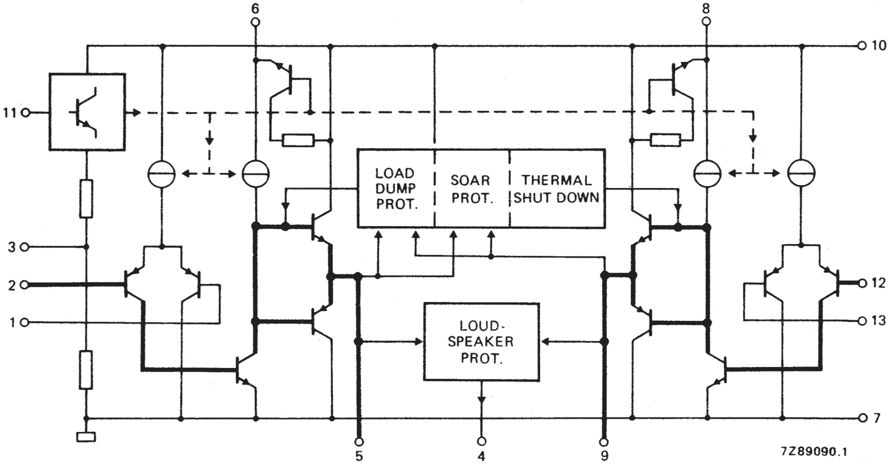

6
8
10
11
3
2
1
12
13
7
5
4
9
LOAD DUMP PROT.
SOAR PROT.
THERMAL SHUT DOWN
LOUD-SPEAKER PROT.
7Z89090.1

Fig. 1 Internal block diagram; the heavy lines indicate the signal paths.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage; operating (pin 10)	V_P	max.	18 V
Supply voltage; non-operating	V_P	max.	28 V
Supply voltage; during 50 ms (load dump protection)	V_P	max.	45 V
Peak output current	I_{OM}	max.	6 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	150 °C
A.C. and d.c. short-circuit safe voltage		max.	18 V

DEVELOPMENT SAMPLE DATA

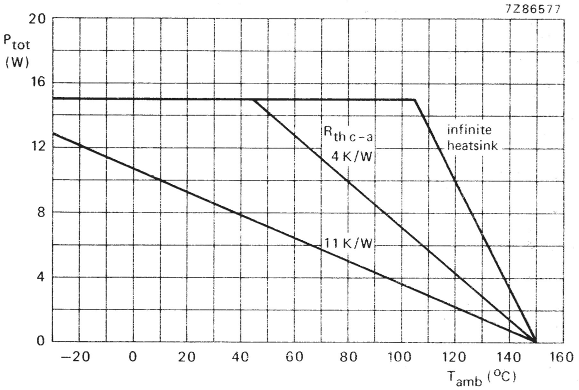


Fig. 2 Power derating curves.

HEATSINK DESIGN EXAMPLE

The derating of 3 K/W of the encapsulation requires the following external heatsink (for sine-wave drive):

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω)

maximum sine-wave dissipation: 12 W

T_{amb} = 65 °C maximum

$$R_{th\ h\text{-}a} = \frac{150-65}{12} - 3 = 4\ \text{K/W}.$$

2 x 7 W stereo (4 Ω)

maximum sine-wave dissipation: 6 W

T_{amb} = 65 °C maximum

$$R_{th\ h\text{-}a} = \frac{150-65}{6} - 3 = 11\ \text{K/W}.$$

D.C. CHARACTERISTICS

Supply voltage range (pin 10)	V_P		6 to 18	V
Repetitive peak output current	I_{ORM}	<	4	A
Total quiescent current	I_{tot}	typ.	75	mA
Switching level pin 11: OFF	V_{OFF}	<	1,8	V
ON	V_{ON}	>	3	V
Stand-by switch OFF ($V_{OFF} < 1{,}8$ V) impedance between pins 10 and 6; 10 and 8	$\lvert Z_{OFF} \rvert$	>	100	kΩ
Stand-by current at 0 to 0,8 V	I_{sb}	typ. <	1 200	μA μA
Switch-on current (pin 11) at $V_{11} \leqslant V_{10}$ (note 1)	I_{so}	typ. <	10 100	μA μA

A.C. CHARACTERISTICS

$T_{amb} = 25\ ^oC$; $V_P = 14{,}4$ V; f = 1 kHz; unless otherwise specified

Bridge tied load application (BTL); see Fig. 3

Output power at $R_L = 4\ \Omega$ (with bootstrap)				
$V_P = 14{,}4$ V; $\mathbf{d_{tot} = 0{,}5\%}$	P_o	> typ.	15,5 18,0	W W
$V_P = 14{,}4$ V; $d_{tot} = 10\%$	P_o	> typ.	20 24	W W
$V_P = 13{,}2$ V; $\mathbf{d_{tot} = 0{,}5\%}$	P_o	typ.	15	W
$V_P = 13{,}2$ V; $d_{tot} = 10\%$	P_o	typ.	20	W
Open loop voltage gain	G_o	typ.	75	dB
Closed loop voltage gain (note 2)	G_c	typ.	40 39,5 to 40,5	dB dB
Frequency response (note 3)	B		20 Hz to 20	kHz
Input impedance (note 4)	$\lvert Z_i \rvert$	>	1	MΩ
Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz				
$R_S = 0\ \Omega$	$V_{n(rms)}$	typ.	0,2	mV
$R_S = 10$ kΩ	$V_{n(rms)}$	typ. <	0,35 0,8	mV mV
$R_S = 10$ kΩ; according to IEC curve A	V_n	typ.	0,25	mV
Ripple rejection (note 5) f = 100 Hz to 15 kHz	RR	> typ.	42 50	dB dB
D.C. output offset voltage between the outputs	$\lvert \Delta V_{5\text{-}9} \rvert$	<	50	mV
Loudspeaker protection (all conditions) maximum d.c. voltage (across the load)	$\lvert \Delta V_{5\text{-}9} \rvert$	<	1	V
Power bandwidth; –0,5 dB; $\mathbf{d_{tot} = 0{,}5\%}$	B		20 Hz to 20	kHz
Bootstrap current at onset of clipping	I_b	typ.	40	mA

Stereo application; see Fig. 4

Output power at d_{tot} = 10%; with bootstrap (note 6)				
V_P = 14,4 V; R_L = 4 Ω	P_o	> typ.	6 7	W W
V_P = 14,4 V; R_L = 2 Ω	P_o	> typ.	10 12	W W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	6	W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	10	W
Output power at **d_{tot} = 0,5%**; with bootstrap (note 6)				
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	5,5	W
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	9,0	W
V_P = 13,2 V; R_L = 4 Ω	P_o	typ.	4,5	W
V_P = 13,2 V; R_L = 2 Ω	P_o	typ.	7,5	W
Output power at d_{tot} = 10%; without bootstrap				
V_P = 14,4 V; R_L = 4 Ω (notes 6 and 8)	P_o	typ.	6	W
Frequency response (note 3)	B		40 Hz to 20	kHz
Supply voltage ripple rejection; R_S = 0 Ω				
f = 1 kHz	RR	typ.	50	dB
Channel separation; R_S = 10 kΩ; f = 1 kHz	α	> typ.	40 50	dB dB
Closed loop voltage gain (note 7)	G_c	typ.	40	dB
Noise output voltage (r.m.s. value) at f = 20 Hz to 20 kHz				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,15	mV
R_S = 10 kΩ	$V_{n(rms)}$	typ.	0,25	mV
R_S = 10 kΩ; according to IEC curve A	V_n	typ.	0,2	mV
Bootstrap current at onset of clipping				
R_L = 4 Ω and 2 Ω	I_b	typ.	40	mA

Notes

1. If $V_{11} > V_{10}$, then $|Z_{11}| > 5$ kΩ.
2. Closed loop voltage gain can be chosen between 26 and 56 dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude: 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 20 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 to reach symmetrical clipping.

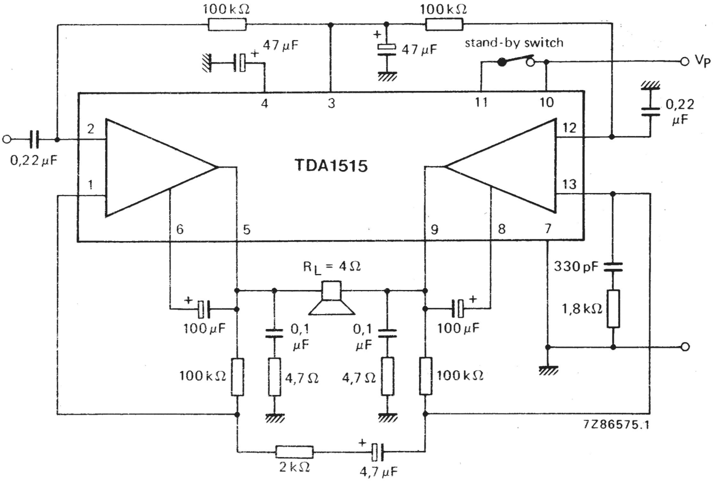

100 kΩ
100 kΩ
47 µF
47 µF
stand-by switch
Vp
4
3
11
10
0,22 µF
2
12
0,22 µF
TDA1515
1
13
6
5
9
8
7
RL = 4 Ω
330 pF
100 µF
0,1 µF
0,1 µF
100 µF
1,8 kΩ
100 kΩ
4,7 Ω
4,7 Ω
100 kΩ
7Z86575.1
2 kΩ
4,7 µF

Fig. 3 Test/application circuit bridge tied load (BTL).

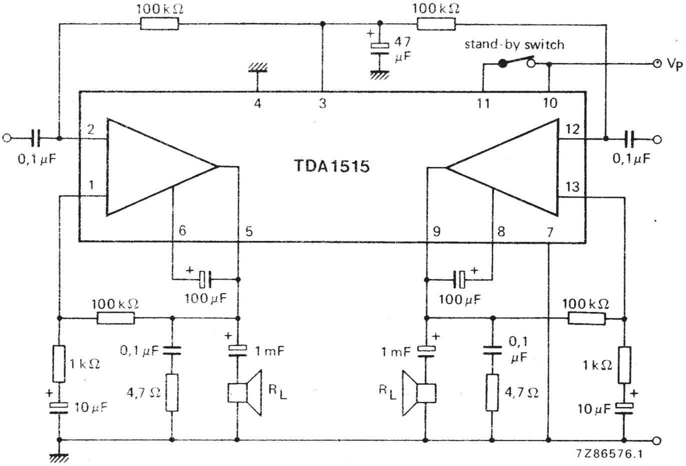

100 kΩ
100 kΩ
47 µF
stand-by switch
Vp
4
3
11
10
2
12
0,1 µF
0,1 µF
TDA1515
1
13
6
5
9
8
7
100 µF
100 µF
100 kΩ
100 kΩ
0,1 µF
1 mF
1 mF
0,1 µF
1 kΩ
1 kΩ
4,7 Ω
RL
RL
4,7 Ω
10 µF
10 µF
7Z86576.1

Fig. 4 Test/application circuit stereo.

20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1520 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Very low intermodulation distortion
- Very low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package
- A.C. short-circuit protected

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 40	V
Total quiescent current at $V_P = 33$ V	I_{tot}	typ.	45	mA
Output power at $d_{tot} = 0{,}5\%$				
sine-wave power				
$V_P = 33$ V; $R_L = 4\ \Omega$	P_o	typ.	22	W
$V_P = 33$ V; $R_L = 4\ \Omega$	P_o	>	20	W
$V_P = 33$ V; $R_L = 8\ \Omega$	P_o	typ.	11	W
Closed-loop voltage gain (externally determined)	G_c	typ.	30	dB
Input resistance (externally determined by R_{8-1})	R_i	typ.	20	kΩ
Signal-to-noise ratio at $P_o = 50$ mW	S/N	typ.	76	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	70	dB

PACKAGE OUTLINE

9-lead SIL; plastic power (SOT-131A).

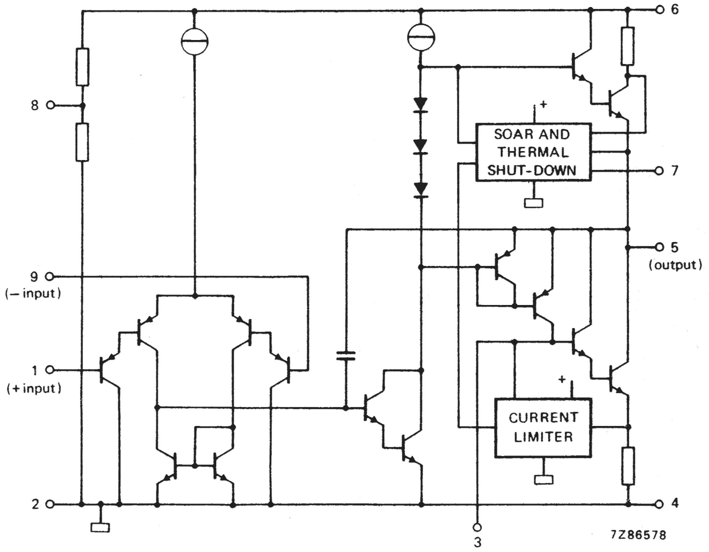

6
8
SOAR AND THERMAL SHUT-DOWN
+
7
5
(output)
9
(– input)
1
(+ input)
CURRENT LIMITER
+
2
3
4
7Z86578

Fig. 1 Simplified internal circuit diagram.

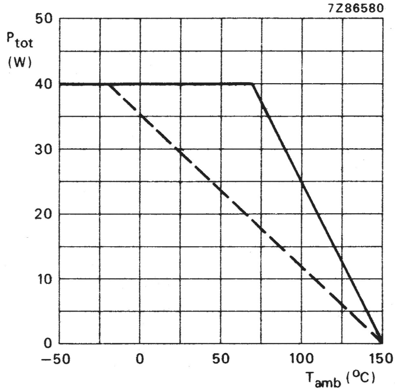
PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply (V_P)
7. Internally connected
8. Ripple rejection
9. Inverting input (feedback)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	44	V
Repetitive peak output current	I_{ORM}	max.	4	A
Non-repetitive peak output current	I_{OSM}	max.	5	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature	T_{amb}	−25 to + 150		°C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 28$ V with $R_i = 4\ \Omega$	t_{sc}	max.	100	hours



—— mounted on infinite heatsink.
– – – mounted on heatsink of 2,3 K/W.

Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	$\leqslant$	2	K/W

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 40 V
Total quiescent current at $V_P = 33$ V	I_{tot}	typ.	45 mA

A.C. CHARACTERISTICS

$V_P = 33$ V; $R_L = 4\ \Omega$; f = 1 kHz; $T_{amb} = 25\ ^oC$; measured in test circuit of Fig. 3; unless otherwise specified

Output power			
sine-wave power at $d_{tot} = 0{,}5\%$			
$R_L = 4\ \Omega$	P_o	typ.	22 W
$R_L = 4\ \Omega$	P_o	>	20 W
$R_L = 8\ \Omega$	P_o	typ.	11 W
Power bandwidth; –3 dB; $d_{tot} = 0{,}5\%$	B	20 Hz to	20 kHz
Voltage gain			
open-loop	G_o	typ.	74 dB
closed-loop	G_c	typ.	30 dB
Input resistance (pin 1)	R_i	>	1 MΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20 kΩ
Input sensitivity			
for $P_o = 50$ mW	V_i	typ.	16 mV
for $P_o = 16$ W	V_i	typ.	260 mV
Signal-to-noise ratio			
at $P_o = 50$ mW; $R_S = 2$ kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	typ.	76 dB
weighted; measured according to IEC 173 (A-curve)	S/N	typ.	80 dB
Ripple rejection at f = 100 Hz	RR	typ.	70 dB
Total harmonic distortion at $P_o = 16$ W	d_{tot}	typ.	0,01 %
Output resistance (pin 5)	R_o	typ.	0,01 Ω
	R_o	<	0,1 Ω

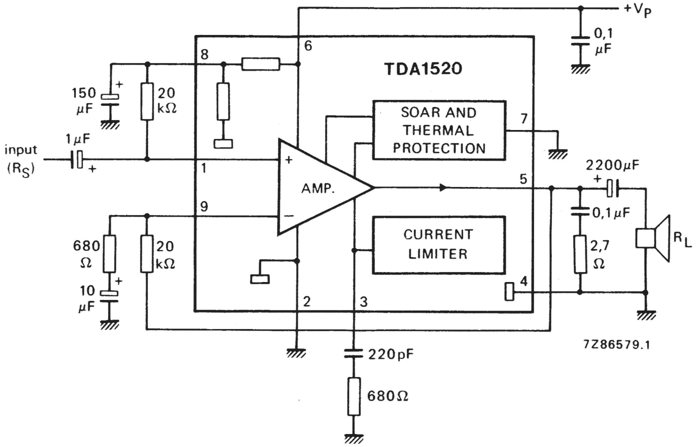

+VP
0,1 μF
TDA1520
6
8
150 μF
20 kΩ
SOAR AND THERMAL PROTECTION
7
input (RS)
1 μF
1
+
AMP.
−
5
2200μF
9
0,1μF
680 Ω
20 kΩ
CURRENT LIMITER
2,7 Ω
RL
10 μF
4
2
3
220pF
680Ω
7Z86579.1

Fig. 3 Test circuit.

STEREO CASSETTE HEAD PREAMPLIFIER AND EQUALIZER

GENERAL DESCRIPTION

The TDA1522 is a playback amplifier for car radio/cassette players.

Features

- Two independent amplifiers with open loop gain of typ. 90 dB
- Internal d.c. feedback via a 140 kΩ resistor from output to feedback point
- A.C. characteristics that can be determined externally by an RC network
- Electronic on/off switching with transient suppression for switch on
- Head input at d.c. ground that eliminates the input coupling capacitor
- Minimal external component requirement
- Stability down to a gain of 30 dB
- Low input noise
- Low distortion
- D.C. input current $< 2\ \mu A$
- Wide supply voltage range

QUICK REFERENCE DATA

Supply voltage range (pin 8)	V_P		7,5 to 23	V
Supply current (pin 8)	I_P	typ.	5	mA
Operating ambient temperature range	T_{amb}		−30 to +85	°C
Total harmonic distortion	THD	typ.	0,05	%
Channel separation at R_S = 10 kΩ; L_S = 0	α	min.	45	dB

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142).

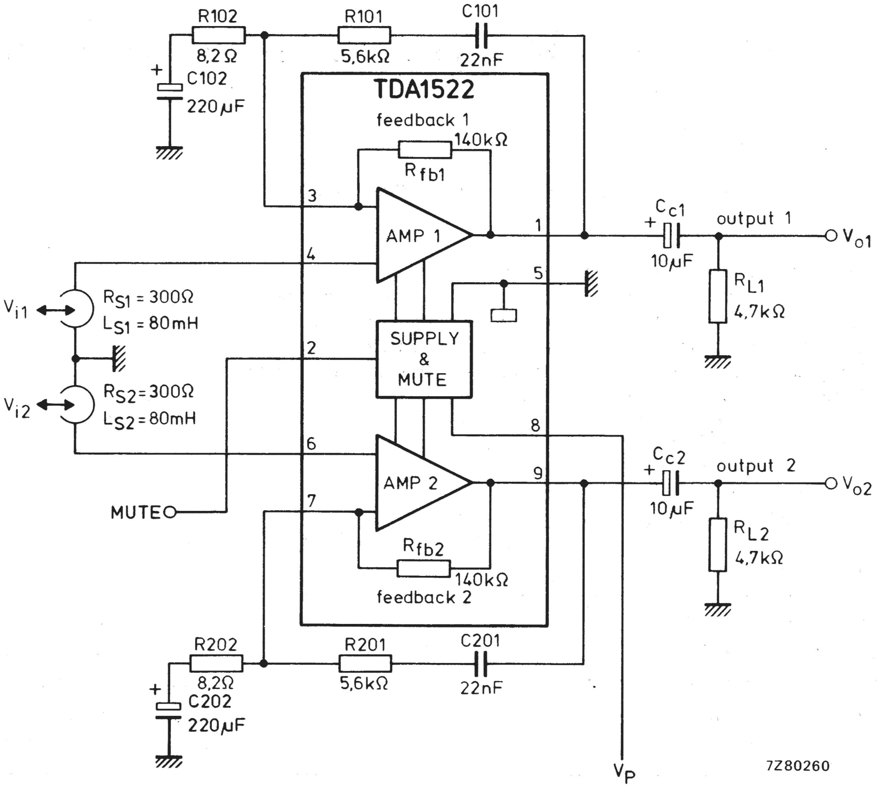
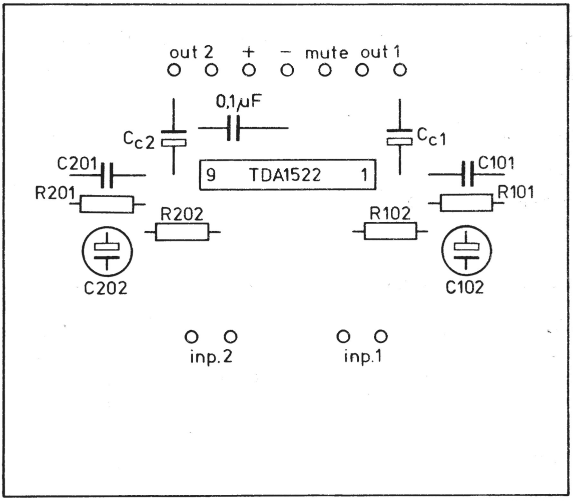

R102
8,2 Ω
C102
220 μF
R101
5,6kΩ
C101
22nF
TDA1522
feedback 1
140kΩ
Rfb1
3
AMP 1
1
4
5
Cc1
10μF
output 1
Vo1
RL1
4,7kΩ
Vi1
RS1 = 300Ω
LS1 = 80mH
Vi2
RS2 = 300Ω
LS2 = 80mH
2
SUPPLY
&
MUTE
8
6
AMP 2
9
Cc2
10μF
output 2
Vo2
RL2
4,7kΩ
MUTE
7
Rfb2
140kΩ
feedback 2
R202
8,2Ω
C202
220μF
R201
5,6kΩ
C201
22nF
VP
7Z80260

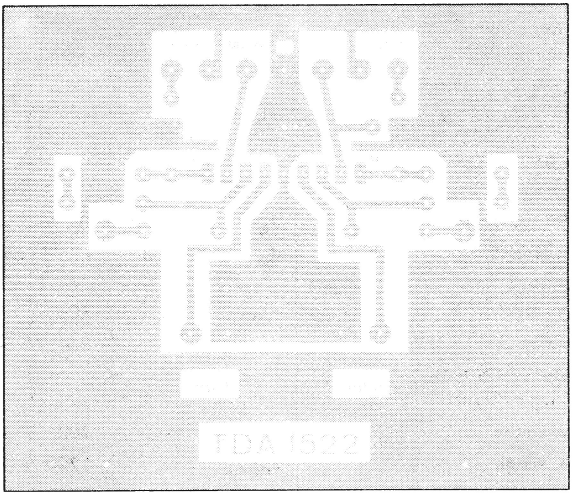
Fig. 1 Block diagram with external components; also used as test circuit.


out 2
+
−
mute
out 1
0,1 μF
Cc2
Cc1
C201
C101
R201
R101
9
TDA1522
1
R202
R102
C202
C102
inp.2
inp.1

7Z80266

Fig. 2 Printed-circuit board component side, showing component layout for circuit of Figure 1.

DEVELOPMENT SAMPLE DATA



7Z80265

Fig. 3 Printed-circuit board, showing track side. Dimensions 75 mm x 65 mm.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_P	7,5 to 23	V
Power dissipation	P_{tot}	max. 800	mW
Feedback current (pins 3 and 7)	I_{fb}	max. 10	mA
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range	T_{amb}	−30 to +85	°C

Note

All pins except 3 and 7 (feedback) can be connected to V_P (pin 8) or ground, (pin 5).

CHARACTERISTICS

V_P = 8,5 V; T_{amb} = 25 °C; test circuit Fig. 1 unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 8)					
Supply voltage range	V_P	7,5	–	23	V
Supply current	I_P	–	5	–	mA
Inputs (pin 4 or 6)					
Noise input voltage (unweighted; r.m.s. value) at f = 20 Hz to 20 kHz*	$V_{n(rms)}$	–	1,6	–	μV
Noise input voltage at R_S = 0; f = 1 kHz*, **	V_n	–	5	–	nV/$\sqrt{Hz}$
Noise input current at f = 1 kHz*, ▲	I_n	–	1,2	–	pA/$\sqrt{Hz}$
D.C. input current at pins 4 and 6	$-I_4; -I_6$	–	–	2	μA
Outputs (pin 1 or 9)					
Output voltage at V_i = 0,3 mV; f = 315 Hz	V_o	–	0,72	–	V
at THD= 1%; f = 1 kHz	V_o	1,0	–	–	V
Output source current at $V_{2\text{-}5} \geqslant$ 7,5 V; mute OFF	$-I_o$	5	10	–	mA
D.C. output voltage	V_o	–	3,7	–	V
Noise output voltage (weighted) at R_S = 300 Ω; L_S = 80 mH					
as DIN A (r.m.s. value)	$V_{n(rms)}$	–	700	–	μV
as CCITT (peak value)	$V_{n(m)}$	–	1200	–	μV
as CCIR (peak value)	$V_{n(m)}$	–	1600	–	μV
Noise output voltage (unweighted) at R_S = 300 Ω; L_S = 80 mH					
as DIN 45405 (peak value)	$V_{n(m)}$	–	1800	–	μV

* Measured in Fig. 4. ** See also Fig. 6. ▲ See also Fig. 7.

parameter	symbol	min.	typ.	max.	unit
Mute on/off characteristics (pin 2)*					
Mute ON voltage at mute switch closed	V_m	0	–	1	V
Mute ON current at mute switch closed or $V_{2\text{-}5} = 0$ V	I_m	–	2,7	–	μA
Mute OFF voltage at mute switch open	V_m	7,5	–	V_P	V
Impedance					
Input impedance** at f = 1 kHz	$\|Z_i\|$	200	–	–	kΩ
Output impedance** at f = 1 kHz	$\|Z_o\|$	–	–	1	kΩ
General					
Internal feedback resistor**	R_{fb}	100	140	180	kΩ
Open-loop voltage gain** at f = 315 Hz	G_v	–	90	–	dB
Channel separation at $R_S = 10$ kΩ; $L_S = 0$; (note 1)	α	45	–	–	dB
Power supply ripple rejection at $V_{P(rms)} = 0{,}1$ V; f = 100 Hz (note 2)	RR	90	95	–	dB
Total harmonic distortion at f = 1 kHz; $V_o = 0{,}72$ V (note 3)	THD	–	0,05	–	%

DEVELOPMENT SAMPLE DATA

Notes

1. Frequency range 300 Hz to 20 kHz.
2. Referred to the input.
3. Measured selective.

---

* See also Fig. 5.

** Applies to each amplifier.

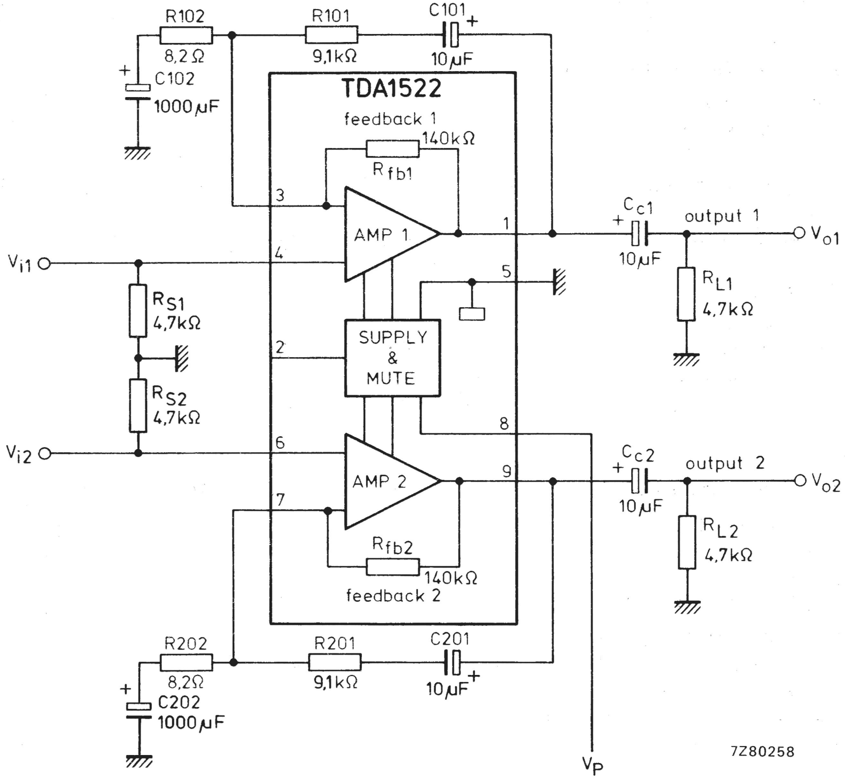

R102
8,2 Ω
R101
9,1kΩ
C101
10 μF
C102
1000 μF
TDA1522
feedback 1
140kΩ
R_{fb1}
3
AMP 1
1
C_{c1}
10μF
output 1
V_{o1}
V_{i1}
4
5
R_{L1}
4,7kΩ
R_{S1}
4,7kΩ
2
SUPPLY & MUTE
R_{S2}
4,7kΩ
8
V_{i2}
6
AMP 2
9
C_{c2}
10μF
output 2
V_{o2}
7
R_{L2}
4,7kΩ
R_{fb2}
140kΩ
feedback 2
R202
8,2Ω
R201
9,1kΩ
C201
10 μF
C202
1000 μF
V_P
7Z80258

Fig. 4 Test circuit for noise measurement.

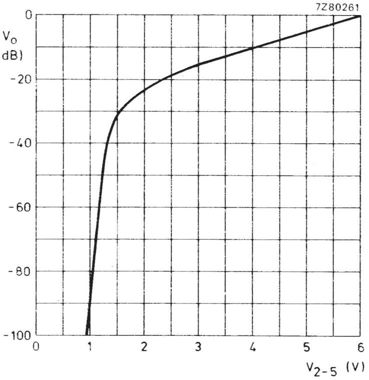


Fig. 5 Muting depth as a function of control voltage at pin 2.

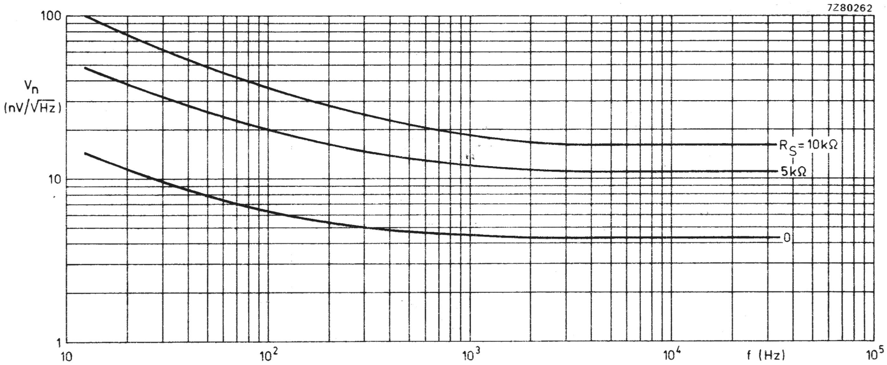


Fig. 6 Noise input voltage as a function of frequency.

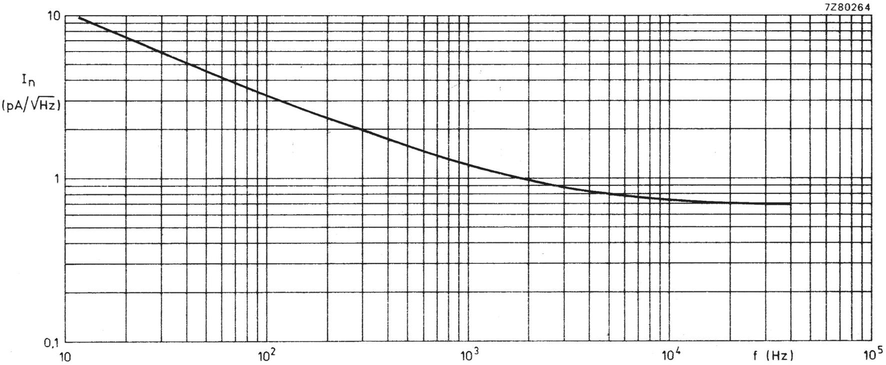


Fig. 7 Noise input current as a function of frequency.

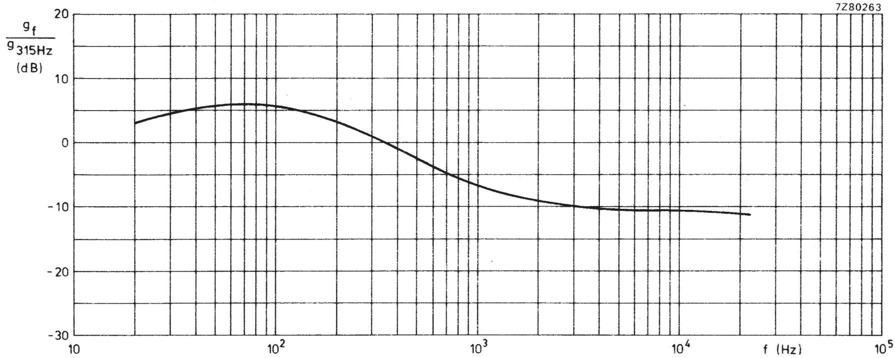


Fig. 8 Frequency response curve for the circuit in Figure 1.

DEVELOPMENT SAMPLE DATA

APPLICATION INFORMATION

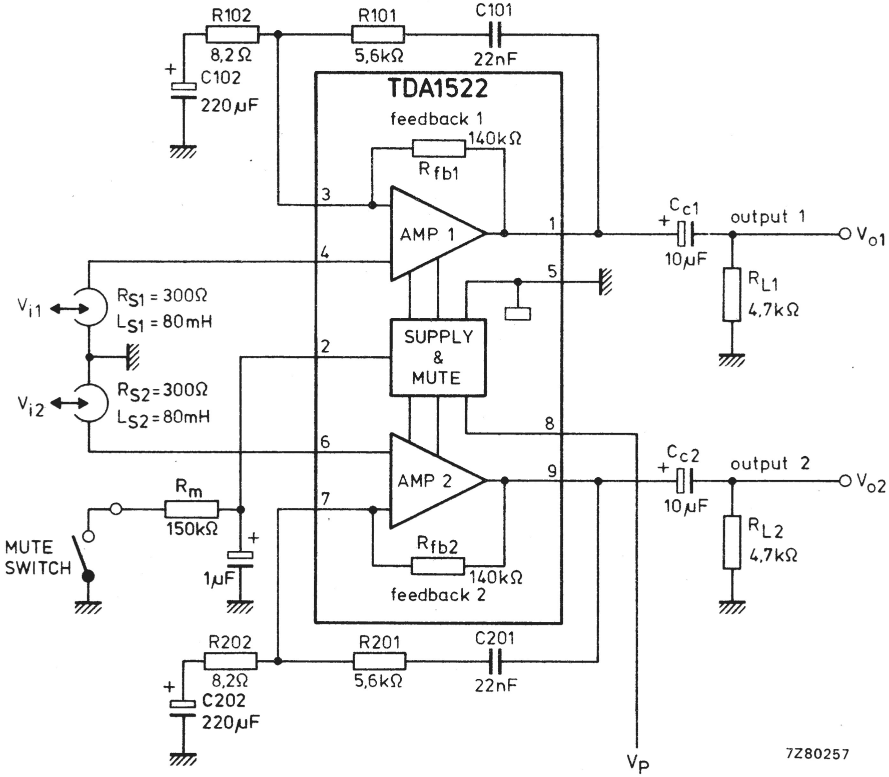

R102
8,2 Ω
R101
5,6kΩ
C101
22nF
C102
220 µF
TDA1522
feedback 1
140kΩ
Rfb1
3
AMP 1
1
output 1
Cc1
10µF
Vo1
4
5
RL1
4,7kΩ
Vi1
RS1 = 300Ω
LS1 = 80mH
2
SUPPLY
&
MUTE
Vi2
RS2 = 300Ω
LS2 = 80mH
8
6
AMP 2
9
output 2
Cc2
10µF
Vo2
Rm
150kΩ
7
RL2
4,7kΩ
MUTE
SWITCH
1µF
Rfb2
140kΩ
feedback 2
R202
8,2Ω
R201
5,6kΩ
C201
22nF
C202
220µF
VP
7Z80257

Fig. 9 Simple mute application.

DEVELOPMENT SAMPLE DATA

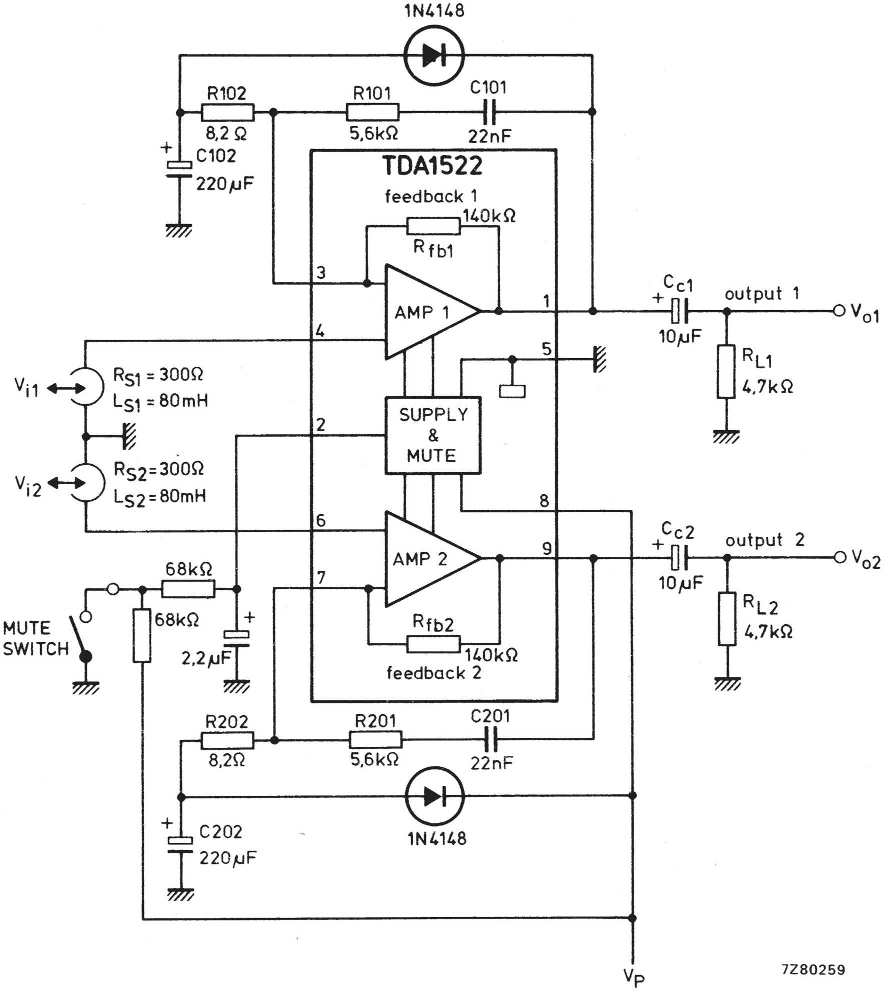

1N4148
R102
8,2 Ω
R101
5,6kΩ
C101
22nF
C102
220μF
TDA1522
feedback 1
140kΩ
R_{fb1}
3
AMP 1
1
C_{c1}
output 1
V_{o1}
10μF
4
5
R_{L1}
4,7kΩ
V_{i1}
R_{S1} = 300Ω
L_{S1} = 80mH
2
SUPPLY & MUTE
V_{i2}
R_{S2} = 300Ω
L_{S2} = 80mH
8
6
AMP 2
9
C_{c2}
output 2
V_{o2}
10μF
68kΩ
7
R_{L2}
4,7kΩ
MUTE SWITCH
68kΩ
2,2μF
R_{fb2}
140kΩ
feedback 2
R202
8,2Ω
R201
5,6kΩ
C201
22nF
1N4148
C202
220μF
V_P
7Z80259

Fig. 10 Application for plop-free muting.

STEREO-TONE VOLUME CONTROL CIRCUIT

GENERAL DESCRIPTION

The TDA1524 is a monolithic integrated circuit designed as an active stereo-tone volume control for car radios, TV receivers and mains-fed equipment. It includes functions for bass and treble control, volume control with built-in contour (can be switched off) and balance. All these functions can be controlled by d.c. voltages or by single linear potentiometers.

Features

- Few external components necessary
- Low noise due to internal gain
- Base emphasis can be increased by an additional filter
- Wide power supply voltage range

QUICK REFERENCE DATA

Supply voltage (pin 3)	$V_P = V_{3\text{-}18}$	typ.	12	V
Supply current (pin 3)	$I_P = I_3$	typ.	35	mA
Maximum input signal with d.c. feedback (r.m.s. value)	$V_{i(rms)}$	typ.	3	V
Maximum output signal with d.c. feedback (r.m.s. value)	$V_{o(rms)}$	typ.	3	V
Volume control range	G_v		−80 to +21,5	dB
Bass control range at 40 Hz	ΔG_v	typ.	± 15	dB
Treble control range at 16 kHz	ΔG_v	typ.	± 15	dB
Total harmonic distortion	THD	max.	0,5	%
Output noise voltage (r.m.s. value)	$V_{no(rms)}$	max.	100	μV
Cross-talk attenuation at G_v = −20 to +21,5 dB	α_{ct}	typ.	60	dB
Tracking between channels at G_v = −20 to +21,5 dB	ΔG_v	max.	2,5	dB
Ripple rejection at 100 Hz	α_{100}	typ.	50	dB
Supply voltage range (pin 3)	$V_P = V_{3\text{-}18}$		7,5 to 16,5	V
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

A COMPLETE DATA SHEET IS AVAILABLE UPON REQUEST

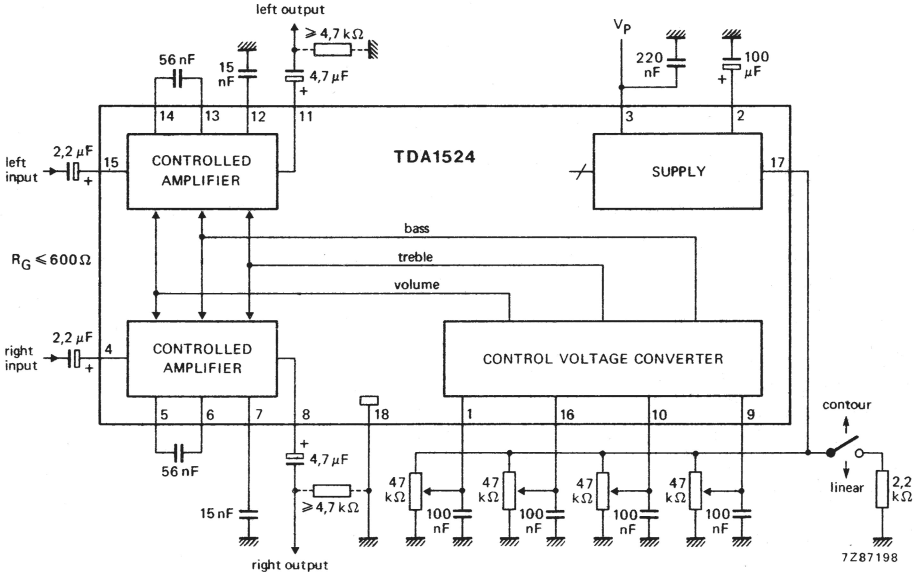

left output
⩾ 4,7 kΩ
4,7 μF
56 nF
15 nF
14
13
12
11
VP
220 nF
100 μF
3
2
left input
2,2 μF
15
CONTROLLED AMPLIFIER
TDA1524
SUPPLY
17
bass
treble
volume
RG ⩽ 600 Ω
right input
2,2 μF
4
CONTROLLED AMPLIFIER
CONTROL VOLTAGE CONVERTER
5
6
7
8
18
1
16
10
9
contour
linear
56 nF
4,7 μF
⩾ 4,7 kΩ
15 nF
47 kΩ
100 nF
2,2 kΩ
right output
7Z87198

Fig. 1 Block diagram and application circuit.

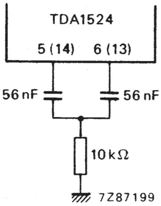

TDA1524
5 (14)
6 (13)
56 nF
56 nF
10 kΩ
7Z87199

Fig. 2 Double-pole low-pass filter for improved bass-boost.

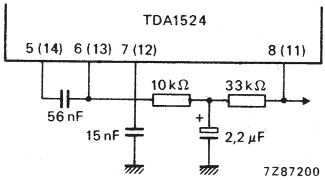

TDA1524
5 (14)
6 (13)
7 (12)
8 (11)
10 kΩ
33 kΩ
56 nF
15 nF
2,2 μF
7Z87200

Fig. 3 D.C. feedback with filter network for improved signal handling.

This information is derived from development samples
made available for evaluation. It does not necessarily
imply that the device will go into regular production.

SIGNAL-SOURCES SWITCH

The TDA1527 is a dual operational amplifier connected as an impedance converter. It incorporates the following features:

- two switchable stereo inputs, with a max. signal handling of 10 V (r.m.s.)
- input protection circuit
- input currents are independent of the switch position
- short-circuit protected outputs

QUICK REFERENCE DATA

Supply voltage range (pin 2)	V_P		4 to 20	V
Operating ambient temperature range	T_{amb}		–30 to + 80	°C
f = 20 Hz to 20 kHz; R_S = 47 kΩ				
Supply voltage (pin 2)	$V_P = V_{2\text{-}8}$	typ.	20	V
Supply current (unloaded)	I_P	typ.	8	mA
Input voltage range at $V_i = V_o$	V_i		1 to V_P–1	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Channel separation (R/L)	α	typ.	74	dB
Crosstalk attenuation between the output and the non-selected input	$\alpha_{I\text{-}II}$	typ.	100	dB
Noise output voltage (unweighted; r.m.s. value)	$V_{n(rms)}$	typ.	6	μV

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142).

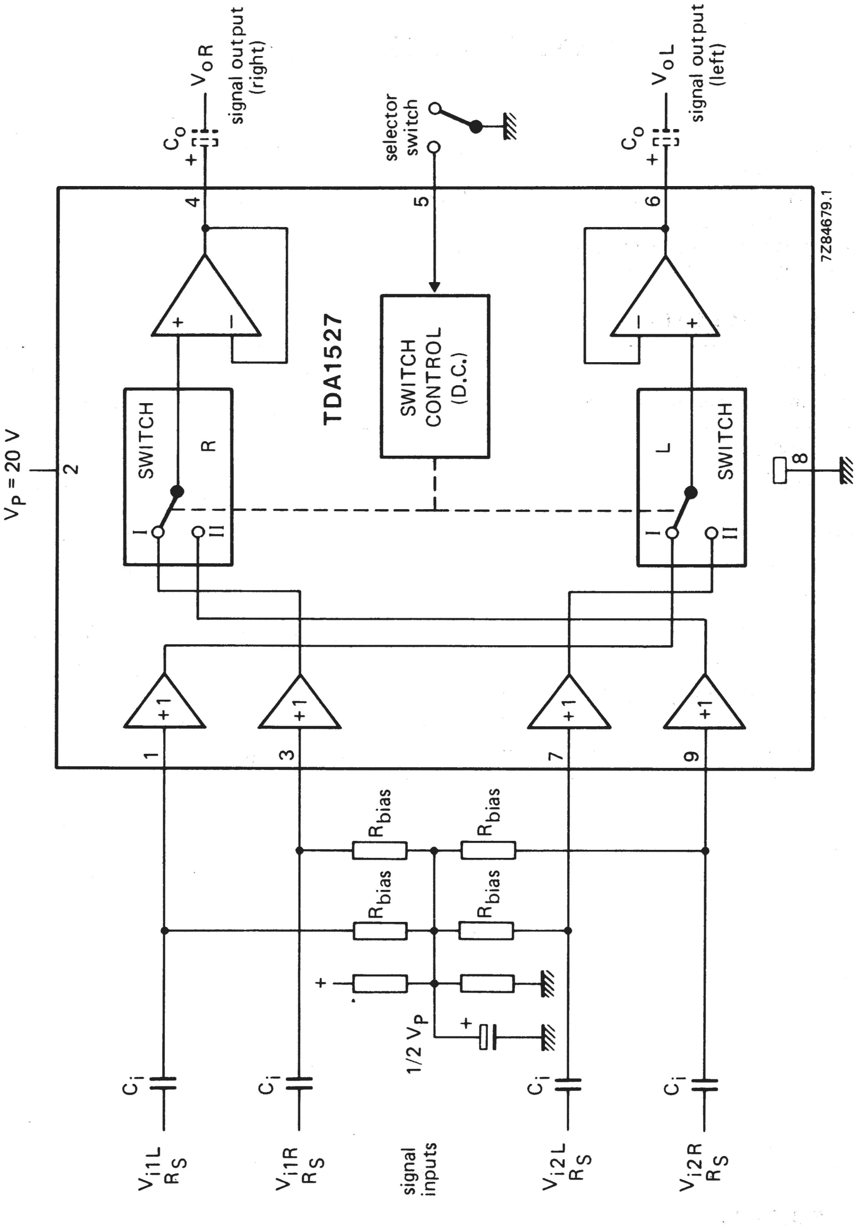

TDA1527
V_P = 20 V
2
SWITCH
R
I
II
SWITCH
L
I
II
SWITCH CONTROL (D.C.)
selector switch
5
4
6
8
C_o
+
V_oR
signal output (right)
C_o
+
V_oL
signal output (left)
+
−
+1
1
3
7
9
R_{bias}
R_{bias}
R_{bias}
R_{bias}
+
1/2 V_P
C_i
C_i
C_i
C_i
V_{i1L}
R_S
V_{i1R}
R_S
signal inputs
V_{i2L}
R_S
V_{i2R}
R_S
7Z84679.1

Fig. 1 Block diagram/test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 2)	$V_P = V_{2\text{-}8}$	max.	23	V
Signal input voltage range (pins 1, 3, 7, 9)	V_I		0 to V_P	V
Input current (pins 1, 3, 7, 9)	$\pm I_I$	max.	10	mA
Input control voltage range (pin 5)	$V_{5\text{-}8}$		−0,5 to + 23	V
Input control current (pin 5)	$-I_5$	max.	10	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−55 to + 80	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

CHARACTERISTICS AND APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; test circuit Fig. 1; unless otherwise specified

Supply voltage range (pin 2)	$V_P = V_{2\text{-}8}$		4 to 20	V
Supply current (unloaded)	$I_P = I_2$	typ.	8	mA
Input voltage range at $V_i = V_o$	V_i		1 to V_P−1	V
Offset voltage at switched-on condition; ± $(V_o - V_i)$	V_{io}	$\leqslant$	20	mV
Offset voltage change at switching from one channel to the other	ΔV_{io}	<	10	mV
Input bias current	I_i	typ.	0,3	µA
Input resistance	R_i	>	10	MΩ
Output current capability				
sink current at V_I = 18 V (current consumption at the outputs)	I_o	>	1,5	mA
		typ.	2,0	mA
source current (available current from the outputs)	$-I_o$	>	5	mA
		typ.	10	mA
Output short-circuit current	$-I_{o(sc)}$	typ.	15	mA
Output resistance	R_o	typ.	10	Ω
Permissible load capacitance	C_L	<	50	pF
Voltage gain of a switched-on amplifier	G_v	typ.	1	
Current gain of a switched-on amplifier	G_i	typ.	120	dB
Crosstalk attenuation between the output and the non-selected input, within the input voltage range; f = 1 kHz	$\alpha_{I\text{-}II}$	typ.	100	dB
Equivalent input noise voltage (r.m.s. value) f = 20 Hz to 20 kHz	$V_{n(rms)}$	typ.	2,5	µV

Switch control (pin 5)

Input switching voltage	$V_{5\text{-}8}$	typ.	2,7	V
Input control current $V_{5\text{-}8}$ = 0 V; pins 7 and 9 in switched-on condition	$-I_5$	typ.	10	µA
		<	40	µA
Input leakage current; $V_{5\text{-}8}$ = 36 V	I_5	<	2	µA

PLL MOTOR SPEED CONTROL CIRCUIT FOR HI-FI APPLICATIONS

The TDA1533 is a monolithic integrated circuit intended for PLL motor speed control in several hi-fi applications; e.g. record players, cassette recorders, reel-to-reel, and operates in accordance with the phase-locked-loop (PLL) system.
The circuit incorporates the following functions:

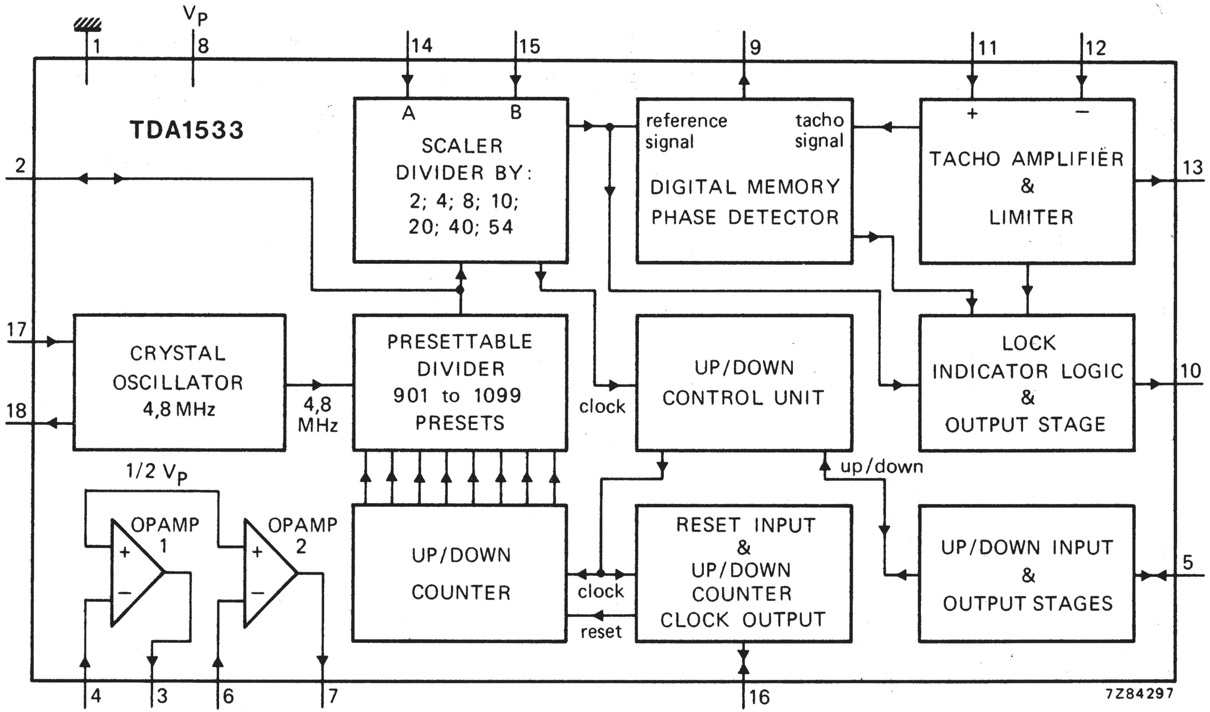
- A quartz reference oscillator
- A synthesizer for adjustment of the phase detector reference frequency
- A programmable scaler for the several applications
- A digital memory phase detector
- A tacho-signal amplifier/limiter
- Two operational amplifiers for the external integration and loop filtering of the phase detector output.

QUICK REFERENCE DATA

Supply voltage range	V_P		9 to 11	V
Supply current	I_P	typ.	50	mA
Crystal oscillator				
Frequency	f	$<$	5	MHz
Temperature coefficient	TC	$<$	$0,1.10^{-6}$	K^{-1}
Tacho input				
Input voltage	V_I		−0,3 to + 10	V
Input sensitivity (peak-to-peak value)	$V_{i(p-p)}$	$>$	10	mV
Operational amplifiers				
Voltage gain	G_v	typ.	10 000	
Input bias current	I_{bias}	$<$	100	nA
Input offset voltage	V_{io}	$<$	15	mV
Temperatures				
Storage temperature	T_{stg}		−25 to + 125	°C
Operating ambient temperature	T_{amb}		0 to + 60	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102C).


TDA1533
1
VP 8
14
15
9
11
12
A
B
SCALER
DIVIDER BY:
2; 4; 8; 10;
20; 40; 54
reference signal
tacho signal
DIGITAL MEMORY
PHASE DETECTOR
+
−
TACHO AMPLIFIER
&
LIMITER
13
2
17
18
CRYSTAL
OSCILLATOR
4,8 MHz
4,8 MHz
PRESETTABLE
DIVIDER
901 to 1099
PRESETS
clock
UP/DOWN
CONTROL UNIT
LOCK
INDICATOR LOGIC
&
OUTPUT STAGE
10
up/down
1/2 VP
OPAMP 1
OPAMP 2
UP/DOWN
COUNTER
clock
reset
RESET INPUT
&
UP/DOWN
COUNTER
CLOCK OUTPUT
UP/DOWN INPUT
&
OUTPUT STAGES
5
4
3
6
7
16
7Z84297

PINNING

1. Ground
2. Test input/output
3. Output of opamp 1
4. Input of opamp 1
5. Up/down input/output
6. Input of opamp 2
7. Output of opamp 2
8. Positive supply (+ 10 V)
9. Phase detector output
10. Lock indicator output
11. + input tacho limiter
12. − input tacho limiter
13. Output tacho limiter
14. A-input scaler control
15. B-input scaler control
16. Reset input/output
17. Crystal oscillator input
18. Crystal oscillator output

Fig. 1 Block diagram.

GENERAL DESCRIPTION (see also Fig. 1)

The crystal frequency (e.g. 4,8 MHz) is divided by the presettable 901 to 1099 divider. The scaler is used to obtain the reference signal for the digital memory phase detector. The tacho signal is derived from the tacho amplifier/limiter.
The output of the phase detector becomes HIGH on the positive-going edge of the reference signal, and it is floating on the first-coming positive edge of the tacho signal, if the angle between the edges is not more than 360°. The output becomes LOW if the first positive-going edge is the edge of the tacho signal, and it is floating on the first-coming positive edge of the reference signal. This means that the holding range is 720°.
The lock indication output is HIGH, except for the period between the two positive and the two negative-going edges of the tacho and reference signals.
The dividing number of the presettable divider depends on the state of its presets, thus on the position of the up/down counter.
A pull-up to the IC supply voltage of the reset input results into a reset of the up/down counter and dividing by 1000.
The up/down counter can be changed in position by means of the up/down input and the up/down control unit, and therefore the divisors of the presettable divider in a range from 901 to 1099.
The clock of the up/down counter is available at the reset input as a 0,1 V_P to 0,8 V_P pulse.
The timing diagram of the up/down counter is given in Fig. 2.
The up/down input and the scaler control inputs are 3-state inputs. The scaler truth table is given below.
A HIGH level at the up/down input gives an increase, a LOW level a decrease, of the phase detector reference signal frequency.
The information at the up/down input will be internally forced on the state present, over a period of 250 ms. Together with the up/down clock at the reset pin, this offers the possibility of displaying the number of clock pulses used.

SCALER TRUTH TABLE

control inputs A	control inputs B	division ratio
H	H	note 1
H	L	note 2
F	F	4
F	H	8
F	L	2
H	F	54
L	H	10
L	L	20
L	F	40

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
F = floating (pin open)

Notes

1. Test 1; general preset.
2. Test 2; fast clock via test pin (pin 2).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{8\text{-}1}$	max.	12	V
Total power dissipation	P_{tot}	max.	1	W
Storage temperature	T_{stg}		−25 to + 125	°C
Operating ambient temperature	T_{amb}		−20 to + 80	°C

CHARACTERISTICS

Supply voltage	V_P	typ.	10	V
			9 to 11	V
Supply current	I_P	typ.	50	mA
Operating ambient temperature	T_{amb}		0 to 60	°C

The following characteristics are measured at $V_P = 10$ V; $T_{amb} = 25$ °C; unless otherwise specified

Crystal oscillator

Frequency	f	typ.	4,8	MHz
		<	5,0	MHz
Input voltage HIGH	V_{IH}		2,6 to 10	V
Input voltage LOW	V_{IL}		−2,0 to + 2,0	V
Input resistance	R_i	>	50	kΩ
Input capacitance	C_i	<	5	pF
Open voltage 1	V_{o1}	typ.	2	V
Open voltage 2	V_{o2}	typ.	1,3	V
Temperature coefficient	TC	<	$0{,}1.10^{-6}$	K^{-1}

Lock indicator output (open collector)

Output voltage HIGH	V_{OH}	<	12	V
Output voltage LOW at 10 mA	V_{OL}	typ.	0,25	V
		<	0,5	V
Output sink current	I_o	typ.	10	mA
		<	20	mA

Phase detector output

Output voltage HIGH at 20 μA	V_{OH}	>	9,5	V
		typ.	9,7	V
Output voltage LOW at 20 μA	V_{OL}	typ.	0,3	V
		<	0,5	V
Output current				
source	I_o	>	30	μA
		typ.	44	μA
sink	I_o	>	30	μA
		typ.	44	μA

Tacho input

Input voltage	V_I		–0,3 to + 10	V
Input biasing current	I_{bias}	typ.	0,5	µA
		<	5,0	µA
Input sensitivity (peak-to-peak value)	$V_{i(p-p)}$	>	10	mV
Offset voltage over temperature range	V_{io}	typ.	0,1	mV
		<	2,0	mV
Offset current over temperature range	I_{io}	typ.	50	nA
		<	250	nA

Tacho output (open collector)

Output voltage HIGH	V_{OH}	<	12	V
Output voltage LOW at 5 mA	V_{OL}	<	0,5	V
Output sink current	I_o	<	10	mA

Up/down - input/output

Input voltage LOW	V_{IL}	typ.	0	V
			–0,4 to + 0,4	V
Output voltage HIGH	V_{OH}		3 to 10	V
Open voltage	V_o	typ.	0,7	V
			0,6 to 0,8	V
Output voltage HIGH at 0,5 mA	V_{OH}	>	8,5	V
		typ.	9,0	V
Output voltage LOW at 5 mA	V_{OL}	<	0,5	V
Output sink current	I_o	<	10	mA
Output source impedance	$\lvert Z_o \rvert$	<	1,5	kΩ

Scaler inputs

Input voltage LOW	V_{IL}	typ.	0	V
			–0,4 to + 0,4	V
Input voltage HIGH	V_{IH}		4 to 10	V
Open voltage	V_o	typ.	0,7	V
			0,6 to 0,8	V

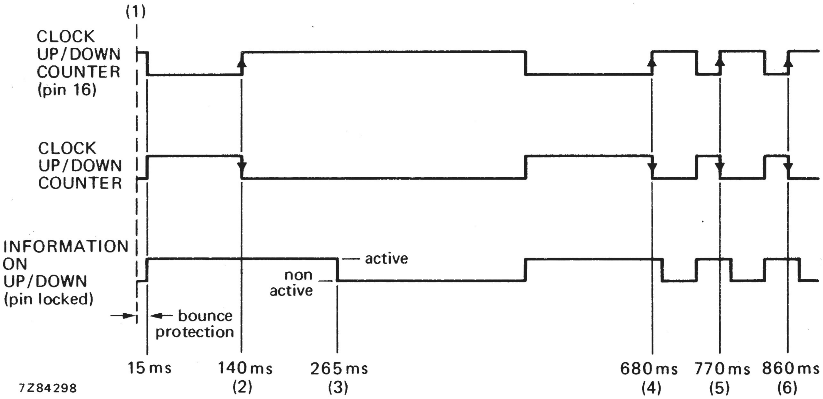
Reset input/output

Input voltage HIGH	V_{IH}	>	9,5	V
		typ.	10,0	V
Output voltage LOW	V_{OL}	typ.	0,3	V
		<	0,5	V
Output voltage HIGH	V_{OH}	typ.	8	V

CHARACTERISTICS (continued)

Operational amplifiers

Voltage gain	G_v	typ.	10 000	
Input bias current	I_{bias}	typ.	30	nA
		<	100	nA
Output sink current at $V_o = 1$ V	I_o	typ.	0,1	mA
Output source current at $V_o = 9$ V	I_o	>	15	mA
		typ.	20	mA
Input offset voltage	V_{io}	<	15	mV
Input offset voltage drift	$\Delta V_{io}/\Delta T$	<	0,25	mV/K
Bandwidth (3 dB)	B		60	Hz


(1)
CLOCK UP/DOWN COUNTER (pin 16)
CLOCK UP/DOWN COUNTER
INFORMATION ON UP/DOWN (pin locked)
active
non active
bounce protection
15 ms
140 ms (2)
265 ms (3)
680 ms (4)
770 ms (5)
860 ms (6)
7Z84298

(1) Start operation of up/down pin.
(2) 1st clock pulse.
(3) From this point on, restart of cycle by second excitation is possible.
(4) 2nd clock pulse.
(5) 3rd clock pulse.
(6) 4th clock pulse.

Fig. 2 Timing diagram of up/down counter.

14-BIT DAC WITH 85 dB S/N RATIO

GENERAL DESCRIPTION

The TDA1540D is a monolithic integrated 14-bit digital to analogue converter (DAC). It incorporates a 14-bit input shift register with output latches, binary weighted current sources with switches and a reference source.

The IC features an improved switch circuitry which eliminates the need for a deglitcher circuit at the output. This results in a signal-to-noise ratio of typical 85 dB in the audio band.

QUICK REFERENCE DATA

Supply voltages				
pin 4	V_{P1}	typ.	5	V
pin 7	V_{N1}	typ.	−5	V
pin 11	V_{N2}	typ.	−17	V
Signal-to-noise ratio (full scale sine-wave) at analogue output (pin 22)	S/N	typ.	85	dB
Non-linearity at T_{amb} = −20 to + 70 °C		typ.	½ LSB	
Current settling time	t_{cs}	typ.	0,5	μs
Maximum input bit rate at data input (pin 1)	BR_{max}	min.	12	Mbit/s
Maximum clock frequency at clock input (pin 28)	$f_{cl\,max}$	min.	12	MHz
Full scale temperature coefficient at analogue output (pin 22)	TC_{FS}	typ.	$\pm 30 \cdot 10^{-6}$	K^{-1}
Operating ambient temperature range	T_{amb}		−20 to + 70	°C
Total power dissipation	P_{tot}	typ.	350	mW

PACKAGE OUTLINE

28-lead DIL; ceramic (cerdip); SOT-135A.

FUNCTIONAL DESCRIPTION

The binary weighted current sources are obtained by a combination of a passive divider and a time division concept. Figure 1a gives the diagram of one divider stage. The total emitter current 4 I of the passive divider is divided into four more or less equal output currents.

The output currents of the passive divider are now interchanged during equal time intervals generated by means of a shift register. The average output currents are exactly equal as a result of this operation. A ripple on the output current, caused by a mismatch of the passive divider, is filtered by an a.c. low-pass filter, requiring an external filter capacitor.

The outputs of the dividers are combined to obtain the output currents I ($\bar{I}_1$), I ($\bar{I}_2$) and 2I ($\bar{I}_3$) (see Fig. 1b). The current of the most significant bit is generated by an on-chip reference source. A binary weighted current network is formed by cascading the current division stages (see Fig. 2).

The interchanging pulses are generated by an on-chip oscillator and a 4-bit shift register. The binary currents are switched to the current output (pin 22) via diode-transistor switching stages; therefore, the voltage on the output pin must be 0 V ± 10 mV. The output current can be converted into a voltage by means of a summing amplifier.

Figure 3 represents the data input format, and an application circuit is given in Fig. 4.

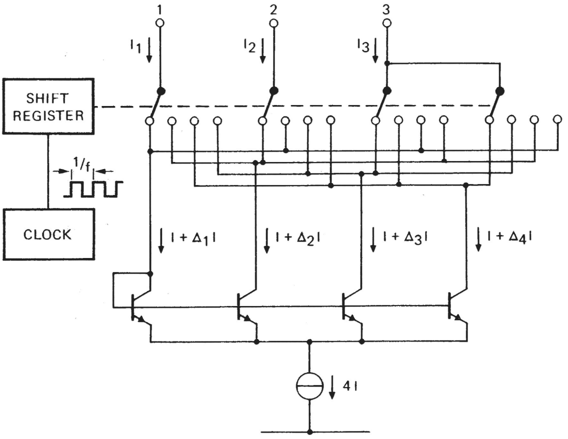


Fig. 1a Circuit diagram of one divider stage.

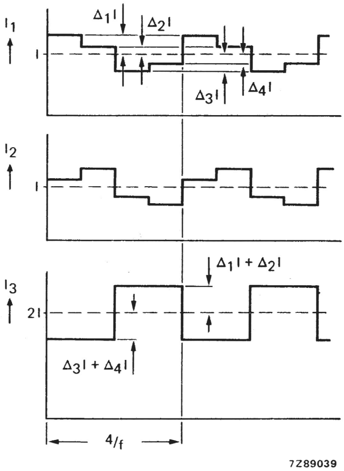


Fig. 1b Waveforms showing output currents I_1, I_2 and I_3 of Fig. 1a.

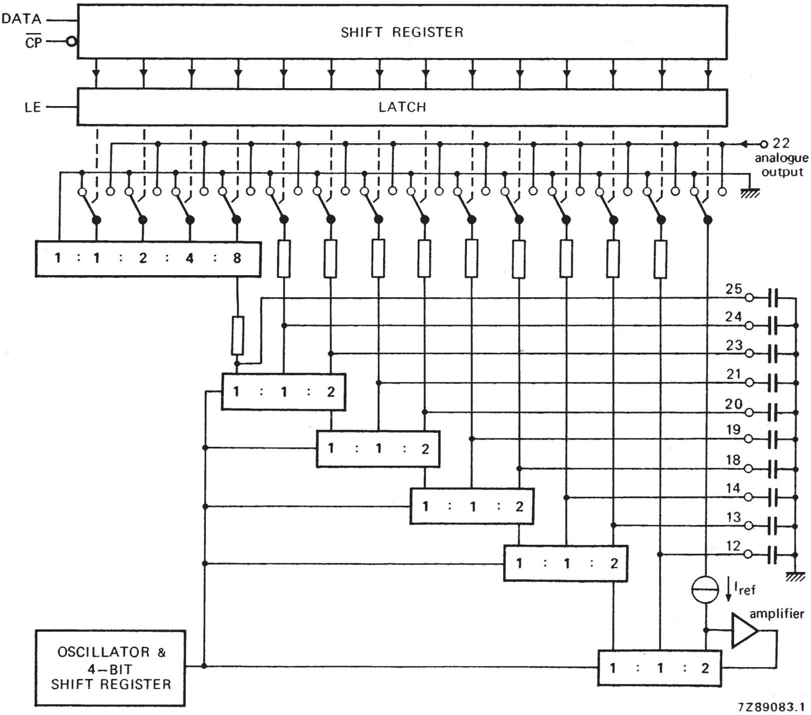

DATA
CP
SHIFT REGISTER
LE
LATCH
22
analogue
output
1 : 1 : 2 : 4 : 8
25
24
23
21
20
19
18
14
13
12
1 : 1 : 2
1 : 1 : 2
1 : 1 : 2
1 : 1 : 2
I ref
amplifier
OSCILLATOR &
4—BIT
SHIFT REGISTER
1 : 1 : 2
7Z89083.1

Fig. 2 Functional diagram showing cascading of current division stages.

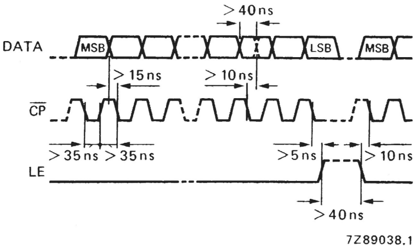

> 40 ns
DATA
MSB
LSB
MSB
> 15 ns
> 10 ns
CP
> 35 ns
> 35 ns
> 5 ns
> 10 ns
LE
> 40 ns
7Z89038.1

Fig. 3 Format of input signals.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages			
with respect to GND (pin 6)			
at pin 4	V_{P1}	max.	12 V
at pin 7	V_{N1}	max.	−12 V
at pin 11	V_{N2}	max.	−20 V
at pin 4 with respect to pin 11	$V_{P1}-V_{N2}$	max.	32 V
at pin 7 with respect to pin 11	$V_{N1}-V_{N2}$		−1 to + 20 V
Total power dissipation	P_{tot}	max.	600 mW
Storage temperature range	T_{stg}		−55 to + 125 °C
Operating ambient temperature range	T_{amb}		−25 to + 80 °C

CHARACTERISTICS (see application circuit Fig. 4)

T_{amb} = 25 °C; at typical supply voltages; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltages					
with respect to GND (pin 6)					
at pin 4	V_{P1}	3	5	7	V
at pin 7	V_{N1}	−4,7	−5	−7	V
at pin 11	V_{N2}	−16,5	−17	−18	V
Supply currents					
at pin 4*	I_{P1}	–	12	14	mA
at pin 7	I_{N1}	–	−20	−24	mA
at pin 11	I_{N2}	–	−11	−13	mA
Power dissipation					
Total power dissipation	P_{tot}	–	350	410	mW
Temperature					
Operating ambient temperature range	T_{amb}	−20	–	+ 70	°C

---

* When the output current is ½I_{FS} (½ full scale output current).

parameter	symbol	min.	typ.	max.	unit
Data input DATA (pin 1)					
Input voltage HIGH	V_{IH}	2,0	–	7,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input current HIGH at V_{IH}	I_{IH}	–	–	50	μA
Input current LOW at V_{IL}	$-I_{IL}$	–	–	0,2	mA
Maximum input bit rate	BR_{max}	12	–	–	Mbits/s
Latch enable input LE (pin 2)					
Clock input $\overline{CP}$ (pin 28)					
Input voltage HIGH	V_{IH}	2,0	–	7,0	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input current HIGH at V_{IH}	I_{IH}	–	–	50	μA
Input current LOW at V_{IL}	$-I_{IL}$	–	–	0,2	mA
Maximum clock frequency	f_{CPmax}	12	–	–	MHz
Oscillator (pins 8 and 9)					
Oscillator frequency at $C_{8\text{-}9}$ = 820 pF	f_{osc}	100	160	200	kHz
Analogue output I_{out} (pin 22)					
Output voltage compliance	V_{OC}	−10	–	+ 10	mV
Full scale current	I_{FS}	3,8	4,0	4,2	mA
Zero scale current	$\pm I_{ZS}$	–	–	100	nA
Full scale temperature coefficient T_{amb} = −20 to + 70 °C	TC_{FS}	–	$\pm 30 \times 10^{-6}$	–	K^{-1}
Settling time to ± ½LSB all bits on or off	t_{cs}	–	0,5	–	μs
Signal-to-noise ratio*	S/N	80	85	–	dB

DEVELOPMENT SAMPLE DATA

---

* Signal-to-noise ratio within 20 Hz and 20 kHz of a 1 kHz full scale sinewave, generated at a sample rate of 44 kHz.

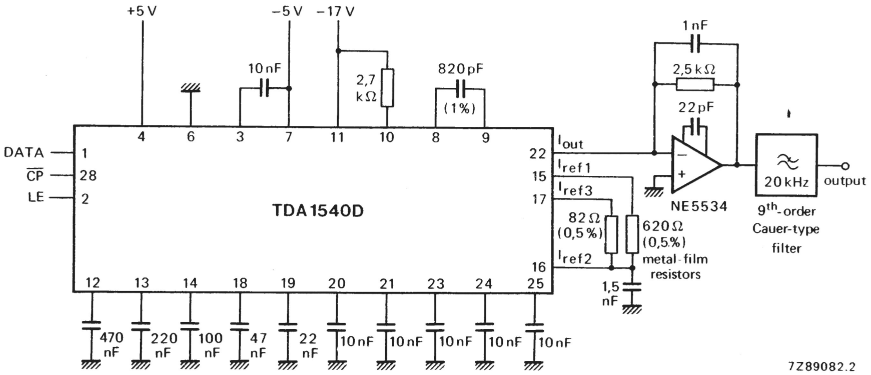

+5 V
−5 V
−17 V
10 nF
2,7 kΩ
820 pF
(1%)
1 nF
2,5 kΩ
22 pF
DATA
$\overline{CP}$
LE
TDA1540D
4
6
3
7
11
10
8
9
1
28
2
22
15
17
16
12
13
14
18
19
20
21
23
24
25
I_{out}
I_{ref1}
I_{ref3}
I_{ref2}
82 Ω (0,5 %)
620 Ω (0,5 %)
metal-film resistors
1,5 nF
NE5534
20 kHz
9th-order Cauer-type filter
output
470 nF
220 nF
100 nF
47 nF
22 nF
10 nF
10 nF
10 nF
10 nF
10 nF
7Z89082.2

Fig. 4 Application circuit.

PINNING

1	DATA	data input
2	LE	latch enable input
3	V_{ref1}	voltage reference
4	V_{P1}	positive supply
5	i.c.*	frequency compensation on-chip operational amplifier
6	GND	ground
7	V_{N1}	negative supply
8	OSC1	oscillator capacitor
9	OSC2	
10	V_{ref2}	voltage reference
11	V_{N2}	negative supply
12	C1	decoupling binary weighted current sources
13	C2	
14	C3	
15	I_{ref1}	current reference sources
16	I_{ref2}	
17	I_{ref3}	
18	C4	decoupling binary weighted current sources
19	C5	
20	C6	
21	C7	
22	I_{out}	analogue output
23	C8	decoupling binary weighted current sources
24	C9	
25	C10	
26	i.c.*	voltage reference
27	i.c.*	voltage reference
28	$\overline{CP}$	clock pulse input

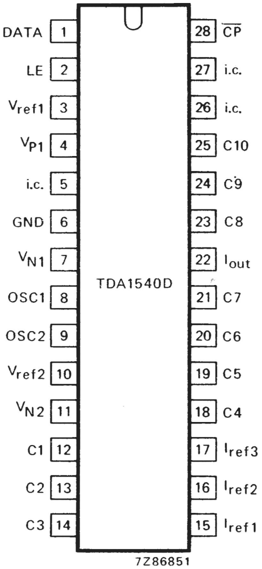

DATA 1
LE 2
V_{ref1} 3
V_{P1} 4
i.c. 5
GND 6
V_{N1} 7
OSC1 8
OSC2 9
V_{ref2} 10
V_{N2} 11
C1 12
C2 13
C3 14
28 $\overline{CP}$
27 i.c.
26 i.c.
25 C10
24 C9
23 C8
22 I_{out}
21 C7
20 C6
19 C5
18 C4
17 I_{ref3}
16 I_{ref2}
15 I_{ref1}
TDA1540D
7Z86851

Fig. 5 Pinning diagram.

---

* i.c.: internally connected.

MOTOR SPEED REGULATOR

The TDA1559 is a 3 pins speed regulator circuit for d.c. motors. It is especially intended for low-voltage motors in battery operated cassette recorder systems and record players. The IC features a high multiplication coefficient (k = 21,5) and a low drop-out voltage (0,5 V). It also contains a current limiter and thermal shut-down.

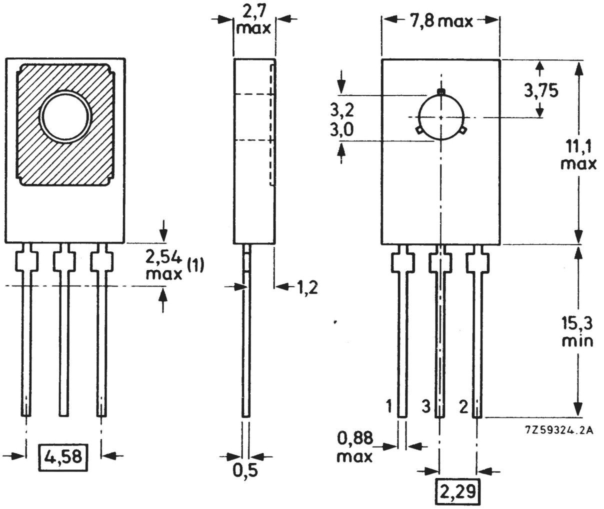
QUICK REFERENCE DATA

Supply voltage	V_P	max.	16	V
Internal reference voltage	V_{ref}	typ.	1,26	V
Drop-out voltage	$V_{2\text{-}3}$	typ.	0,5	V
Limited output current	$I_{2\,lim}$	typ.	0,7	A
Multiplication coefficient	k	typ.	21,5	
Thermal limitation	$T_{j\,lim}$	typ.	145	°C
Operating ambient temperature range	T_{amb}	−25 to	+70	°C

PACKAGE OUTLINE

Dimensions in mm

Fig. 1 TO-126 (SOT-32).
Pin 1 connected to metal part of mounting surface.



(1) Within this region the cross-section of the leads is uncontrolled.

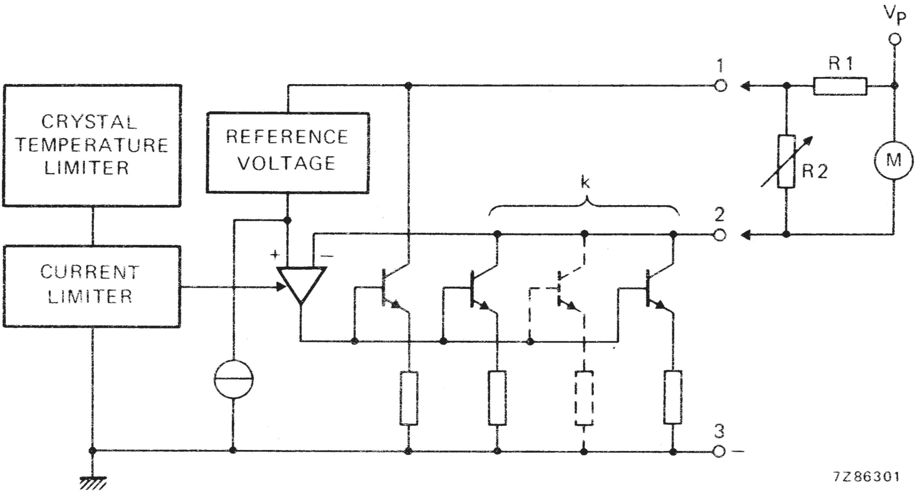

CRYSTAL TEMPERATURE LIMITER
REFERENCE VOLTAGE
CURRENT LIMITER
+
−
k
V_P
R 1
R 2
M
1
2
3
−
7Z86301

Fig. 2 Functional diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{1\text{-}3}$	max.	16	V
Output current	I_2	max.	1,2	A
Storage temperature	T_{stg}		−25 to +125	°C
Junction temperature (limited by thermal limitation)	T_j	max.	130	°C

THERMAL RESISTANCE

From junction to case	$R_{th\ j\text{-}c}$	=	10	K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	100	K/W

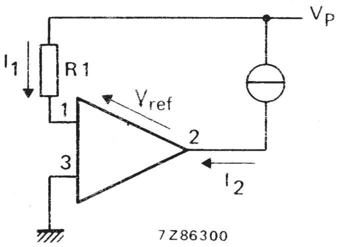

V_P
I_1
R 1
V_{ref}
1
2
3
I_2
7Z86300

Fig. 3 Test circuit.

CHARACTERISTICS

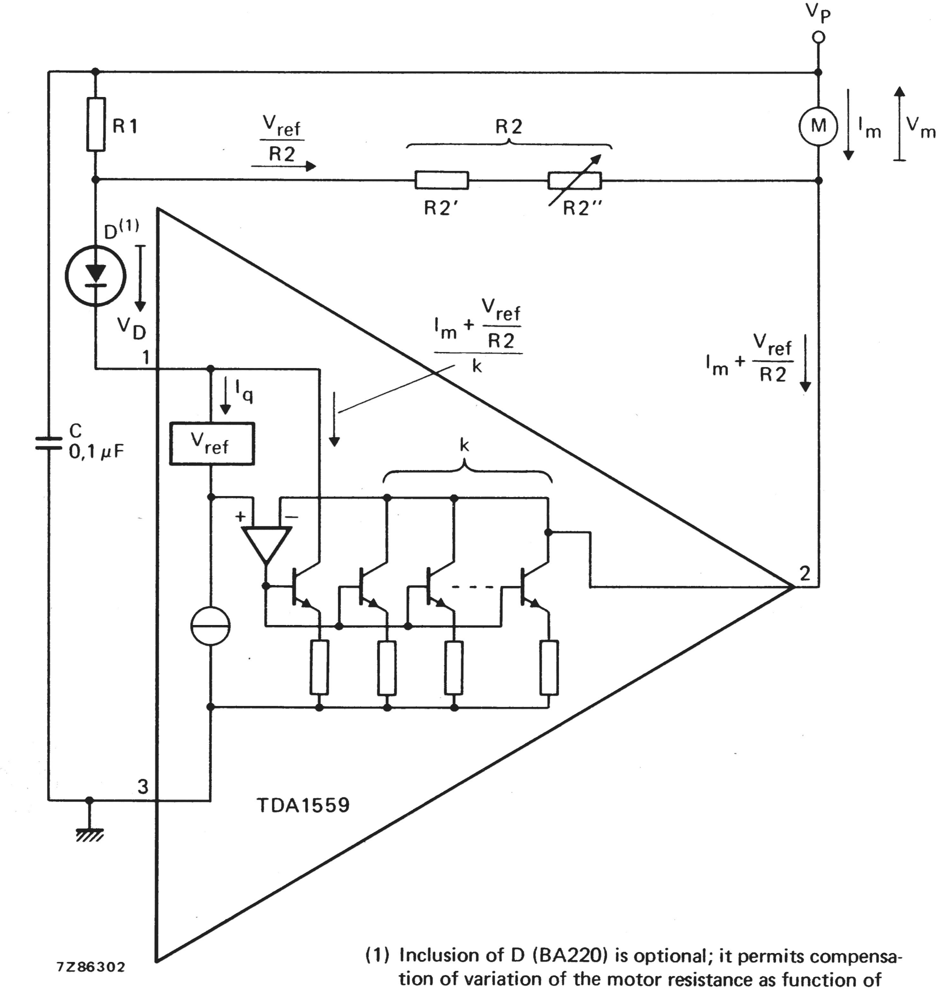
V_P = 9 V; I_2 = 70 mA; T_{amb} = 25 °C; R1 = 0; heatsink with R_{th} = 100 K/W and after thermal stabilization; unless otherwise specified; see test circuit Fig. 3.

	symbol	min.	typ.	max.	unit	conditions
Internal reference voltage	$V_{ref} = V_{1\text{-}2}$	1,20	1,26	1,32	V	V_P = 2,1 V
Drop-out voltage	$V_{2\text{-}3}$	–	0,5	0,7	V	
Quiescent current	I_q	0,8	1,3	1,8	mA	
Limiting output current	$I_{2\,lim}$	0,4	0,7	–	A	
Multiplication coefficient*	$k = \frac{\Delta I_2}{\Delta I_1}$	19,3	21,5	24,3		$\Delta I_2 = \pm 10$ mA
Thermal limitation	$T_{j\,lim}$	130	–	160	°C	V_{ref} = 1,2 V
Line regulation variation						
V_{ref} versus V_P	$\frac{\Delta V_{ref}}{\Delta V_P}$	0 0	0,9 0,07	2,0 0,16	mV/V %/V	V_P = 2,1 to 15 V
k-spread versus V_P	$\frac{\Delta k}{\Delta V_P}$	–0,3	+0,2	+1	%/V	$\Delta I_2 = \pm 10$ mA V_P = 2,1 to 15 V
I_q versus V_P	$\frac{\Delta I_q}{\Delta V_P}$	– –	11 0,95	– –	μA/V %/V	$I_2 = 0$ V_P = 2,1 to 15 V
Load regulation variation						
V_{ref} versus I_2	$\frac{\Delta V_{ref}}{\Delta I_2}$	–0,4 –0,03	0 0	+0,4 +0,03	V/A %/mA	I_2 = 50 to 100 mA
k-spread versus I_2	$\frac{\Delta k}{\Delta I_2}$	–0,05	0	+0,05	%/mA	I_2 = 50 to 100 mA $\Delta I_2 = \pm 10$ mA
Temperature coefficient variation						
V_{ref} versus T_{amb}	$\frac{\Delta V_{ref}}{\Delta T_{amb}}$	–0,2 –0,02	0,1 0,01	+0,4 +0,04	mV/K %/K	T_{amb} = –5 to +55 °C
k-spread versus T_{amb}	$\frac{\Delta k}{\Delta T_{amb}}$	–0,03	0	+0,03	%/K	T_{amb} = –5 to +55 °C $\Delta I_2 = \pm 10$ mA
I_q versus T_{amb}	$\frac{\Delta I_q}{\Delta T_{amb}}$	– –	–1,1 –0,08	– –	μA/K %/K	T_{amb} = –5 to +55 °C $I_2 = 0$

* There are 4 ranges of k-factors, indicated by either '1', '2', '3', or '4' on the package. Ordering a specific range is not possible.

1 = 19,3 to 20,5
2 = 20,3 to 21,5
3 = 21,3 to 22,7
4 = 22,5 to 24,3

APPLICATION INFORMATION


VP
R1
Vref / R2
R2
R2′
R2″
M
Im
Vm
D(1)
VD
1
Iq
Vref
Im + Vref/R2 / k
Im + Vref/R2
C
0,1 μF
k
+
−
2
3
TDA1559
7Z86302

(1) Inclusion of D (BA220) is optional; it permits compensation of variation of the motor resistance as function of temperature.

Fig. 4 Example of using the TDA1559 in a d.c. motor speed regulation circuit.

Notes to Fig. 4

$R2 = R2' + R2''$

$E_n = n \times C \times \phi$ where: n = speed in revolutions per minute

$I_m = T \times \frac{2\pi}{60} = \frac{1}{C.\phi}$

C = motor constant

ϕ = magnetic flux

E_n = electromotive force (e.m.f.)

T = motor torque

R_m = motor resistance

E_n can be expressed as:

$$E_n = I_m\left(\frac{R1}{k} - R_m\right) + V_{ref}\left\{1 + \frac{R1}{R2}\left(1 + \frac{1}{k}\right)\right\} + R2 \times I_q$$

For optimal regulation (dn/dT = 0), $\left(\frac{R1}{k} - R_m\right)$ should be zero.

However, if $R1 = k \times R_m$, the regulator will be oscillating, so for stability always $R1 < k \times R_m$.

R2 is determined by:

$$R2 = \frac{V_{ref} \times R1 \times \left(1 + \frac{1}{k}\right)}{E_n - (R1 \times I_q) - V_{ref} - I_m\left(\frac{R1}{k} - R_m\right)}$$

Example:

$E_n = E_{2000} = 3{,}58\ V \pm 11{,}6\%$
$R_m = 13\ \Omega \pm 10\%$
$n = 2000$ rev/min
$T = 1$ mNm
$R1 = 220\ \Omega$
$R2' = 82\ \Omega$
$R2'' = 220\ \Omega$

When a diode (D = BA220) is connected is series with pin 1, then the expressions for R2 and E_n are:

$$R2 = \frac{(V_{ref} + V_D) \times R1 \times \left(1 + \frac{1}{k}\right)}{E_n - (R1 \times I_q) - (V_{ref} + V_D) - I_m\left(\frac{R1}{k} - R_m\right)}$$

$$E_n = I_m\left(\frac{R1}{k} - R_m\right) + \left(V_{ref} + V_D\right)\left\{1 + \frac{R1}{R2}\left(1 + \frac{1}{k}\right)\right\} + R2 + I_q$$

Example:

$E_n = E_{2000} = 3{,}58\ V \pm 11{,}6\%$
$R_m = 13\ \Omega \pm 10\%$
$n = 2000$ rev/min
$T = 1$ mNm
$R1 = 220\ \Omega$
$R2' = 160\ \Omega$
$R2'' = 470\ \Omega$
D = BA220

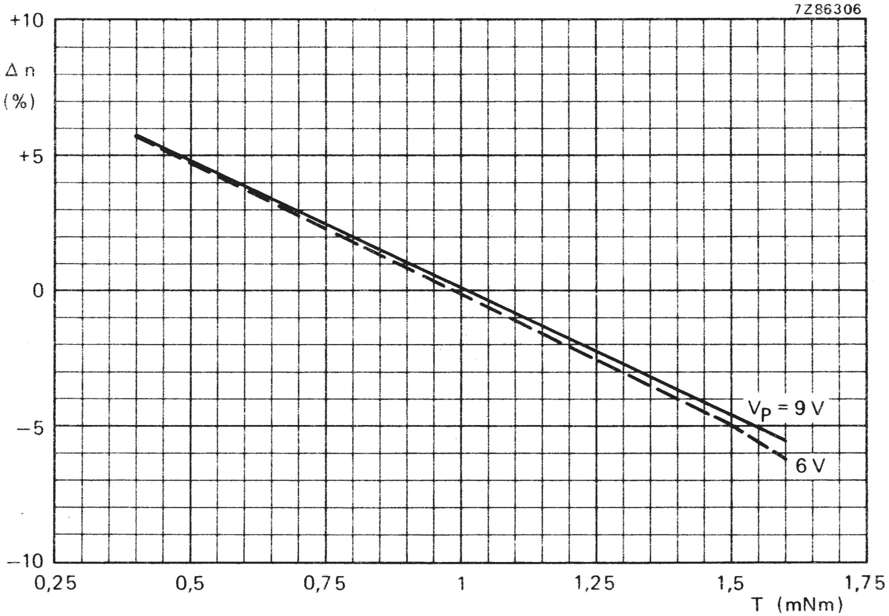


Fig. 5 Variation in motor speed (n is revolutions per minute) as a function of the applied motor torque at T_{amb} = 25 °C.

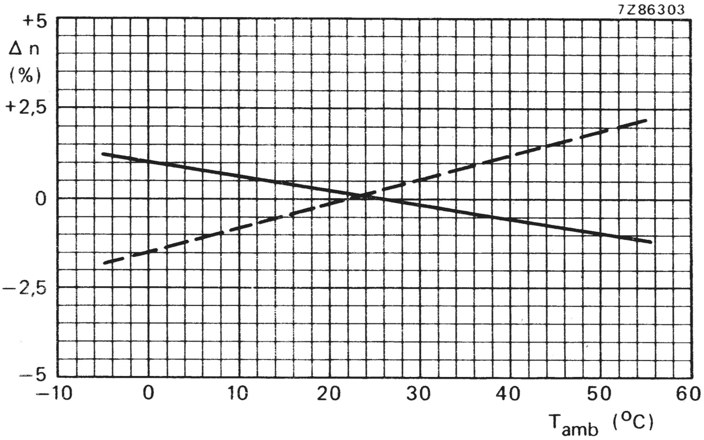


Fig. 6 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature at T = 1 mNm nominal and V_P = 9 V.

————————: with diode (D = BA220; see Fig. 4).

— — — — — —: without diode.

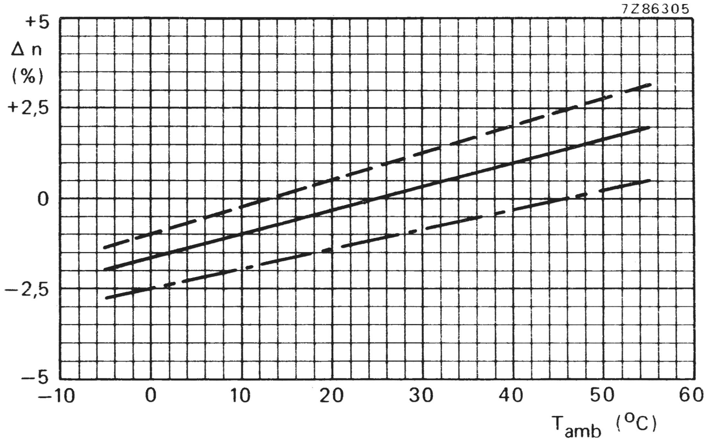


Fig. 7a $V_P = 6$ V.

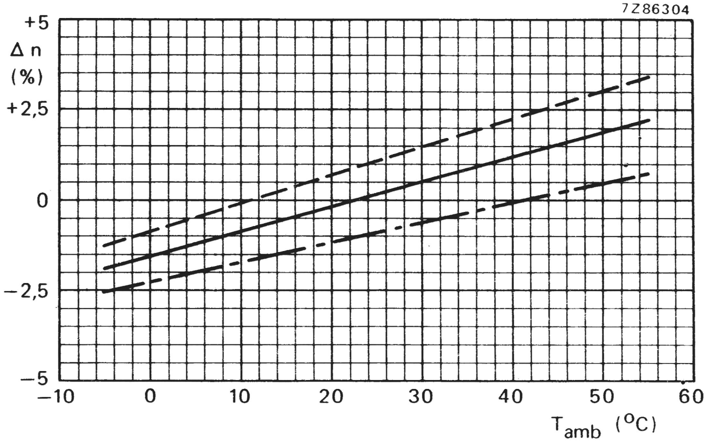


Fig. 7b $V_P = 9$ V.

Fig. 7 Variation in motor speed (n is revolutions per minute) as a function of the ambient temperature without diode (D = BA220; see Fig. 4).

– – – – – – – – : T = 0,9 mNm
———————— : T = 1,0 mNm
- — - — - — - : T = 1,1 mNm

BALANCED MIXER/MODULATOR/DEMODULATOR CIRCUIT

GENERAL DESCRIPTION

The TDA1571 is a monolithic integrated circuit which, due to the universal design, can be used in various applications such as:

- Mixer
- Modulator
- Chopper
- AM synchronous demodulator
- FM quadrature detector
- Differential amplifier

QUICK REFERENCE DATA

For application as a mixer in FM tuners; f_i = 98 MHz; f_{osc} = 108,7 MHz

Supply voltage (pins 12 and 13)	V_P	typ.	15	V
Total supply current (from V_S)	I_S	typ.	6,5	mA
Input admittance				
at pins 2 and 7 for f = 98 MHz	y_{11}	typ.	3,8 + j5	mS
at pins 3 and 5 for f = 108,5 MHz	y_{11}	typ.	2,3 + j8	mS
Mixer gain	G_{mix}	typ.	19,5	dB
Mixer noise figure	F_{mix}	typ.	6,5	dB
I.F. suppression	α_{if}	typ.	40	dB
Oscillator suppression at the input	α_{osc}	typ.	46	dB
Supply voltage range (pins 12 and 13)	V_P		4 to 25	V
Operating ambient temperature range	T_{amb}		−30 to +80	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

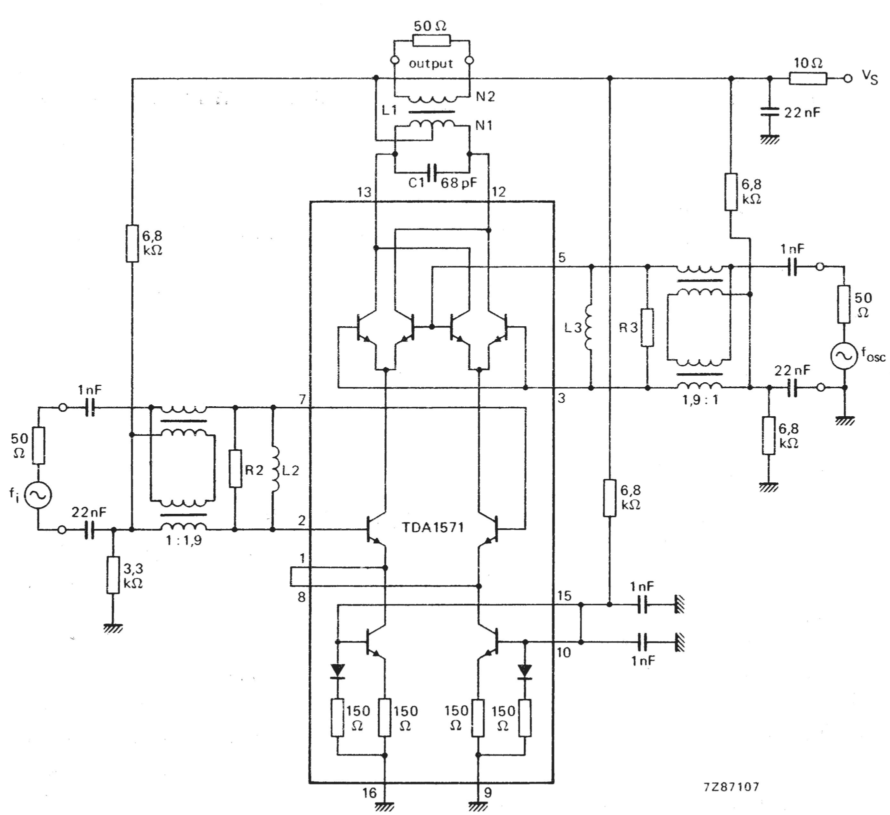

50 Ω
output
10 Ω
V_S
N2
L1
N1
22 nF
C1
68 pF
13
12
6,8 kΩ
6,8 kΩ
5
1 nF
50 Ω
L3
R3
f_{osc}
22 nF
3
1,9 : 1
6,8 kΩ
1 nF
7
50 Ω
f_i
R2
L2
22nF
2
TDA1571
1 : 1,9
3,3 kΩ
1
8
6,8 kΩ
15
1 nF
10
1 nF
150 Ω
150 Ω
150 Ω
150 Ω
16
9
7Z87107

Fig. 1 Application circuit diagram of the TDA1571 used as FM mixer; also used as test circuit for the characteristics.

Data for coil L1: N1 = 2 x 7 turns CuL (0,18 mm) on coil former
N2 = 1 turn Cul (0,18 mm) on coil former
$Q_o = 78$

L2, R2, L3 and R3 are selected for minimum reflection
$r < 0,03$; $R2 = R3 = 1\ k\Omega$

N.B.: Unused pins should be grounded.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages (pins 12 and 13)	$V_P = V_{12\text{-}9} = V_{13\text{-}16}$	max.	40 V
Voltage at pins 2 and 7	$V_{2\text{-}9} = V_{7\text{-}16}$	max.	18 V
Voltage at pins 3 and 5	$V_{3\text{-}2} = V_{5\text{-}7}$	max.	18 V
Voltage at pins 3 and 5	$V_{3\text{-}9} = V_{5\text{-}16}$	max.	23 V
Voltage at pins 12 and 13	$V_{12\text{-}3} = V_{13\text{-}5}$	max.	18 V
Voltage between pins 3 and 5	$\pm V_{3\text{-}5}$	max.	6 V
Voltage at pins 2 and 7	$-V_{2\text{-}1} = -V_{7\text{-}8}$	max.	6 V
Current on all pins	I_n	max.	10 mA
Total power dissipation	P_{tot}	max.	700 mW
Storage temperature range	T_{stg}		−55 to +150 °C
Operating ambient temperature range	T_{amb}		−30 to +80 °C

CHARACTERISTICS

f_i = 98 MHz; f_{osc} = 108,7 MHz with $R_S = R_L$ = 50 Ω; oscillator amplitude P_{osc} = −14 dBm;
T_{amb} = 25 °C; measured in test circuit in Fig. 1; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_S	—	15	—	V
Total supply current	I_S	—	6,5	—	mA
D.C. supply current output stage (pins 12 and 13)	I_P	—	2	—	mA
Input admittance					
at pins 2 and 7 for f = 98 MHz	y_{11}	—	3,8 + j5	—	mS
at pins 3 and 5 for f = 108,7 MHz	y_{11}	—	2,3 + j8	—	mS
Output admittance at pins 12 and 13 for f = 108,7 MHz	y_{22}	—	0,001 + j0,24	—	mS
Conversion transconductance of mixer	$\lvert y_{21} \rvert$	—	11	—	mS
Mixer gain	G_{mix}	—	19,5	—	dB
Mixer noise figure at R_S' = 200 Ω	F_{mix}	—	6,5	—	dB
I.F. suppression at an input signal amplitude P_i = −60 dBm	α_{if}	—	40	—	dB
Oscillator suppression					
at the input	$\alpha_{osc\ i}$	—	46	—	dB
at the i.f. output	$\alpha_{osc\ if}$	—	38	—	dB

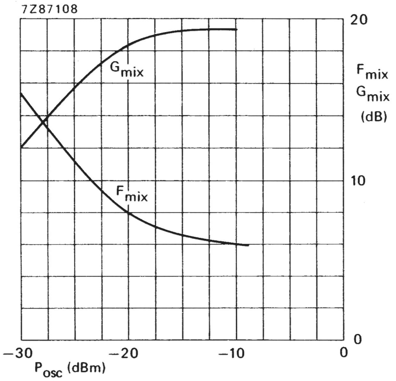


Fig. 2 Mixer gain (G_{mix}) and mixer noise figure (F_{mix}) at R_S' = 200 Ω as a function of the oscillator amplitude (P_{osc}).

DEVELOPMENT SAMPLE DATA

This information is derived from development samples
made available for evaluation. It does not necessarily
imply that the device will go into regular production.

TDA1576

FM/IF AMPLIFIER CIRCUIT

The TDA1576 is a monolithic integrated f.m./i.f. amplifier circuit provided with the following functions:

- symmetrical limiting i.f. amplifier
- symmetrical quadrature demodulator
- internal muting circuit
- symmetrical a.f.c. output
- field-strength indication output
- detune-detector
- reference voltage output
- electronic smoothing of the supply voltage
- standby on/off switching circuit.

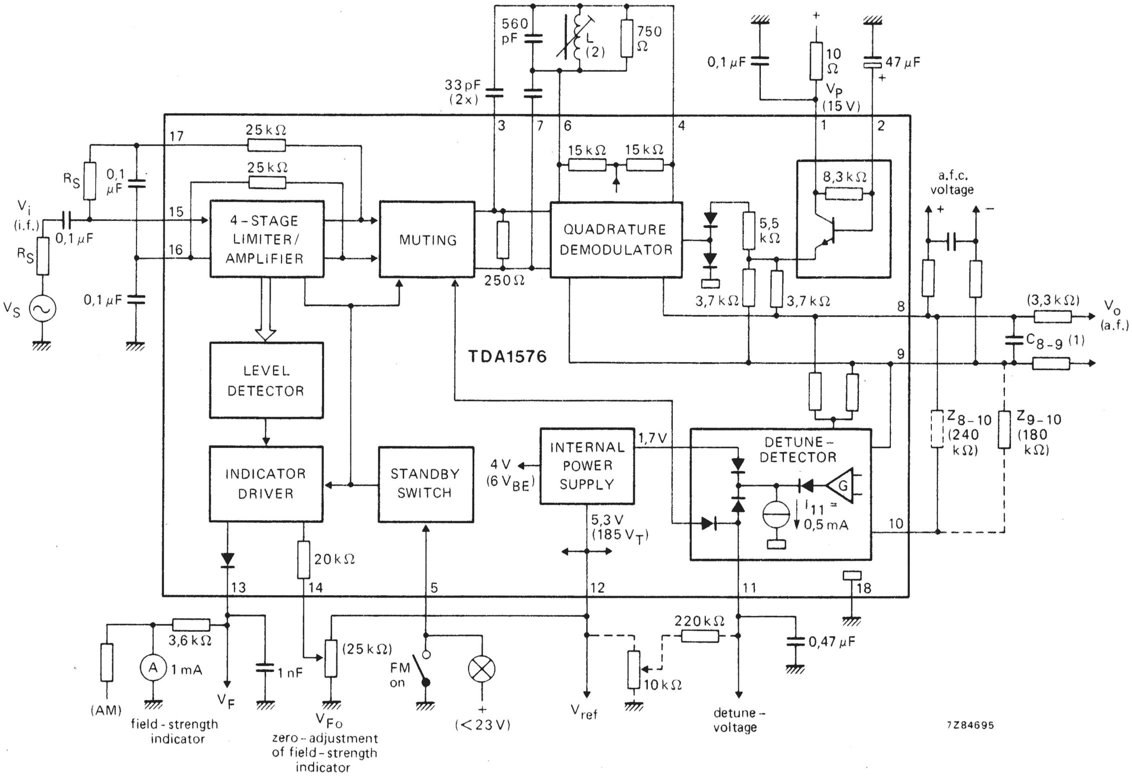
QUICK REFERENCE DATA

f_o = 10,7 MHz; $\Delta f = \pm$ 22,5 kHz; f_m = 400 Hz; Q_L = 20; de-emphasis τ = 50 μs

Supply voltages (pin 1)	V_P		8,5	15	V
Supply current	I_P	typ.	16	18	mA
Sensitivity at −3 dB before limiting	V_i	typ.	22		μV
I.F. sensitivity for					
S + N/N = 26 dB	V_i	typ.	8		μV
S + N/N = 46 dB	V_i	typ.	35		μV
A.F. output voltage	V_o	typ.	67	135	mV
Total distortion					
single tuned circuit	d_{tot}	typ.	0,1		%
two tuned circuits	d_{tot}	typ.	0,02		%
Signal plus noise-to-noise ratio; $V_i > 1$ mV	S + N/N	typ.	76	80	dB
A.M. rejection	α	typ.	50		dB
A.F.C. offset drift	$\pm \Delta f$	typ. <	3 6		kHz kHz
Field-strength indication range	ΔV_i	typ.	90		dB
Permissible indicator (load) current	I_L	<	2		mA
Supply voltage range (pin 1)	V_P		7,5 to 20		V
Ambient temperature range	T_{amb}		−30 to +80		°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102C).


TDA1576
4-STAGE LIMITER/ AMPLIFIER
MUTING
QUADRATURE DEMODULATOR
LEVEL DETECTOR
INDICATOR DRIVER
STANDBY SWITCH
INTERNAL POWER SUPPLY
DETUNE-DETECTOR
G
$I_{11} \approx 0,5$ mA
1,7 V
4 V ($6 V_{BE}$)
5,3 V ($185 V_T$)
V_i (i.f.)
R_S
R_S
V_S
0,1 μF
0,1 μF
0,1 μF
25 kΩ
25 kΩ
560 pF
L (2)
750 Ω
33 pF (2x)
15 kΩ
15 kΩ
250 Ω
5,5 kΩ
3,7 kΩ
3,7 kΩ
8,3 kΩ
0,1 μF
10 Ω
V_P (15 V)
47 μF
a.f.c. voltage
+
−
(3,3 kΩ)
V_o (a.f.)
C_{8-9} (1)
Z_{8-10} (240 kΩ)
Z_{9-10} (180 kΩ)
20 kΩ
3,6 kΩ
1 mA
1 nF
(AM)
field-strength indicator
V_F
(25 kΩ)
V_{Fo}
zero-adjustment of field-strength indicator
FM on
+ (< 23 V)
V_{ref}
10 kΩ
220 kΩ
0,47 μF
detune-voltage
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
7Z84695

(1) For de-emphasis $\tau = 50\ \mu s$: $C_{8\text{-}9} = 6{,}8$ nF.
For stereo operation: $C_{8\text{-}9} = 56$ pF.

(2) $L = 0{,}38\ \mu H$; $Q_o = 70$; $Q_L = 20$; adjusted to minimum 2nd harmonic distortion (d_2); at $V_i = 1$ mV; coil: 6 turns CuL (0,25 mm) on coil former KAN (C).

Fig. 1 Block diagram and test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1\text{-}18}$	max.	23	V
Voltages				
at pin 2	$V_{2\text{-}18}$	max.	V_P	V
	$-V_{2\text{-}18}$	max.	0	V
at pin 5	$V_{5\text{-}18}$	max.	23	V
	$-V_{5\text{-}18}$	max.	0	V
at pin 12	$V_{12\text{-}18}$	max.	7	V
	$-V_{12\text{-}18}$	max.	0	V
at pin 13	$V_{13\text{-}18}$	max.	6	V
at pin 14	$V_{14\text{-}18}$	max.	23	V
	$-V_{14\text{-}18}$	max.	0	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−55 to + 150		°C
Operating ambient temperature range	T_{amb}	−30 to + 80		°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80	K/W

CHARACTERISTICS

f_o = 10,7 MHz; $\Delta f = \pm$ 22,5 kHz; f_m = 400 Hz; R_S = 60 Ω; de-emphasis τ = 50 μs (C_{8-9} = 6,8 nF); T_{amb} = 25 °C; measured in Fig. 1, unless otherwise specified. The demodulator circuit is adjusted at minimum 2nd harmonic (d_2) distortion: V_i = 1 mV; $\Delta f = \pm$ 75 kHz.

Supply voltage range (pin 1)	V_P			7,5 to 20	V
			V_P = 8,5 V	V_P = 15 V	
Supply current; without load ($I_{12} = I_{13} = 0$)	I_P	typ.	16	18	mA
			10 to 23	12 to 25	mA
I.F. amplifier/detector					
Sensitivity at −3 dB before limiting	V_i	typ.	22		μV
		$<$	30		μV
I.F. sensitivity for					
S + N/N = 26 dB	V_i	typ.	8		μV
S + N/N = 46 dB	V_i	typ.	35		μV
I.F. output voltage (peak-to-peak value) V_i = 1 mV; $Z_{3-18} = Z_{7-18}$ = 1 MΩ in parallel with 10 pF	$V_{3-7(p-p)}$	typ.	680		mV
I.F. output resistance	R_{3-7}	typ.	250		Ω
Detector input impedance	R_{4-6}	typ.	30		kΩ
	C_{4-6}	typ.	1		pF
Output resistance	R_8; R_9	typ.	3,7		kΩ
D.C. output voltage	$V_{8-18} = V_{9-18}$	typ.	5,5	9,8	V
A.F. output voltage; Q_L = 20	V_o	typ.	67	135	mV
			60 to 75	120 to 150	mV
Total distortion					
single tuned circuit; Q_L = 20	d_{tot}	typ.	0,1		%
two tuned circuits	d_{tot}	typ.	0,02		%
Signal plus noise-to-noise ratio B = 250 Hz to 15 kHz; $V_i > 1$ mV	S + N/N	typ.	76	80	dB
A.M. rejection; V_i = 10 mV f.m.: f_m = 70 Hz; $\Delta f = \pm$ 22,5 kHz a.m.: f_m = 1 kHz; m = 0,3	α	typ.	54		dB*
I.F. input voltage range; $\alpha > 40$ dB	V_i		0,5 to 500		mV
Hum suppression at f = 100 Hz $V_P = V_{1-18}$ = 100 mV r.m.s.; C_{2-18} = 47 μF	α_{100}	$>$	43		dB
		typ.	48		dB
A.F.C. tuning slope at Q_L = 20	$\frac{\Delta V_{8-9}}{\Delta f_o}$	typ.	8,5	17	mV/kHz
A.F.C. offset voltages; Q_L = 20					
at V_i = 1 mV	$\pm \Delta V_{8-9}$	$<$	100	200	mV
at V_i = 30 μV to 500 mV (reference at 1 mV and muting)	$\pm \Delta V_{8-9}$	typ.	25	50	mV
		$<$	50	100	mV

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* Simultaneously measured.

DEVELOPMENT SAMPLE DATA

			V_P = 8,5 V	V_P = 15 V	
Field-strength indication					
Indicator sensitivity; $I_{14} = 0$	V_i		20 µV to 600 mV		
Field-strength indicator voltage $R_{13\text{-}18}$ = 3,6 kΩ; $I_{14} = 0$ $V_i = 0$	$V_F = V_{13\text{-}18}$	typ.	0		mV
		<	200		mV
V_i = 250 mV	$V_F = V_{13\text{-}18}$	typ.	3,6		V
			3,2 to 4,1		V
Available output current	$-I_{13}$	>	2		mA
Reverse voltage at the output for FM 'off'; $V_{5\text{-}18} > 3,5$ V	$V_{13\text{-}18}$	>	5		V
Detune-detector					
Quiescent input current; $V_{10\text{-}9} = 0$	I_{10}	typ.	20		nA
		<	100		nA
Output voltage range	$V_{11\text{-}18}$		1,8 to 5,0		V
Available output current	I_{11}	typ.	0,5		mA
			0,35 to 0,65		mA
Voltage gain: $\Delta V_{11}/\Delta(\pm V_{10\text{-}9})$ at I_{11} = 0,25 mA	G_v	typ.	–	3,3	
Input offset voltage (pin 10) at $V_{11\text{-}18}$ = 2,5 V	$V_{10\text{-}9}$	typ.	20		mV
Reference voltage					
Output voltage; $-I_{12}$ = 1 mA	$V_{ref} = V_{12\text{-}18}$	typ.	5,1	5,3	V
Available output current	$-I_{12}$	typ.	2,5		mA
Standby switch					
Required control voltage within the rated ambient temperature and supply voltage ranges for FM 'on'	$V_{5\,on}$	<	2		V
for FM 'off'	$V_{5\,off}$	>	3,5		V
Input switching current for FM 'on'	$-I_5$	<	100		µA

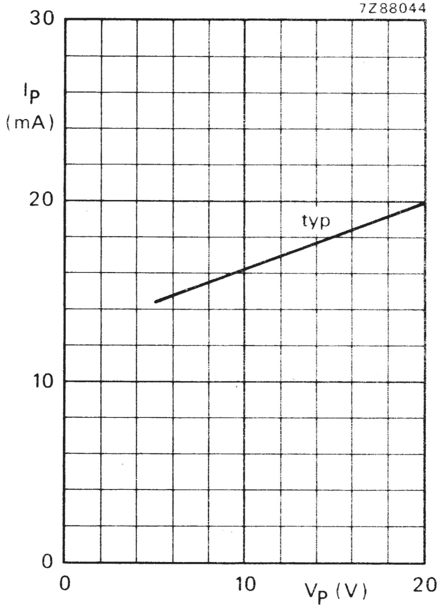


Fig. 2 Supply current consumption; without load.

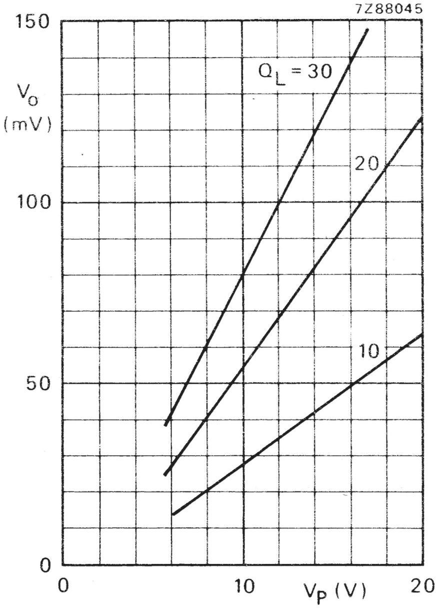


Fig. 3 A.F. output voltage; V_i = 1 mV (i.f.); Δf = ± 15 kHz; f_m = 400 Hz; typical values.

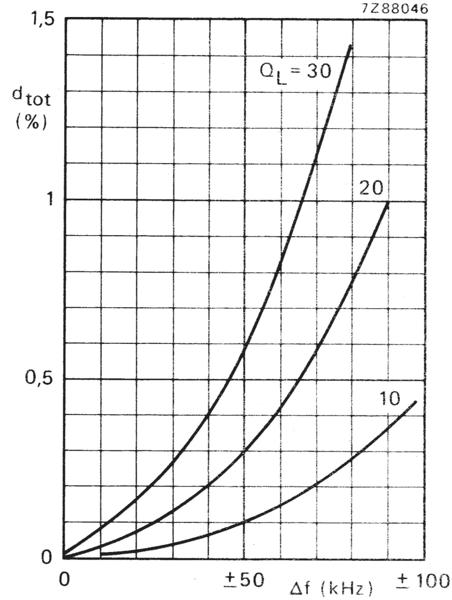


Fig. 4 Total distortion for single tuned circuit; V_i = 1 mV (i.f.); f_m = 400 Hz; adjusted at minimum 2nd harmonic distortion; typical values.

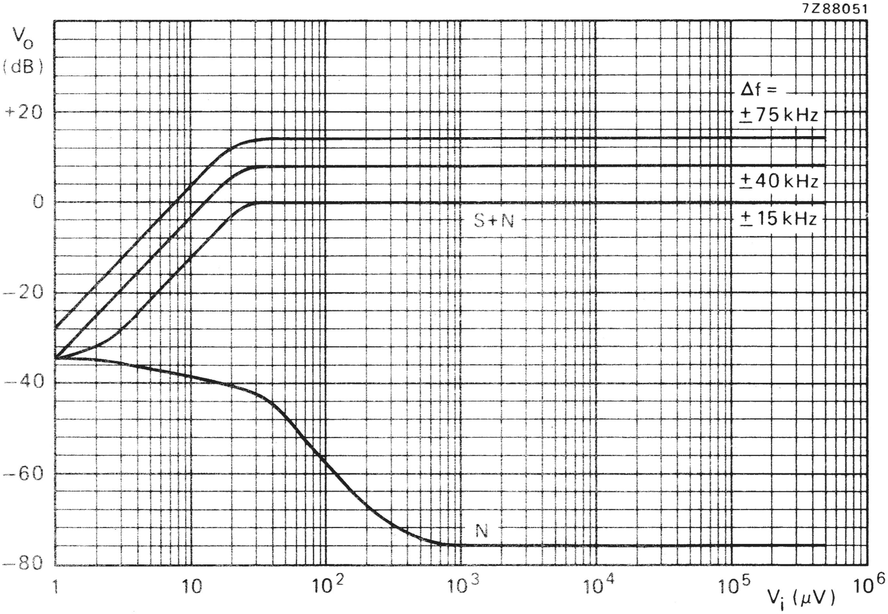


Fig. 5 A.F. output voltage level as a function of i.f. input voltage; S = signal voltage; N = noise voltage; V_P = 15 V; f_m = 400 Hz; B = 250 Hz to 16 kHz; Q_L = 20; $C_{8\text{-}9}$ = 6,8 nF; typical values.

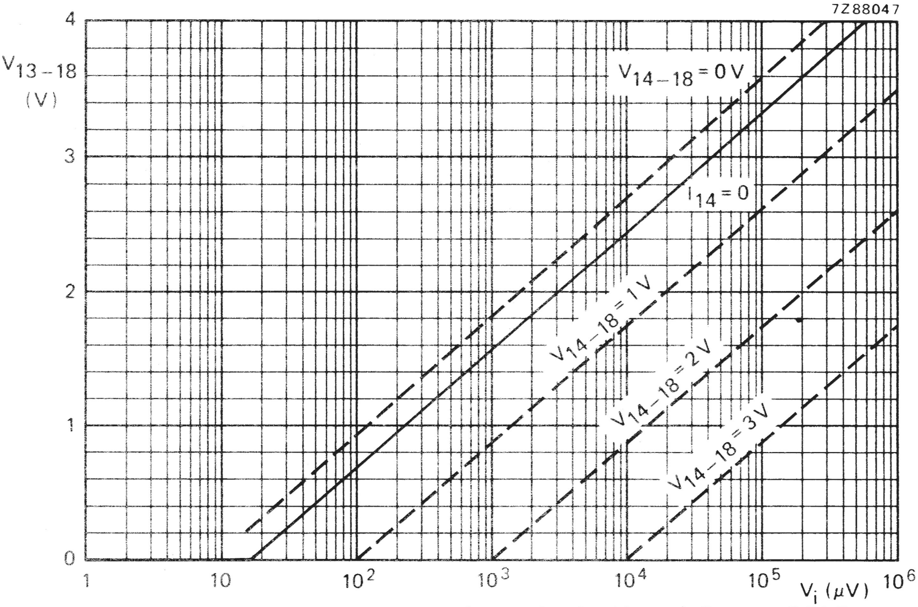


Fig. 6 Voltage at field-strength indicator output (proportional to $V_{12\text{-}18}$); $R_{13\text{-}18}$ = 3,6 kΩ.

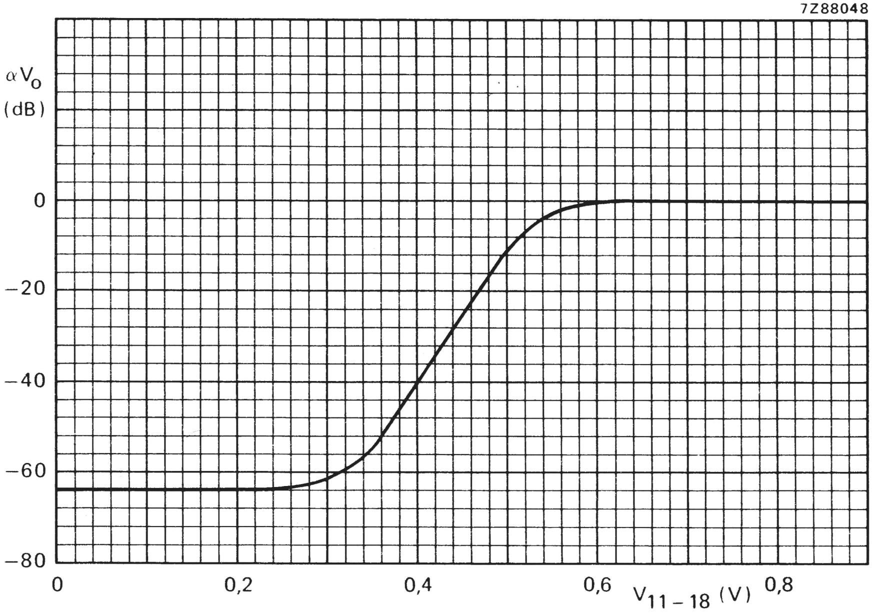


Fig. 7 Attenuation of output voltage (αV_o) as a function of the muting control voltage $V_{11\text{-}18}$.

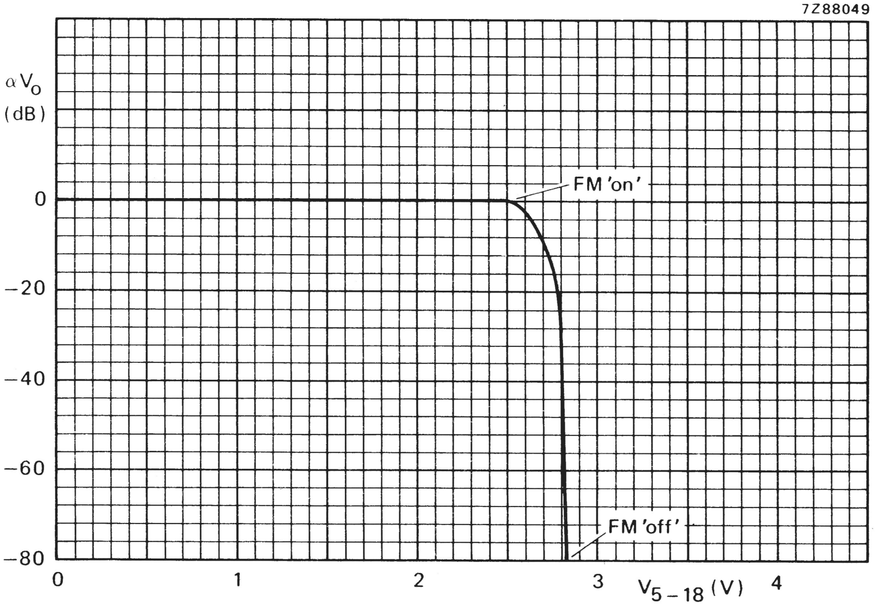
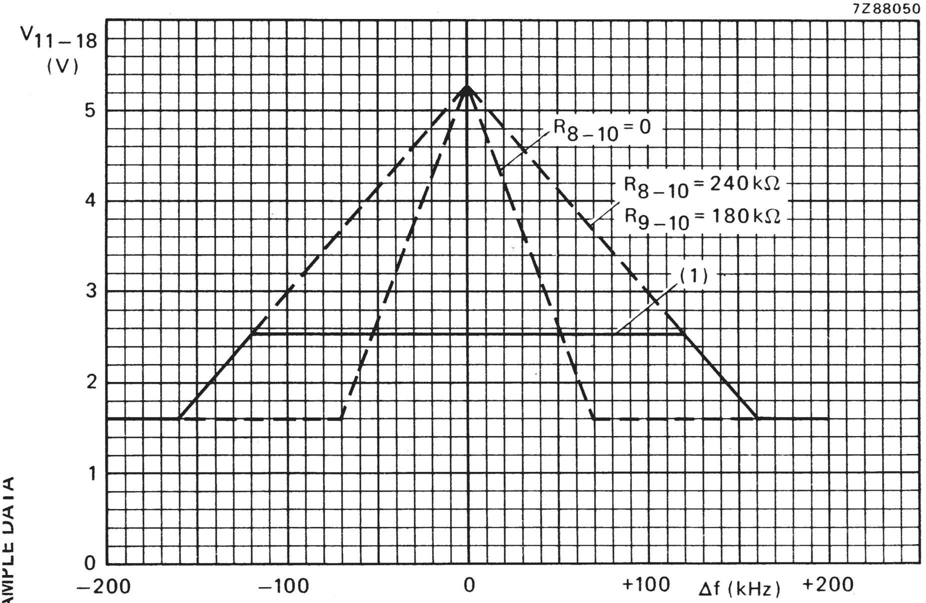


Fig. 8 FM 'on'/FM 'off' stand-by switch; attenuation of output voltage (αV_o) as a function of control voltage $V_{5\text{-}18}$.



(1) Limited by external preset ($\alpha \cdot V_{12\text{-}18}$).

Fig. 9 Detune-detector output voltage; V_P = 7,5 to 20 V; Q_L = 20.

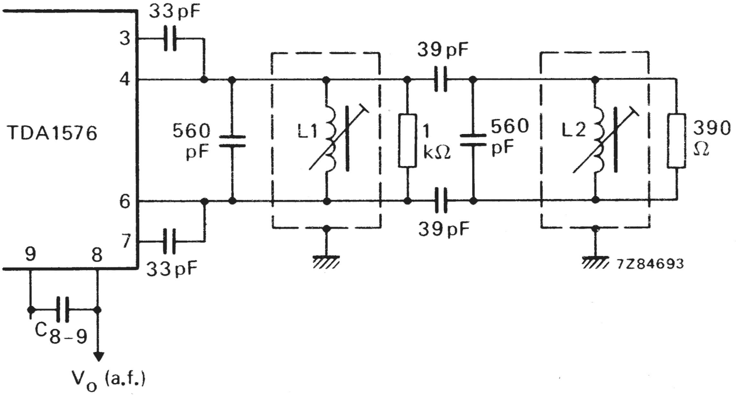

33 pF
3
4
TDA1576
560 pF
L1
39 pF
1 kΩ
560 pF
L2
390 Ω
6
39 pF
7
33 pF
9
8
C_{8-9}
V_o (a.f.)
7Z84693

Fig. 10 Example of the TDA1576 when using a demodulator with two tuned circuits. Adjustment of the demodulator circuit is obtained with an i.f. signal which is higher than the 3 dB limiting level, L2 should be short-circuited or detuned, L1 should be adjusted to min. d_2 distortion, and then L2 to min. d_2 distortion. Coil data: L1 = L2 = 0,38 μH; Q_o = 70; coil former KAN (C).

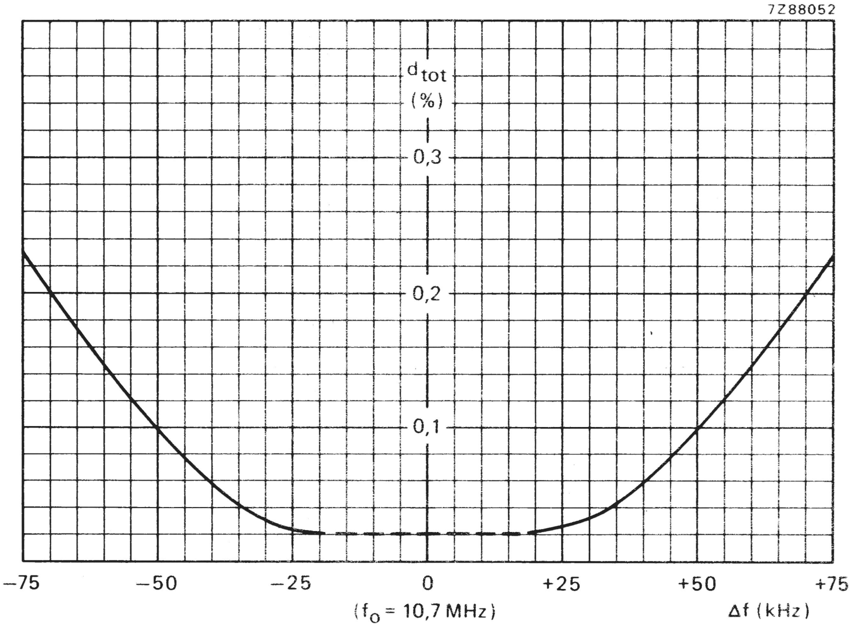
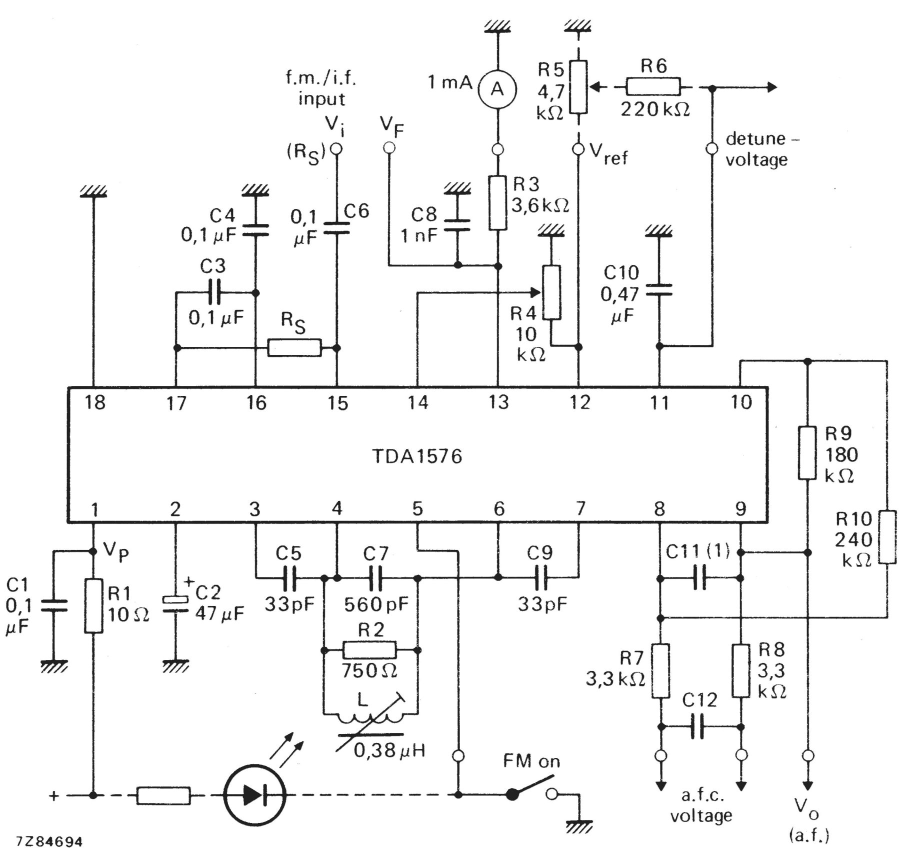


Fig. 11 Total distortion as a function of detuning; f_m = 400 Hz; $C_{8\text{-}9}$ = 6,8 nF; Δf = ± 75 kHz; V_o = 330 mV for a frequency deviation Δf = ± 75 kHz.


1 mA
A
R5
4,7
kΩ
R6
220 kΩ
f.m./i.f.
input
V_i
(R_S)
V_F
V_{ref}
detune -
voltage
C4
0,1 μF
0,1
μF
C6
C8
1 nF
R3
3,6 kΩ
C3
0,1 μF
R_S
R4
10
kΩ
C10
0,47
μF
18
17
16
15
14
13
12
11
10
TDA1576
1
2
3
4
5
6
7
8
9
R9
180
kΩ
R10
240
kΩ
V_P
C1
0,1
μF
R1
10 Ω
+
C2
47 μF
C5
33pF
C7
560 pF
C9
33pF
R2
750 Ω
L
0,38 μH
C11 (1)
R7
3,3 kΩ
R8
3,3
kΩ
C12
FM on
+
a.f.c.
voltage
V_o
(a.f.)
7Z84694

(1) For mono: C11 = 6,8 nF; for stereo: C11 = 56 pF.

Fig. 12 Application example of using TDA1576.

TIME MULTIPLEX PLL STEREO DECODER

GENERAL DESCRIPTION

The TDA1578A is a PLL stereo decoder based on the time-division multiplex principle.

Features

- adjustable input and output voltage levels
- automatic mono/stereo switching with hysteresis, controlled by both pilot signal and field strength level
- analogue control of mono/stereo change over
- pilot indicator driver
- analogue muting control
- muting indicator driver
- oscillator with decoupled frequency measurement output
- electronic smoothing of the supply voltage

QUICK REFERENCE DATA

Measured with a frequency deviation Δf = ± 75 kHz without pilot; $f_m = 1$ kHz

Supply voltage (pin 8)		$V_P = V_{8-7}$	typ.	8,5	15	V
Supply current (pin 8)		$I_P = I_8$	typ.	21	30	mA
Multiplex input signal (adjustable)		$V_{MUX(p-p)}$	typ.	0,5	1	V
Input resistance (adjustable)		R_i	typ.	47		kΩ
A.F. output voltage (R = 15 kΩ)		V_o	typ.	0,75	1,5	V
Output resistance		R_o		low-ohmic		
Spread in gain		ΔG_v	≤	1		dB
Channel separation		α	typ.	50		dB
Total harmonic distortion		THD	≤	0,3	0,1	%
Signal-to-noise ratio		S/N	typ.	90		dB
Carrier and harmonic suppression						
pilot signal;	f = 19 kHz	α_{19}	typ.	32		dB
subcarrier;	f = 38 kHz	α_{38}	typ.	50		dB
	f = 57 kHz	α_{57}	typ.	46		dB
	f = 76 kHz	α_{76}	typ.	60		dB
traffic radio (V.W.F.);	f = 57 kHz	$\alpha_{57(VWF)}$	typ.	70		dB
SCA (Subsidiary Communications Authorization);	f = 67 kHz	α_{67}	typ.	70		dB
ACI (Adjacent Channel Interference);	f = 114 kHz	α_{114}	typ.	80		dB
intermodulation;	f = 10/13 kHz	α_2, α_3	typ.	70		dB
Supply voltage range (pin 8)		$V_P = V_{8-7}$		7,5 to 18		V
Operating ambient temperature range		T_{amb}		−30 to + 80		°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102C).

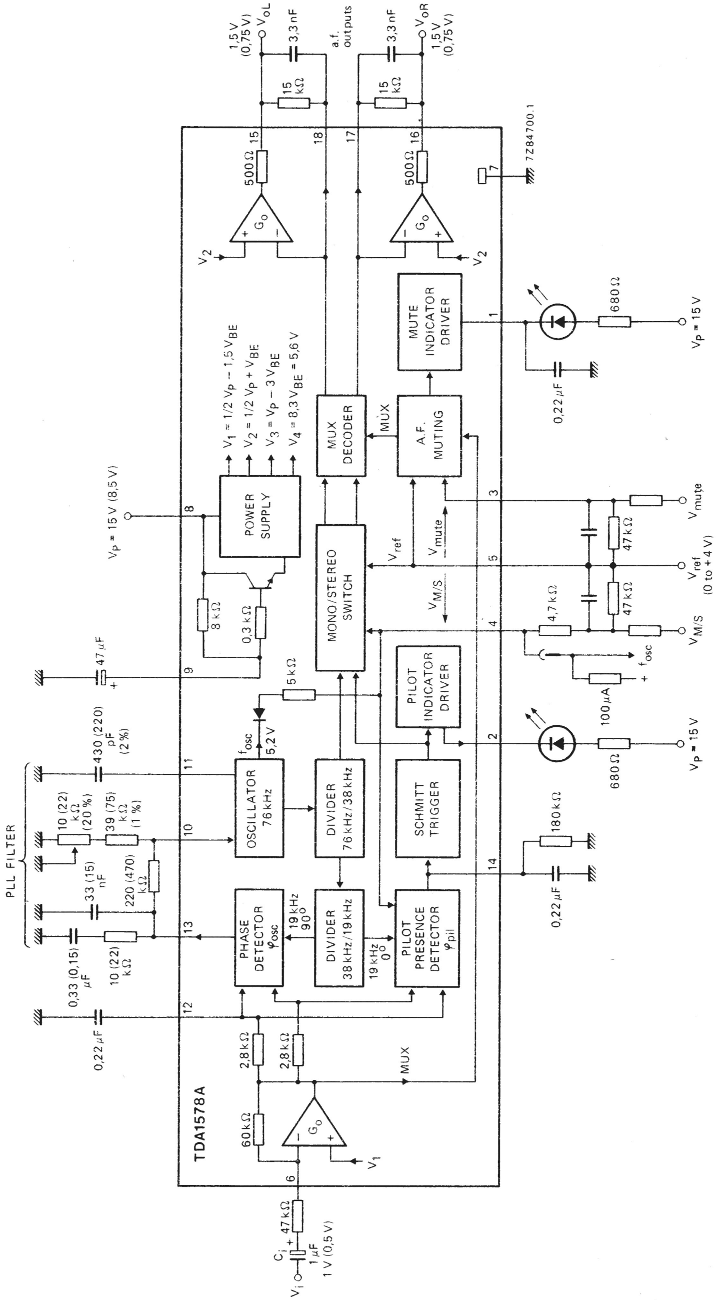

TDA1578A
OSCILLATOR 76 kHz
PHASE DETECTOR φ_{osc}
DIVIDER 76 kHz/38 kHz
DIVIDER 38 kHz/19 kHz
PILOT PRESENCE DETECTOR φ_{pil}
SCHMITT TRIGGER
PILOT INDICATOR DRIVER
MONO/STEREO SWITCH
POWER SUPPLY
MUX DECODER
A.F. MUTING
MUTE INDICATOR DRIVER
PLL FILTER
$V_1 = 1/2\ V_P - 1{,}5\ V_{BE}$
$V_2 = 1/2\ V_P + V_{BE}$
$V_3 = V_P - 3\ V_{BE}$
$V_4 = 8{,}3\ V_{BE} = 5{,}6\ V$
$V_P = 15\ V\ (8{,}5\ V)$
V_{oL}
V_{oR}
1,5 V (0,75 V)
a.f. outputs
3,3 nF
15 kΩ
500 Ω
G_o
V_1
V_2
MUX
V_{ref}
V_{mute}
$V_{M/S}$
V_{ref} (0 to +4 V)
47 kΩ
4,7 kΩ
f_{osc}
100 µA
680 Ω
$V_P = 15\ V$
0,22 µF
180 kΩ
19 kHz 90°
19 kHz 0°
5,2 V
5 kΩ
8 kΩ
0,3 kΩ
47 µF
430 (220) pF (2 %)
10 (22) kΩ (20 %)
39 (75) kΩ (1 %)
33 (15) nF
220 (470) kΩ
0,33 (0,15) µF
10 (22) kΩ
2,8 kΩ
60 kΩ
47 kΩ
C_i 1 µF
V_i 1 V (0,5 V)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
7Z84700.1

Fig. 1 Block diagram with external components; used as test circuit. Values given in parentheses are for $V_P = 8{,}5\ V$.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_P = V_{8\text{-}7}$	max.	20	V
Input voltages (pins 3, 4 and 5)	$V_{3;4;5\text{-}7}$		0 to 12	V
Indicator driver output voltage	$V_{1;2\text{-}7}$	max.	24	V
Indicator driver output current	$I_1; I_2$	max.	30	mA
Total power dissipation at T_{amb} = 25 °C	P_{tot}	max.	1,2	W
Storage temperature range	T_{stg}		–55 to + 150	°C
Operating ambient temperature range	T_{amb}		–30 to + 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\,c\text{-}a}$	=	80	K/W

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (measured in Fig. 1)

Input signal: m = 100% ($\Delta f = \pm 75$ kHz); pilot signal: m = 9% ($\Delta f = \pm 6{,}75$ kHz);
modulation frequency: 1 kHz; $V_{3\text{-}5} = V_{4\text{-}5} = 0$ V;
de-emphasizing time: T = 50 μs; oscillator adjusted to f_{osc} at a pilot voltage $V_i = 0$ V;
$T_{amb} = 25\ ^oC$; unless otherwise specified

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Supply voltage range (pin 8)	–	V_P	7,5	–	18	V
Supply current (except	8,5	I_P	–	21	–	mA
output and indicator) pin 8	15	I_P	–	30	40	mA
Nominal multiplex input						
voltage (peak-to-peak value)	8,5	$V_{MUX(p\text{-}p)}$	–	0,5	–	V
$R_i = 47\ k\Omega$	15	$V_{MUX(p\text{-}p)}$	–	1,0	–	V
Overdrive reserve of input						
at THD = 1 %	8,5		3	6	–	dB
at THD = 0,3 %	15		3	6	–	dB
A.F. output voltage (r.m.s. value; mono without pilot)						
$R_{15\text{-}18} = R_{16\text{-}17} = 15\ k\Omega$	8,5	$V_{o(rms)}$	–	0,75	–	V
	15	$V_{o(rms)}$	–	1,5	–	V
$R_{15\text{-}18} = R_{16\text{-}17} = 24\ k\Omega$	8,5	$V_{o(rms)}$	–	1,2	–	V
	15	$V_{o(rms)}$	–	2,4	–	V
Overdrive reserve of output $R_{15\text{-}18} = R_{16\text{-}17} = 24\ k\Omega$	*		3	–	–	dB
Spread in output voltage levels	*	$\pm \Delta V_o/V_o$	–	–	1	dB
Difference of output voltage levels	*	$\pm \Delta V_{15\text{-}16}/V_o$	–	–	1	dB
Output resistance	*	R_o	low-ohmic			
Available output current pins 15 and 16	*	$\pm I_o$	–	–	–	mA
Modulation range at output (unloaded)	*	$V_{15;16\text{-}7}$	–	1 to $V_{9\text{-}7} - 1$	–	V
Internal current limiting	*	I_o	–	15	–	mA
D.C. output voltage	8,5	$V_{15;16\text{-}7}$	3,6	4,1	4,6	V
$R_{15\text{-}18} = R_{16\text{-}17} = 24\ k\Omega$	15	$V_{15;16\text{-}7}$	7,0	7,7	8,4	V
D.C. current	8,5	$-I_{17;18}$	–	33	–	μA
(pins 17 and 18)	15	$-I_{17;18}$	–	23	–	μA

* V_P = 8,5 or 15 V.

parameter	Vp (V)	symbol	min.	typ.	max.	unit
Channel separation	8,5	α	32	50	–	dB
at V_{4-5} = 0 V	15	α	39	50	–	dB
Total harmonic distortion	8,5	THD	–	0,1	0,3	%
	15	THD	–	0,04	0,1	%
Signal-to-noise ratio	8,5	S/N	–	87	–	dB
f = 20 Hz to 16 kHz	15	S/N	–	90	–	dB
Carrier and harmonic suppression at the output						
pilot signal; f = 19 kHz	*	α_{19}	–	32	–	dB
subcarrier; f = 38 kHz	*	α_{38}	40	50	–	dB
f = 57 kHz	*	α_{57}	–	46	–	dB
f = 76 kHz	*	α_{76}	–	60	–	dB
intermodulation (note 1) f_m = 10 kHz; spurious signal f_s = 1 kHz						
PLL-filter Fig. 1	*	α_2	–	50	–	dB
PLL-filter Fig. 2	*	α_2	–	70	–	dB
f_m = 13 kHz; spurious signal f_s = 1 kHz	*	α_3	–	75	–	dB
traffic radio (V.W.F.); f = 57 kHz (note 2)	*	$\alpha_{57(VWF)}$	–	70	–	dB
SCA (Subsidiary Communications Authorization); f = 67 kHz (note 4)	*	α_{67}	–	70	–	dB
ACI (Adjacent Channel Interference) (note 3);						
f = 114 kHz	*	α_{114}	–	80	–	dB
f = 190 kHz	*	α_{190}	–	52	–	dB
Ripple rejection at the output; f = 100 Hz; $V_{P(rms)}$ = 100 mV (pin 8)	*	RR_{100}	40	43	–	dB
Voltage on filter capacitor without external load	*	V_{9-7}	–	V_P–0,25	–	V
Source resistance	*	R_{9-8}	6	8	10	kΩ

* V_P = 8,5 or 15 V.

CHARACTERISTICS (continued)

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Mono/stereo control						
Pilot threshold voltages (peak-to-peak values)						
for stereo 'ON'	8,5	$V_{i(p-p)}$	—	21	30	mV
	15	$V_{i(p-p)}$	—	43	61	mV
for mono 'ON'	8,5	$V_{i(p-p)}$	6	15	—	mV
	15	$V_{i(p-p)}$	12	30	—	mV
Switch hysteresis $V_{i\,ON}/V_{i\,OFF}$	*	ΔV_i	—	3	—	dB
Switching time at $C_{14-7} = 0{,}22\ \mu F$						
for stereo 'ON'	*	t_{st} ON	—	15	—	ms
for mono 'ON'	*	t_m ON	—	27	—	ms
External mono/stereo control (see Fig. 12 and note 5)						
Switching voltage for external mono control	8,5	V_{14-7}	—	—	0,7	V
	15	V_{14-7}	—	—	1,4	V
	*	or: $-V_{4-5}$	300	—	—	mV
Control voltage for channel separation: $\alpha = 6$ dB	8,5	$-V_{4-5}$	—	120	—	mV
	15	$-V_{4-5}$	—	130	—	mV
	*	ΔV_{4-5}	—	—	± 20	mV
$\alpha = 26$ dB	8,5	$-V_{4-5}$	—	70	—	mV
	15	$-V_{4-5}$	—	80	—	mV
Control voltage						
for mono 'ON'	8,5	$-V_{4-5}$	—	240	—	mV
	15	$-V_{4-5}$	—	270	—	mV
for stereo 'ON'	8,5	$-V_{4-5}$	—	220	—	mV
	15	$-V_{4-5}$	—	250	—	mV
Control voltage difference for $\alpha = 6$ dB; stereo 'ON'	8,5	ΔV_{4-7}	80	100	120	mV

---

* $V_P = 8{,}5$ or 15 V.

parameter	V_P (V)	symbol	min.	typ.	max.	unit
Muting circuit (see Fig. 13 and note 5)						
Control voltage for an attenuation: $\alpha = 3$ dB	8,5	$-V_{3\text{-}5}$	–	140	–	mV
	15	$-V_{3\text{-}5}$	–	145	–	mV
	*	$\Delta V_{3\text{-}5}$	–	± 20	–	mV
$\alpha = 26$ dB	8,5	$-V_{3\text{-}5}$	–	255	–	mV
	15	$-V_{3\text{-}5}$	–	270	–	mV
Attenuation						
with $V_{3\text{-}5} = 0$ V	*	α	–	–	0,2	dB
with $-V_{3\text{-}5} = 450$ mV	*	α	–	80	–	dB
LED driver output current at an attenuation: $\alpha = 3$ dB	*	I_1	1,2	1,7	2,2	mA
Control voltage for $I_1 = 200\ \mu$A	8,5	$-V_{3\text{-}5}$	–	150	–	mV
	15	$-V_{3\text{-}5}$	–	160	–	mV
Control inputs						
Recommended voltage range	*	$V_{3;4;5\text{-}7}$	0	–	4	V
Input bias current	*	$I_{3;4;5}$	–	10	100	nA
Indicator driver						
Output saturation voltages						
at $I_1 = 20$ mA; $V_{3\text{-}5} = 0$ V	*	$V_{1\text{-}7sat}$	–	1,2	1,8	V
at $I_2 = 20$ mA	*	$V_{2\text{-}7sat}$	–	0,5	1,0	V
Output leakage current at $V_{1;2\text{-}7} = 24$ V	*	$I_{1;2}$	–	20	–	μA

DEVELOPMENT SAMPLE DATA

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* V_P = 8,5 or 15 V.

CHARACTERISTICS (continued)

parameter	V_P (V)	symbol	min.	typ.	max.	unit
VCO						
Oscillator frequency adjustable with $R_{10\text{-}7}$	*	f_{osc}	–	76	–	kHz
Spread of free-running frequency at nominal external circuitry	*	f_{osc}	71	–	82	kHz
Free-running frequency dependency (note 6)						
with temperature	*	TC	–	1×10^{-4}	–	K^{-1}
with supply voltage	*	$\Delta f_{osc}/\Delta V_P$	–	–	400	Hz/V
Capture and holding range for a pilot input voltage $V_{pil} = 0{,}5 \times V_{pil\,nom}$	*	$\Delta f/f$	± 2	–	–	%
PLL control slope (total)	*	S_{tot}	–	4,5	–	kHz/μs
D.C. voltage at pin 10	*	$V_{10\text{-}7}$ or:	– –	2,1 $3{,}2\ V_{BE}$	– –	V V
Frequency measuring point; internal switching threshold	*	$V_{4\text{-}7}$ or:	– –	6 $9\ V_{BE}$	– –	V V
Output voltage (peak-to-peak value) at pin 4; R = 4,7 kΩ	*	$V_{4\text{-}7(p\text{-}p)}$	–	350	–	mV
Output resistance	*	$R_{4\text{-}7}$	–	5	–	kΩ

---

* V_P = 8,5 or 15 V.

Notes to the characteristics

1. Intermodulation suppression (BFC: Beat-Frequency Components)

$$\alpha_2 = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz})};\ f_s = (2 \times 10\ \text{kHz}) - 19\ \text{kHz}$$

$$\alpha_3 = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz})};\ f_s = (3 \times 13\ \text{kHz}) - 38\ \text{kHz}$$

measured with: 91% mono signal; f_m = 10 or 13 kHz; 9% pilot signal.

2. Traffic radio (V.W.F.) suppression

$$\alpha_{57(VWF)} = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 1 kHz} \pm \text{23 kHz})}$$

measured with: 91% stereo signal; f_m = 1 kHz; 9% pilot signal;
5% traffic subcarrier (f = 57 Hz, f_m = 23 Hz AM, m = 60%).

3. ACI (Adjacent Channel Interference)

$$\alpha_{114} = \frac{V_{o\ (signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 4 kHz})};\ f_s = 110\ \text{kHz} - (3 \times 38\ \text{kHz})$$

$$\alpha_{190} = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 4 kHz})};\ f_s = 186\ \text{kHz} - (5 \times 38\ \text{kHz})$$

measured with: 90% mono signal; f_m = 1 kHz; 9% pilot signal;
1% spurious signal (f_s = 110 or 186 kHz, unmodulated).

4. SCA (Subsidiary Communications Authorization)

$$\alpha_{67} = \frac{V_{o(signal)}\ (\text{at 1 kHz})}{V_{o(spurious)}\ (\text{at 9 kHz})};\ f_s = (2 \times 38\ \text{kHz}) - 67\ \text{kHz}$$

measured with: 81% mono signal; f_m = 1 kHz; 9% pilot signal;
10% SCA-subcarrier (f_s = 67 kHz, unmodulated).

5. Assuming $V_T = \frac{k \times T}{q} = 28{,}6\ \text{mV}$ at $T_j = 330\ \text{K}$.

6. The effects of external components are not taken into account.

APPLICATION NOTES

1. When mono/stereo control and muting control are not used, pins 3, 4 and 5 have to be grounded.
2. In a receiver, channel separation adjustment can be obtained by:
   - a. A capacitor at pin 12 ($C_{12\text{-}7}$): phasing 19/38 kHz
   - b. RC or LCR filter at the input: frequency response compensation ($V_G = f(\omega)$)
   - c. Feeding the output signals of the output amplifier to the inputs of the other channel.
3. PLL-filter for reduced intermodulation (α_2); see Fig. 2.
4. External mono 'ON' switch; see Fig. 3.
5. Switching 'OFF' the oscillator; see Fig. 4.

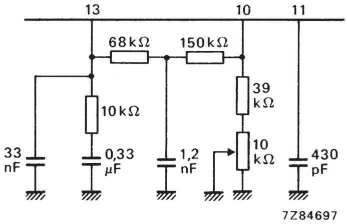

13
10
11
68 kΩ
150 kΩ
10 kΩ
39 kΩ
10 kΩ
33 nF
0,33 µF
1,2 nF
430 pF
7Z84697

Fig. 2 PLL-filter for α_2 = 70 dB at V_P = 15 V (see also Fig. 1).

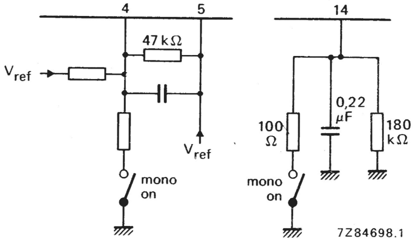

4
5
47 kΩ
V_{ref}
V_{ref}
mono on
14
0,22 µF
100 Ω
180 kΩ
mono on
7Z84698.1

Fig. 3 (a) At pin 4; $-V_{4\text{-}5} > 300$ mV; (b) at pin 14.

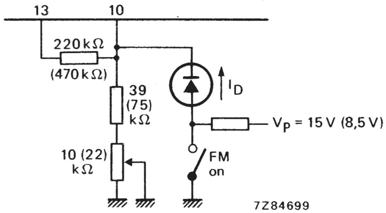

13
10
220 kΩ
(470 kΩ)
39 (75) kΩ
10 (22) kΩ
I_D
V_P = 15 V (8,5 V)
FM on
7Z84699

Fig. 4 The oscillator is switched-off when: $I_D > 100\ \mu A$ ($> 50\ \mu A$ for $V_P = 8{,}5$ V) and $I_D < 1$ mA.

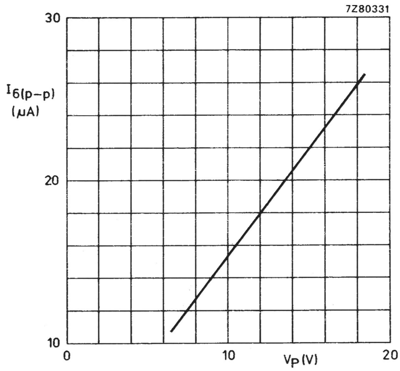


Fig. 5 Signal handling range at the input for I_{6nom} (± 75 kHz); $V_{9\text{-}7} = V_P$.

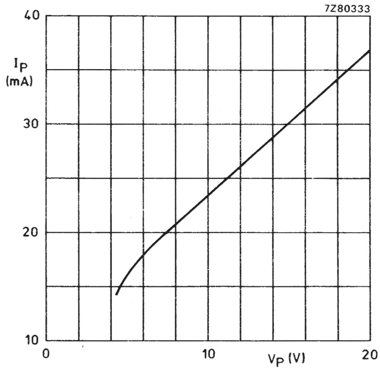


Fig. 6 Supply current comsumption at $V_{9\text{-}7} = V_P$.

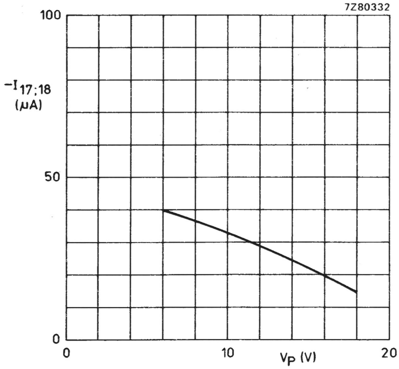


Fig. 7 D.C. current in the feedback loop of the output amplifier.

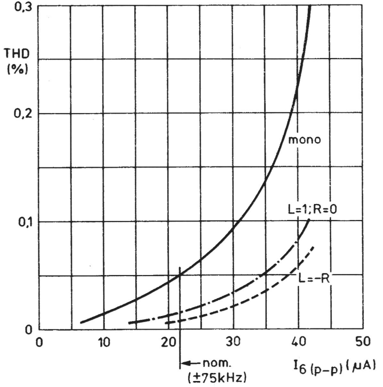


Fig. 8 Total harmonic distortion (THD) as a function of the peak-to-peak input current at pin 6; V_P = 15 V; f_m = 1 kHz; $V_{3\text{-}5} = V_{4\text{-}5}$ = 0 V.

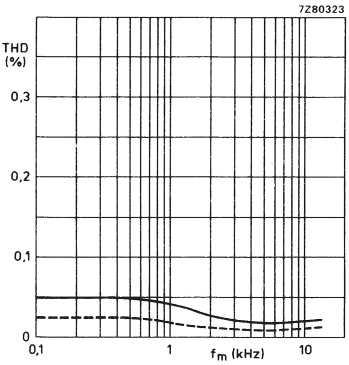


Fig. 9 Total harmonic distortion (THD) as a function of the modulation frequency (f_m); V_P = 15 V; $I_{6(p\text{-}p)}$ = 21,5 μA.

———— mono

– – – – stereo; L = −R; 91% + 9% pilot signal.

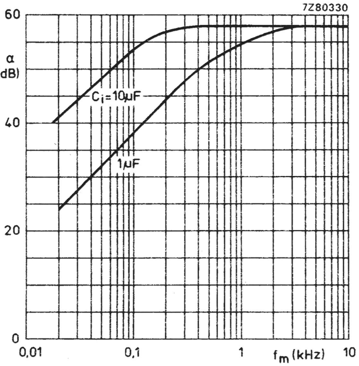


Fig. 10 Channel separation (α) as a function of the modulation frequency (f_m); V_P = 15 V; R_i = 47 kΩ; $V_{4\text{-}5}$ = 0 V.

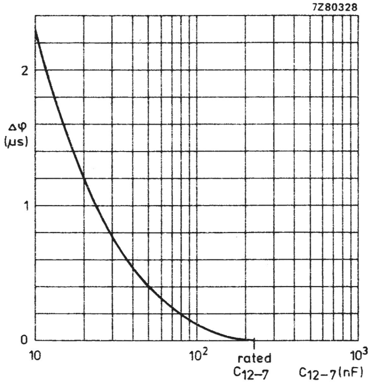


Fig. 11 Phase shift between pilot signal at the input and the internal carrier processing as a function of $C_{12\text{-}7}$.

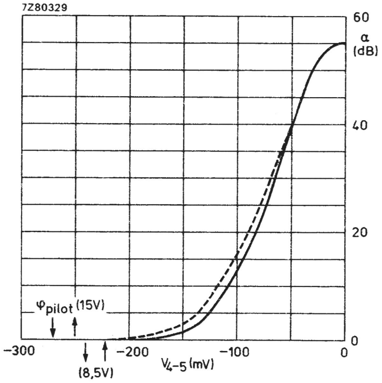


Fig. 12 Mono/stereo control at f_m = 1 kHz; α is the channel separation.
———— V_P = 8,5 V
– – – – V_P = 15 V

DEVELOPMENT SAMPLE DATA

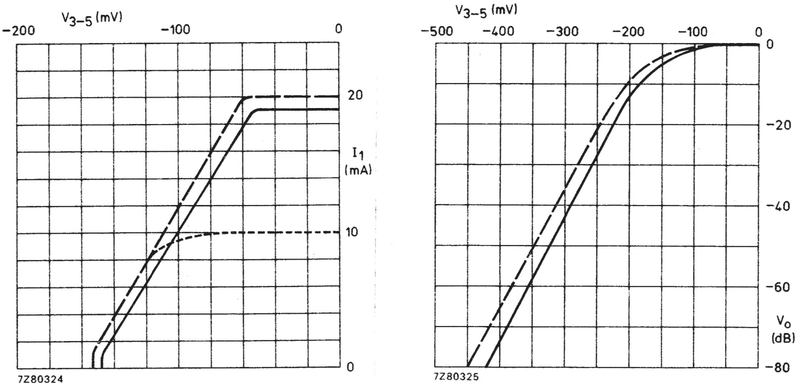


Fig. 13 Muting (V_o) and muting indicator current (I_1) as a function of $V_{3\text{-}5}$.

V_o in dB curves; ——— V_P = 8,5 V
– – – – V_P = 15 V

I_1 in mA curves for V_{PL}/R_{bias1} (pin 1); – – – – 22 V/1 kΩ
——— 14 V/680 Ω
- - - - - - - 10 V/680 Ω

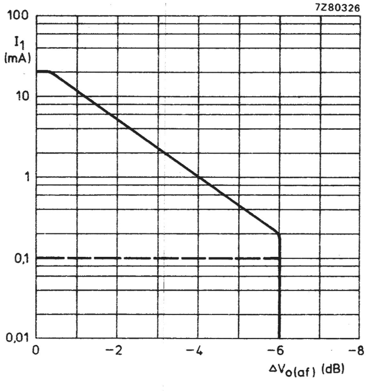


Fig. 14 Muting indicator current; V_P = 8,5 to 15 V; V_{PL} = 14 V.

——— R_{bias1} = 680 Ω
– – – – R_{bias1} = matched

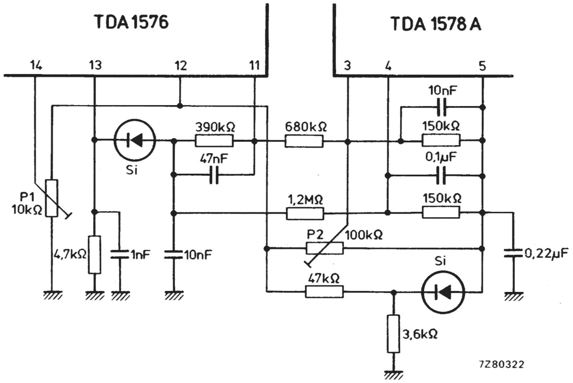

TDA1576
TDA 1578 A
14
13
12
11
3
4
5
10nF
390kΩ
680kΩ
150kΩ
47nF
0,1μF
Si
P1
10kΩ
1,2MΩ
150kΩ
P2
100kΩ
4,7kΩ
1nF
10nF
0,22μF
47kΩ
Si
3,6kΩ
7Z80322

Fig. 15 Application information for external circuitry to provide external mono/stereo and muting control.

Adjustment recommendations:

at $V_{i(hf)}$ = 100 μV with P1 to α = 6 dB (channel separation),
at $V_{i(hf)}$ = 15 μV with P2 to $V_{o(af)}$ = –3 dB.

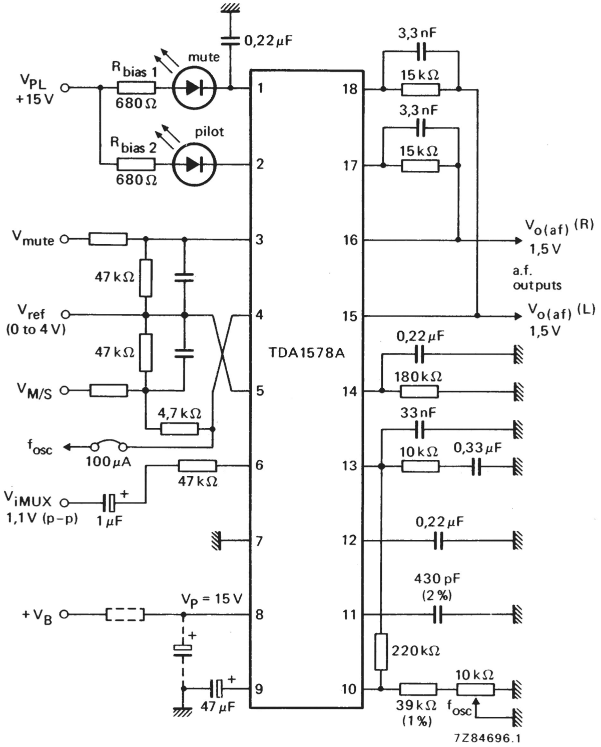

0,22μF
mute
$R_{bias\,1}$
680Ω
V_{PL}
+15V
pilot
$R_{bias\,2}$
680Ω
3,3nF
15kΩ
3,3nF
15kΩ
1
2
18
17
V_{mute}
3
16
47kΩ
$V_{o(af)}$ (R)
1,5V
a.f. outputs
V_{ref}
(0 to 4 V)
4
15
$V_{o(af)}$ (L)
1,5V
47kΩ
TDA1578A
0,22μF
$V_{M/S}$
5
14
180kΩ
4,7kΩ
33nF
f_{osc}
100μA
10kΩ
0,33μF
6
13
47kΩ
V_{iMUX}
1,1V (p-p)
1μF
7
12
0,22μF
430pF
(2%)
V_P = 15 V
$+V_B$
8
11
220kΩ
9
10
47μF
10kΩ
39kΩ
(1%)
f_{osc}
7Z84696.1

Fig. 16 Typical application circuit using TDA1578A for V_P = 15 V.

AUTOMATIC TUNING CIRCUIT

GENERAL DESCRIPTION

The TDA1580 is a monolithic integrated circuit for automatic tuning applications in TV and radio receivers.

Features

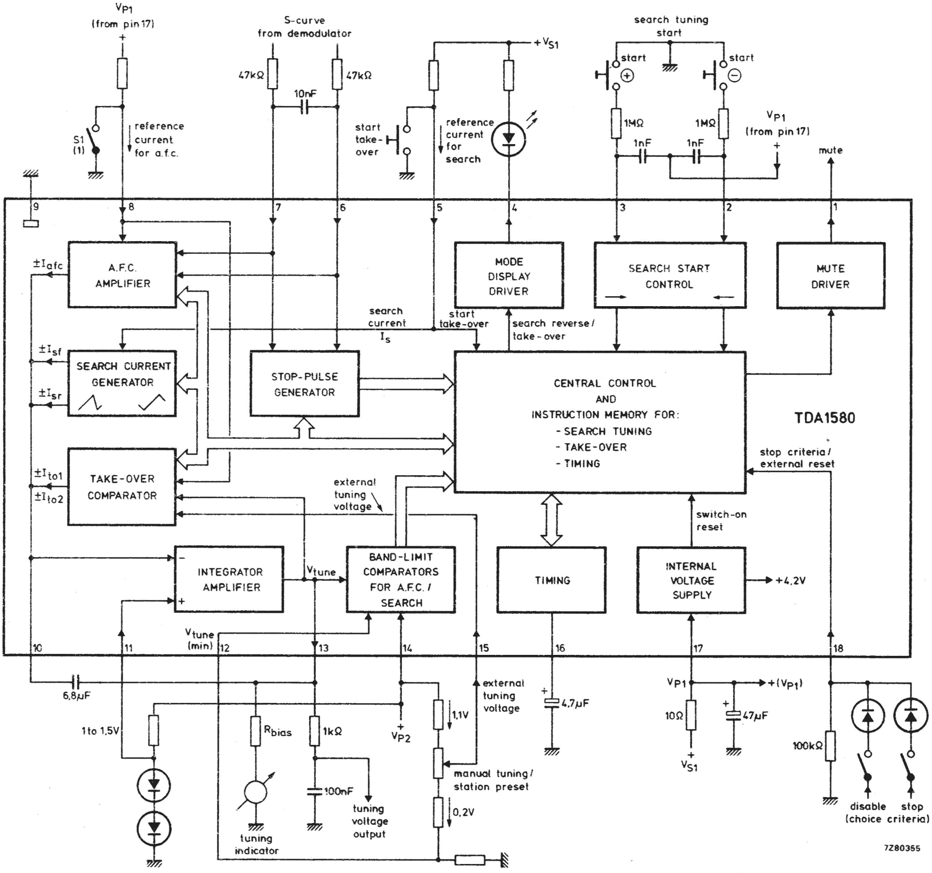
- Bi-directional search; sawtooth characteristic
- Stop-pulse generator (S-curve evaluation)
- Start/stop memory
- Internal control of timing and mute operation
- Take-over circuit for external station-presets
- Search tuning always starts from previous tuning position
- Integrating a.f.c.
- Integrator/amplifier for driving analogue displays
- Comparators for band limits
- Station select input (e.g. field-strength, stereo, traffic news, TV carrier)
- Adjustable a.f.c. and search-tuning characteristic
- Internal switch-on reset (preset station circuit take-over)

QUICK REFERENCE DATA

Supply voltages				
(pin 17)	V_{P1}	typ.	15	V
(pin 14)	V_{P2}	typ.	30	V
Supply currents (unloaded)				
(pin 17)	I_{P1}	typ.	10	mA
(pin 14)	I_{P2}	typ.	1,2	mA
Tuning voltage	$V_{13\text{-}9}$		0,5 to $V_{P2}-1$	V
Permissible load current (for display)	I_{13}	typ.	1,2	mA
Integrator current for search (adjustable)	$\pm I_{s10}$		20 to 200	μA
Integrator input current (a.f.c. off)	I_{o10}	typ.	10	nA
Input voltage range for the a.f.c. inputs	$V_{6;7\text{-}9}$		2,5 to $V_{P1}-1,4$	V
Supply voltage ranges				
(pin 17)	V_{P1}		6 to 24	V
(pin 14)	V_{P2}		6 to 33	V
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102CS).


V_{P1}
(from pin 17)
reference current for a.f.c.
S1 (1)
S-curve from demodulator
47kΩ
10nF
47kΩ
start take-over
$+V_{S1}$
reference current for search
search tuning start
start ⊕
start ⊖
1MΩ
1MΩ
1nF
1nF
V_{P1} (from pin 17)
mute
9
8
7
6
5
4
3
2
1
$\pm I_{afc}$
A.F.C. AMPLIFIER
search current I_s
start take-over
search reverse / take-over
MODE DISPLAY DRIVER
SEARCH START CONTROL
MUTE DRIVER
$\pm I_{sf}$
$\pm I_{sr}$
SEARCH CURRENT GENERATOR
STOP-PULSE GENERATOR
CENTRAL CONTROL AND INSTRUCTION MEMORY FOR:
- SEARCH TUNING
- TAKE-OVER
- TIMING
TDA1580
stop criteria / external reset
$\pm I_{to1}$
$\pm I_{to2}$
TAKE-OVER COMPARATOR
external tuning voltage
switch-on reset
INTEGRATOR AMPLIFIER
V_{tune}
BAND-LIMIT COMPARATORS FOR A.F.C. / SEARCH
TIMING
INTERNAL VOLTAGE SUPPLY
+4,2V
V_{tune} (min)
10
11
12
13
14
15
16
17
18
6,8µF
1 to 1,5V
R_{bias}
1kΩ
V_{P2}
1,1V
external tuning voltage
4,7µF
V_{P1}
$+(V_{P1})$
10Ω
47µF
100kΩ
tuning indicator
100nF
tuning voltage output
manual tuning / station preset
0,2V
V_{S1}
disable
stop
(choice criteria)
7Z80355

(1) S1:

1 — A.F.C. OFF (search stand-by mode)

2 — Continuous take-over without muting (take-over stand-by mode)

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 17)		V_{P1}	max.	24	V
Supply voltage (pin 14)		V_{P2}	max.	33	V

Voltages/currents

Mute output (pin 1)		$V_{1\text{-}9}$	max.	33	V
		I_1	max.	10	mA
		$-V_{1\text{-}9}$	max.	0,5	V
	or:	$-I_1$	max.	10	mA
Start inputs (pins 2 and 3)		$V_{2;3\text{-}9}$	max.	$V_{P1}+0,5$	V
	or:	$I_{2;3}$	max.	10	mA
		$-V_{2;3\text{-}9}$	max.	5	V
	or:	$-I_{2;3}$	max.	10	mA
Mode output (pin 4)		$V_{4\text{-}9}$	max.	33	V
		I_4	max.	50	mA
		$-V_{4\text{-}9}$	max.	0,5	V
	or:	$-I_4$	max.	10	mA
Search current/take-over control (pin 5)		$V_{5\text{-}9}$	max.	V_{P1}	V
		$-V_{5\text{-}9}$	max.	0,5	V
	or:	$-I_5$	max.	10	mA
A.F.C. inputs (pins 6 and 7)		$V_{6;7\text{-}9}$	max.	V_{P1}	V
		$\pm I_{6;7}$	max.	2	mA
		$-V_{6;7\text{-}9}$	max.	0,5	V
A.F.C. switch (pin 8)		$V_{8\text{-}9}$	max.	V_{P1}	V
		I_8	max.	2	mA
		$-V_{8\text{-}9}$	max.	0,5	V
	or:	$-I_8$	max.	10	mA
Integrator input (pin 10)		$V_{10\text{-}9}$	max.	5	V
	or:	I_{10}	max.	10	mA
		$-V_{10\text{-}9}$	max.	0,5	V
	or:	$-I_{10}$	max.	10	mA
for $t < 1$ ms		$\pm V_{10\text{-}9}$	max.	30	V
		$\pm I_{10}$	max.	60	mA
Integrator bias (pin 11)		$V_{11\text{-}9}$	max.	10	V
		$-V_{11\text{-}9}$	max.	0,5	V
		$-I_{11}$	max.	5	mA
Band limiting (pin 12)		$V_{12\text{-}9}$	max.	14	V
		$-V_{12\text{-}9}$	max.	0,5	V
		$-I_{12}$	max.	10	mA
Integrator output (pin 13)		$V_{13\text{-}9}$	max.	V_{P2}	V
		$-V_{13\text{-}9}$	max.	0	V

RATINGS (continued)

External tuning (pin 15)	$V_{15\text{-}9}$	max.	V_{P2}	V
	$-V_{15\text{-}9}$	max.	0,5	V
	or: $-I_{15}$	max.	10	mA
Timing (pin 16)	$V_{16\text{-}9}$	max.	V_{P1}	V
	$-V_{16\text{-}9}$	max.	0,5	V
Station select input (pin 18)	$V_{18\text{-}9}$	max.	V_{P1}	V
	$-V_{18\text{-}9}$	max.	0,5	V
	or: $-I_{18}$	max.	10	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80	K/W

CHARACTERISTICS

V_{P1} = 6 to 24 V; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply control section					
Supply voltage range (pin 17)	V_{P1}	6 (5)	–	24	V
Supply current (pin 17) at V_{P1} = 15 V	I_{P1}	–	10	20	mA
Supply tuning section					
Supply voltage range (pin 14)	V_{P2}	6	–	33	V
Supply current (pin 14) at V_{P2} = 30 V; without load at pin 13	I_{P2}	–	1,2	2	mA
Reset circuit (note 1)					
Input control voltage for reset	$V_{18\text{-}9}$	4,5	–	V_{P1}	V
A.F.C. amplifier					
Common-mode input voltage range	$V_{6;7\text{-}9}$	2,5	–	$V_{P1}-1,4$	V
Input bias current	$I_{6;7}$	–	0,2	0,5	μA
Input offset current	$I_{io6;7}$	–	–	0,2	μA
Input resistance	$R_{6\text{-}7}$	1	–	–	MΩ
Maximum a.f.c. output current	$\pm I_{afc10}$	–	$\frac{1}{120} \times I_8$	–	μA
at I_8 = 25 μA	$\pm I_{afc10}$	–	0,21	–	μA
A.F.C. input voltage for $I_{afc10} = 0,7 \times I_{afc10}$	$V_{6\text{-}7}$	–	100	–	mV
A.F.C. control input					
A.F.C. ON:					
permissible input current	I_8	15	–	500	μA
input voltage at I_8 = 25 μA	$V_{8\text{-}9}$	–	$V_{6;7\text{-}9}+0,6$	–	V
A.F.C. OFF (continuous take-over without muting); note 2:					
input voltage	$V_{8\text{-}9}$	0	–	$V_{6;7\text{-}9}$	V
reverse input current; $V_{8\text{-}9}$ = 0 V	$-I_{i8}$	–	–	1	μA

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Integrator amplifier (note 3)					
Required input bias voltage					
pin 11	$V_{11\text{-}9}$	1	–	1,5	V
pin 10	$V_{10\text{-}9}$	–	$V_{11\text{-}9}$	–	V
Input bias currents					
pin 11; at $V_{11\text{-}9} = 1{,}2$ V	I_{11}	–	2	–	μA
pin 10; for search stand-by; A.F.C. OFF	$\pm I_{10}$	–	10	100	nA
Output voltage range with load; $\pm I_{13} = 1{,}2$ mA	$V_{13\text{-}9}$	0,5	–	$V_{14\text{-}9}-1$	V
Available output current ($t < 1$ ms) peak value	$\pm I_{o13m}$	–	10	–	mA
Noise output voltage (peak value) ($f = 20$ Hz to 20 kHz) weighted to DIN45405; $R_L = 1$ kΩ in series with $C_L = 0{,}1$ μF	V_{no13m}	–	5	–	μV
Station search circuit (note 4)					
Start inputs (pins 2 and 3)					
Input bias voltage	V_i	–	$V_{P1}-0{,}2$	–	V
Input threshold voltage for "search start"	V_{is}	$V_{P1}-2{,}3$	$V_{P1}-1{,}8$	$V_{P1}-0{,}8$	V
Input control current for "search start"	$-I_{is}$	0,2	0,5	1	μA
Input short-circuit current					
at $V_{P1} = 20$ V	$-I_{i\,sc}$	–	0,7	–	μA
at $V_{P1} = 6$ V	$-I_{i\,sc}$	–	0,4	–	μA
Required voltage difference for defined direction of search mode	$\pm \Delta V_{2\text{-}3}$	300	–	–	mV

parameter	symbol	min.	typ.	max.	unit
Search-current generator (note 5)					
Permissible input current range	I_5	20	–	200	μA
Input voltage at "search stand-by"	$V_{5\text{-}9}$	–	0,7	–	V
	or:	–	$V_{BE}+R_{i5}\times I_5$	–	V
Input voltage at "search active"	$V_{5\text{-}9}$	–	1,5	–	V
	or:	–	$2V_{BE}+R_{i5}\times I_5$	–	V
Input resistance	R_{i5}	–	2,5	–	kΩ
Output current at pin 10					
at search forward	$\pm I_{sf10}$	$0{,}65I_5$	I_5	$1{,}35I_5$	μA
at search reverse	$\pm I_{sr10}$	–	$I_{sr\,int}+I_{sf10}$	–	μA
	$I_{sr\,int}$	170	330	540	μA
	or:	–	$4V_{BE}/8{,}3$ kΩ	–	mA
Stop-pulse generation (note 6)					
Input threshold levels					
for "stop preparation"	$\pm V_{6\text{-}7}$	100	160	200	mV
for "stop release"; $I_{sf10} = 0$; note 7	$\pm V_{6\text{-}7}$	–	0	30	mV
Stop-criteria (external reset) (note 8)					
Desired tuning position					
from "search start" to "search stop"					
required input voltage	$V_{18\text{-}9}$	0	–	450	mV
or input open circuit	I_{18}	–	–	0,1	μA
Non-desired tuning position					
search re-started					
required input voltage	$V_{18\text{-}9}$	1	–	2,5	V
or input control current	I_{18}	20	–	125	μA
Reset to "search stand-by"					
required input voltage	$V_{18\text{-}9}$	4,5	–	V_{P1}	V
or input control current	I_{18}	0,7	–	–	mA

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Band-limit comparators (note 9)					
Lower-band limit					
Permissible input voltage range	V_{12-9}	–	0,5	$V_{P2}-4$	V
Input current	$-I_{12}$	–	0,5	2	μA
Lower switching threshold level	V_{13-9}	$V_{12-9}+0{,}18$	$V_{12-9}+0{,}2$	$V_{12-9}+0{,}22$	V
Upper-band limit					
Permissible input voltage range	V_{14-9}	6	–	33	V
Upper switching threshold level	V_{13-9}	$V_{P2}-1{,}25$	$V_{P2}-1{,}1$	$V_{P2}-1$	V
Take-over circuit (note 10)					
Take-over start inputs					
Input voltage (note 11)					
for "search stand-by"	V_{5-9}	–	0,7	–	V
for "search active"	V_{5-9}	–	1,5	–	V
Required control voltage for "start take-over"	V_{sto5-9}	–	–	0,35	V
or control current for "start take-over"	I_{sto5}	–	–	1	μA
Continuous take-over e.g. a.f.c. OFF; note 12					
Required control voltage for "continuous take-over"; a.f.c. OFF	V_{8-9}	–	–	$V_{6;\,7-9}$	V
Reverse input current; $V_{8-9} = 0$	$-I_8$	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Take-over comparator					
Input voltage range	$V_{15\text{-}9}$	0,5	–	$V_{P2}-1$	V
Input bias current	$-I_{15}$	–	0,2	1	μA
Input offset voltage $I_{to1} = I_{to2} = 0$ (note 13)	$V_{io15\text{-}13}$	–	3	10	mV
Output current at $\pm V_{13\text{-}15} > 200$ mV					
at "take-over active"	$\pm I_{to1(10)}$	–	500	–	μA
at "continuous take-over"	$\pm I_{to2(10)}$	–	40	–	μA
De-tuning slope at pin 10 for $\pm V_{13\text{-}15} < 50$ mV					
at "take-over active"	S_{to1}	–	4	–	mS
at "continuous take-over"	S_{to2}	–	0,5	–	mS
Threshold voltage for start-timing at "take-over active"	$\pm \Delta V_{13\text{-}15}$	–	50	–	mV
Timing circuit					
Bias voltage	$V_{16\text{-}9}$	–	4,2	–	V
Internal discharge resistance (internally switched)	$R_{i'16\text{-}9}$	0,7	1	1,3	kΩ
Charge current (switched)					
slow	$-I_{16(1)}$	6	9	12	μA
fast	$-I_{16(2)}$	95	150	195	μA
Internal switching thresholds					
lower threshold voltage	$V_{16\text{-}9(1)}$	–	1	–	V
upper threshold voltage	$V_{16\text{-}9(2)}$	–	3,8	–	V
Mute-driver (open collector)					
Output voltage					
LOW level (conducting)		mute active			
HIGH level (non-conducting)		mute in-active			
Output saturation voltage at $I_1 = 2$ mA	$V_{1\text{-}9sat}$	–	–	0,5	V
Output leakage current at $V_{1\text{-}9} = 20$ V	I_1	–	–	10	μA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Mode-driver					
Output voltage					
LOW level (conducting)		search forward or search stand-by mode			
HIGH level (non-conducting)		search reverse mode or take-over active mode or take-over stand-by mode			
Output saturation voltage at I_4 = 25 mA	$V_{4\text{-}9sat}$	–	–	0,8	V
Reverse output current at $V_{4\text{-}9}$ = 20 V	I_4	–	–	1	μA
Switch-on reset (note 14)					
Reset threshold voltage	$V_{17\text{-}9}$	2	–	4	V

Notes to the characteristics

1. The a.f.c. circuit is operational during the "take-over stand-by" mode as well as during the "search stand-by" mode. The latter is set automatically after "search start" and a station is been found (see also note 4).
   In addition, this mode can be selected by activating the reset via pin 18. The "take-over stand-by" mode is set automatically after "start take-over" and an external tuning voltage applied at pin 15 is taken over (see also note 10).
   The a.f.c. output current is controlled to zero by the band limit comparators, when the tuning voltage range limit is reached (see also note 9).
2. The "continuous take-over without muting" mode is only set during a.f.c. OFF, in the "take-over stand-by" mode.
3. The inputs of the integrator amplifier are protected against over-load by internal clamping diodes, enabling a charged storage capacitor to be directly connected.
   Also, the response of the protection circuit will increase the slew-rate of the amplifier, so that the loss of charge when connecting the capacitor is decreased (see Fig. 4).
4. Station search-tuning circuit
   start instruction + (pin 3): the tuning voltage will go positive ($+I_{10}$)
   start instruction – (pin 2): the tuning voltage will go negative ($-I_{10}$).

   The start instruction is internally stored and therefore continuous operation is not necessary. So, the automatically activated variation of the tuning voltage (search) is terminated when the station is found, and a control voltage appears at the a.f.c. inputs (stop-pulse generation).
   This results in analizing the level at pin 18 (station select input for field-strength, stereo, traffic news, TV-carrier etc.) which is controlled by the timing circuit. If $V_{18\text{-}9} < 0{,}45$ V (desired station) the start memory is reset (search stand-by mode) and the tuning voltage will be controlled by the a.f.c. If $V_{18\text{-}9}$ = 1 to 2,5 V (non-desired station) the search-current generator is re-activated, until the next stop pulse appears.

When the tuning voltage range limit is reached (band-limit comparators), a fast "search reverse" follows automatically, during which a "search stop" is impossible. After reaching the other tuning voltage limit, the search is reset in the originally selected direction.

The "take-over active" mode has priority and stops the search tuning. For all the various operation modes, signals are available at the outputs pin 4 (mode display) and pin 1 (muting).
If a start instruction is operated continuously, the circuit operates in a scan-mode, i.e. after having stopped at a desired station a restart appears automatically after about 1,5 seconds.

5. The search tuning speed depends on the value of C_{10-13} and the reference current I_5.
6. The circuit is only active for search forward in the "search active" mode.
7. The signal sequence "search/stop-release" is only possible if before the search-direction choice was made (positive or negative), the threshold voltage for "stop preparation" was passed (see Fig. 8). For more data of pins 6 and 7, see item a.f.c. amplifier.
8. The circuit responds to pin 18 only in the "search active" mode at the end of the analizing time; the timing circuit determines the required analizing time once the "stop-release" threshold is established (see Fig. 8). The circuit responds immediately and independently of the mode to a reset instruction.
9. The circuit limits the tuning voltage at pin 13 to the preset values at pin 12 (lower limit) and pin 14 (upper limit).

   Switching from search forward to reverse and back to forward is obtained automatically during "search active".

   During "a.f.c. ON" the values are limited to those preset (given under item band-limiter comparators).
10. The take-over circuit controls the tuning voltage to a value of an external reference voltage derived from pin 15. There are two operation modes possible.
    a. Tuning by station-selection switches with muting.

       The reference voltage from an external station memory (tuning potentiometer, electronic analogue memory e.g. D/A converter) is applied to pin 15. With the additional start instruction at pin 5 "start take-over" (e.g. mute contact of a tuning potentiometer module) the take-over circuit will be activated. The "start take-over" instruction will be internally stored. The take-over follows as an automatic control process of both the take-over comparator and the timing circuit. After terminating the tuning ($V_{13} = V_{15}$) the circuit returns to the "take-over stand-by" mode ($I_{to1} = I_{to2} = 0$) and the tuning voltage is applied by the a.f.c. circuit. If operation is re-activated from e.g. "search start", the circuit commences its search from the previous set tuning voltage. During changing the tuning voltage the mute output (pin 1) is active.

    b. Manual tuning without muting

       This operation mode is only possible during the "take-over stand-by" mode.
       For manual tuning with the tuning potentiometer it is necessary that the tuning voltage continuously follows the reference voltage at pin 15.
       To achieve this, pin 8 has to be grounded (a.f.c. OFF). The mute output (pin 1) is non-active.
11. See also items under "station search-tuning circuit".
12. For example during manual tuning.
13. I_{to1} is the fast and I_{to2} is the slow take-over current.
14. When the supply voltage V_{P1} (at pin 17) is switched on the circuit is set in the "take-over active" mode. This operation mode corresponds to the instruction "take-over" at pin 5.

DEVELOPMENT SAMPLE DATA

Table 1 Operating modes

ref.	search tuning			take-over		timing			outputs		input	tuning currents (pin 10)					remarks
no.	stand-by	active		stand-by	active	stand-by	active		mode	mute	a.f.c.						
		forward	reverse				0,1 s	1,5 s	pin 4	pin 1	pin 8	I_{afc}	I_{sf}	I_{sr}	I_{tol}	I_{to2}	
1	+					+			0	1	0	0	0	0	0	0	
2	+					+			0	1	1	1	0	0	0	0	● listen
3		+				+			0	0	0	0	1	0	0	0	
4		+				+			0	0	1	1	1	0	0	0	● search tuning
5		+					+		0	0	0	0	0	0	0	0	
6		+					+		0	0	1	1	1	0	0	0	● evaluation
7		+						+	0	1	0	0	0	0	0	0	
8		+						+	0	1	1	1	0	0	0	0	● listen (scan)
9			+			+			1	0	X	0	0	1	0	0	● reverse
10				+		+			1	1	0	0	0	0	1	0	● continuous take-over (no muting) *
11				+		+			1	1	1	1	0	0	0	0	● listen
12					+	+			1	0	X	0	0	0	1	1	take-over (mute)
13					+		+		1	0	0	0	0	0	1	0	
14					+		+		1	0	1	1	0	0	1	0	take-over (mute)

+ corresponds to instantaneous mode of operation

1 = high-ohmic
0 = conducting

0 = current not released
1 = current released
X = don't care

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* For example during manual tuning.

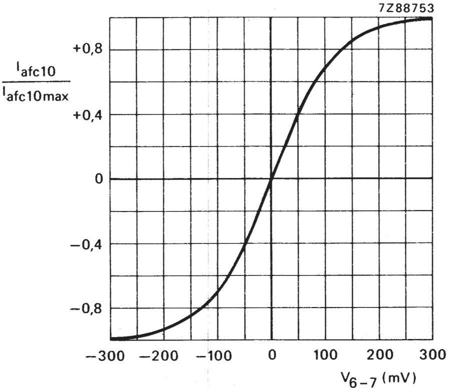


Fig. 2 A.F.C. control curve.

DEVELOPMENT SAMPLE DATA

$$I_{afc10} = \left\{ \frac{2}{e^{-\frac{V_{6\text{-}7}}{2V_T}}+1} \right\} \times \frac{I_8}{120} \qquad I_8 = \frac{V_{P1} - V_{8\text{-}9}}{R_{8\text{-}17} + 10\ \text{k}\Omega}$$

$$V_T = \frac{k \times T}{q} = 28\ \text{mV (at } T_j = 330\ \text{K)}$$

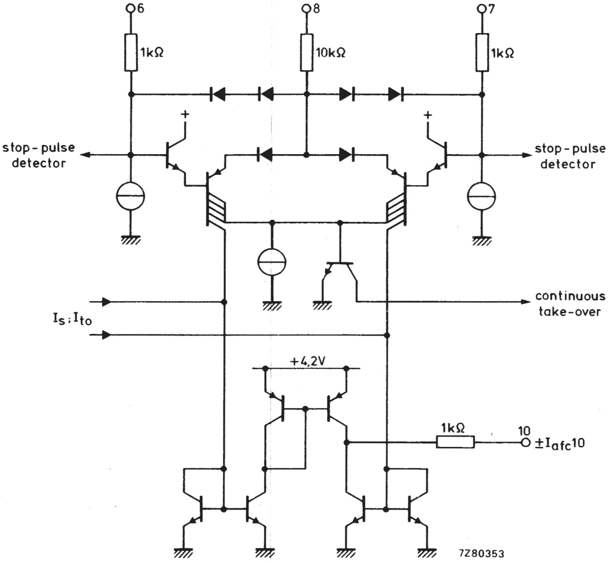

6
8
7
1kΩ
10kΩ
1kΩ
+
+
stop-pulse detector
stop-pulse detector
continuous take-over
I_s; I_{to}
+4,2V
1kΩ
10
$\pm I_{afc10}$
7Z80353

Fig. 3 A.F.C. amplifier (schematic).

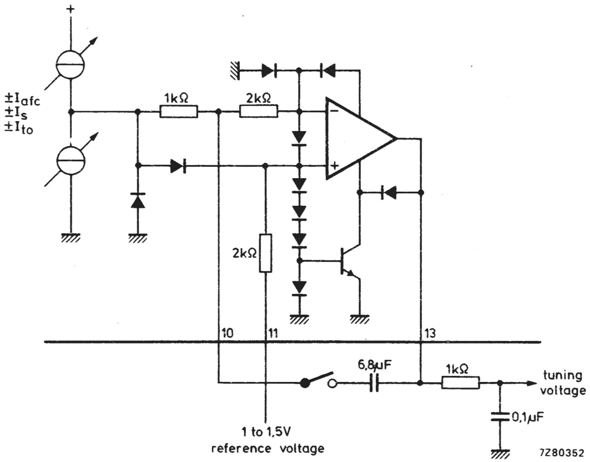
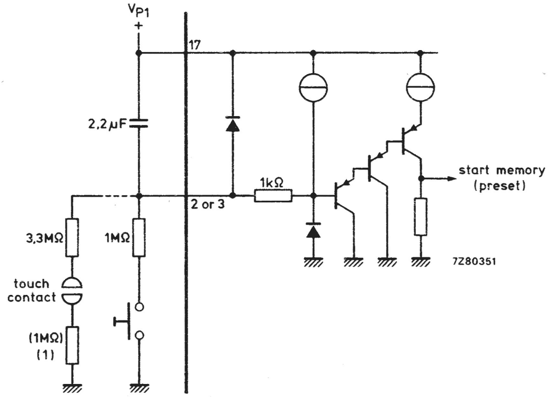

±I_afc
±I_s
±I_to
1kΩ
2kΩ
2kΩ
10
11
13
6,8μF
1kΩ
tuning voltage
0,1μF
1 to 1,5V reference voltage
7Z80352

Fig. 4 Integrator with switch-on clamping circuit (schematic).


V_P1
+
17
2,2μF
1kΩ
2 or 3
3,3MΩ
1MΩ
touch contact
(1MΩ)
(1)
start memory
(preset)
7Z80351

(1) In case the mains supply cannot be disconnected.

Fig. 5 Search-tuning start inputs (schematic).

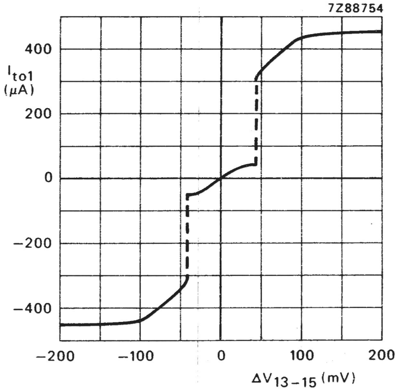


Fig. 6 Take-over current (I_{to10}) as a function of the voltage variation at pin 13 ($\Delta V_{13\text{-}15}$) at tuning to external station memory (external presets).

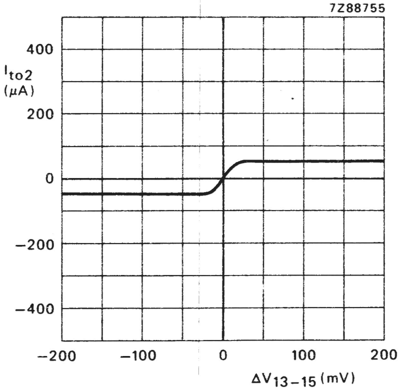
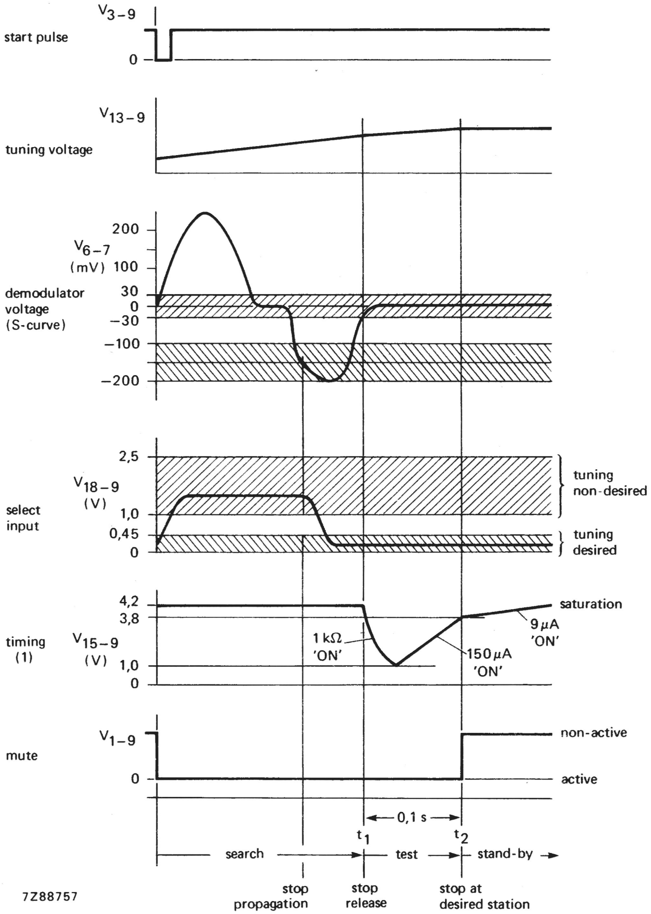


Fig. 7 Take-over current (I_{to10}) as a function of the voltage variation at pin 13 ($\Delta V_{13\text{-}15}$) at continuous take-over (e.g. manual tuning).



(1) The timing is obtained by using the circuit below.

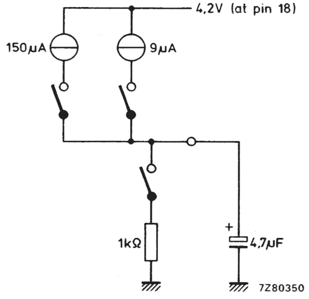

4,2V (at pin 18)
150μA
9μA
1kΩ
+
4,7μF
7Z80350

Fig. 8 Timing diagram for search tuning after "search start" instruction (+).

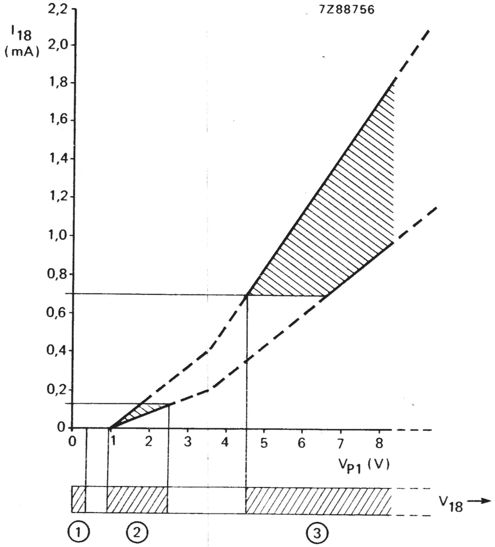
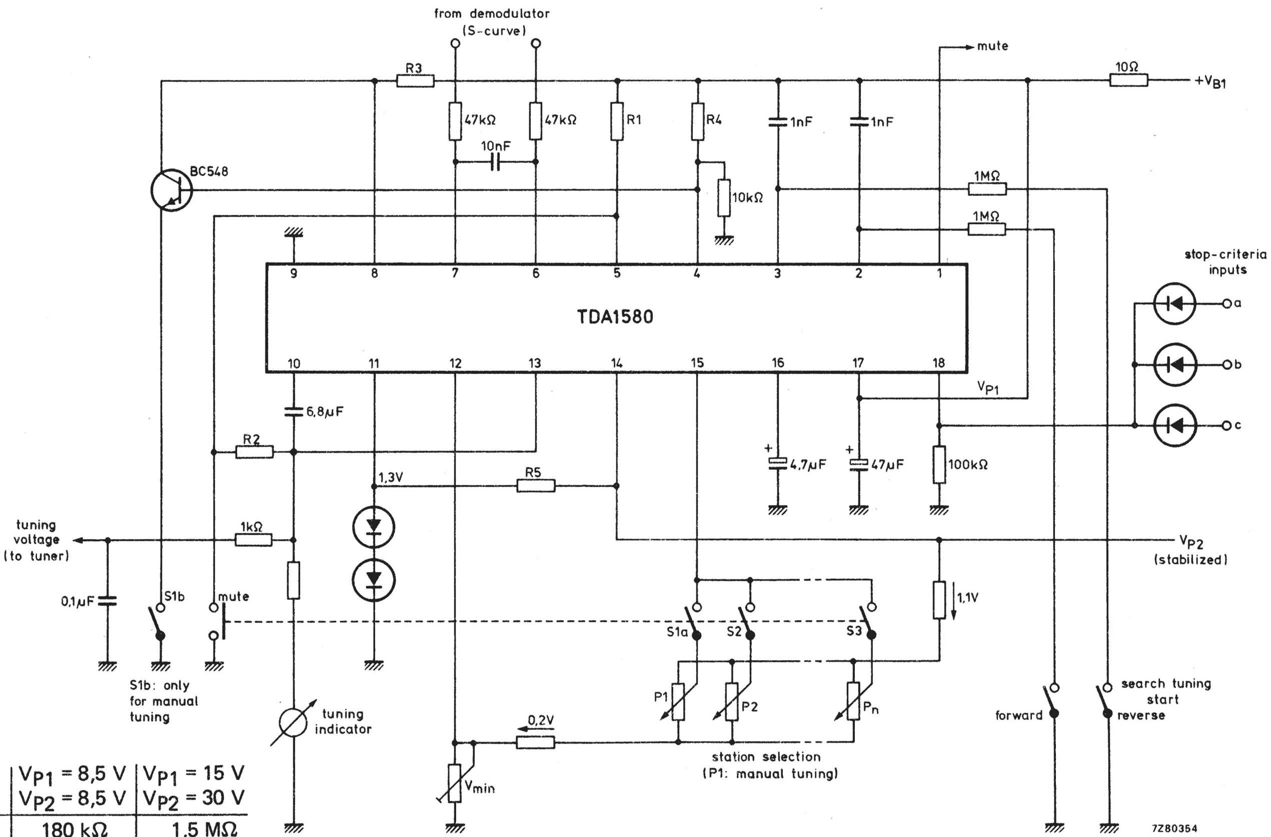


Fig. 9 Stop criteria:

operating range (1) = desired tuning position
operating range (2) = non-desired tuning position
operating range (3) = reset to "search stand-by mode".


from demodulator
(S-curve)
mute
10Ω
+V_{B1}
R3
47kΩ
47kΩ
10nF
R1
R4
10kΩ
1nF
1nF
1MΩ
1MΩ
BC548
stop-criteria
inputs
a
b
c
TDA1580
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
V_{P1}
6,8µF
R2
1,3V
R5
4,7µF
47µF
100kΩ
tuning
voltage
(to tuner)
1kΩ
0,1µF
S1b
mute
V_{P2}
(stabilized)
1,1V
S1a
S2
S3
P1
P2
P_n
S1b: only
for manual
tuning
tuning
indicator
0,2V
V_{min}
station selection
(P1: manual tuning)
forward
search tuning
start
reverse
7Z80354

	V_{P1} = 8,5 V V_{P2} = 8,5 V	V_{P1} = 15 V V_{P2} = 30 V
R1	180 kΩ	1,5 MΩ
R2	82 kΩ	150 kΩ
R3	220 kΩ	390 kΩ
R4	47 kΩ	100 kΩ
R5	68 kΩ	150 kΩ

Fig. 10 Application circuit diagram.

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

MEMORY CONVERTER FOR 4 PRESETS

GENERAL DESCRIPTION

The TDA1584 is a monolithic integrated circuit designed as a memory store for preset tuning positions. Together with the TDA1580 it forms a complete tuning system.

The operation of the TDA1584 memory is based on a 4 x 12-bit data format. The information of 4 preset stations is stored in that memory. The circuit also comprises a 12-bit D/A converter, a 12-bit counter acting as a memory for the last tuned position, two comparators, a voltage-controlled analogue switch and a sequential control logic.

The circuit is capable of digitizing and storing an external d.c. voltage as well as converting stored digital information to a d.c. voltage which is available at output V_{TO} (pin 9).

A built-in adjustable oscillator provides the reference for the correct timing of the internal functions. However, it does not operate continuously.

Features

- Static 12-bit DAC (Digital-to-Analogue Converter)
- 4 presets with 12-bit code available
- Stand-by mode
- A/D conversion of the search tuning voltage and tuning-potentiometer voltage when in the manual mode
- Storage of search and manual tuned voltages
- Automatic a.f.c. selection during the manual tuning mode
- Automatic clamped tuning voltage during reduced signal strength (without a.f.c.)
- Minimal external circuit components required
- Automatic memory set-up when switched-on for the first time (e.g., not from the stand-by position)

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102C).

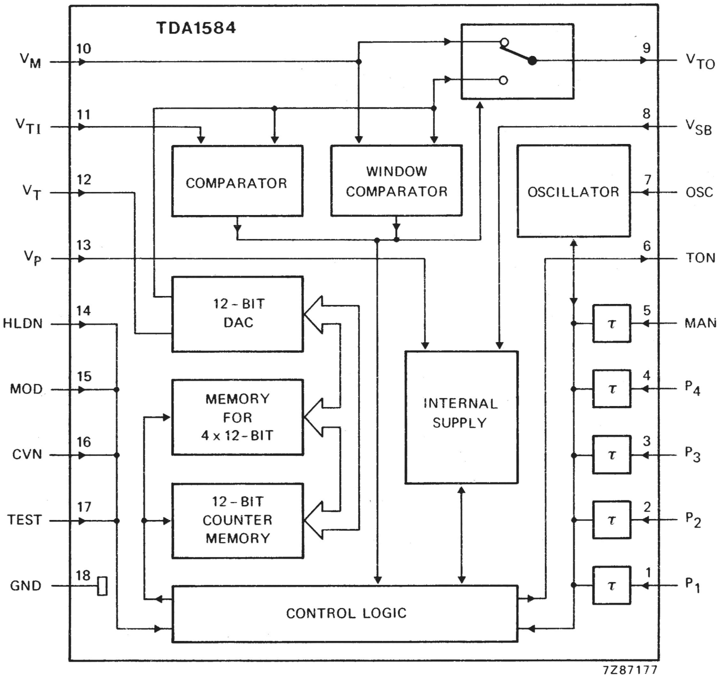

TDA1584
V_M 10
V_TI 11
V_T 12
V_P 13
HLDN 14
MOD 15
CVN 16
TEST 17
GND 18
9 V_TO
8 V_SB
7 OSC
6 TON
5 MAN
4 P_4
3 P_3
2 P_2
1 P_1
COMPARATOR
WINDOW COMPARATOR
OSCILLATOR
12-BIT DAC
MEMORY FOR 4 x 12-BIT
12-BIT COUNTER MEMORY
INTERNAL SUPPLY
CONTROL LOGIC
τ
7Z87177

Fig. 1 Block diagram.

PINNING

1	P_1	preset 1 input
2	P_2	preset 2 input
3	P_3	preset 3 input
4	P_4	preset 4 input
5	MAN	manual tuning input
6	TON	take-over output
7	OSC	oscillator input
8	V_{SB}	stand-by supply
9	V_{TO}	tuning voltage output
10	V_M	tuning voltage manual
11	V_{TI}	tuning voltage input
12	V_T	tuning voltage supply
13	V_P	main supply
14	HLDN	hold input
15	MOD	mode input
16	CVN	converter input
17	TEST	test input
18	GND	ground

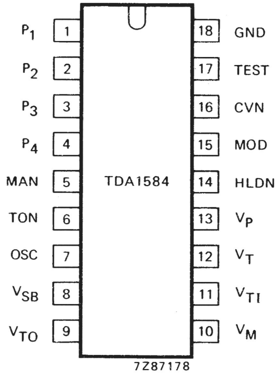

P_1 1
P_2 2
P_3 3
P_4 4
MAN 5
TON 6
OSC 7
V_SB 8
V_TO 9
18 GND
17 TEST
16 CVN
15 MOD
14 HLDN
13 V_P
12 V_T
11 V_TI
10 V_M
TDA1584
7Z87178

Fig. 2 Pinning diagram.

FUNCTIONAL DESCRIPTION

The functions are described for the combination of the TDA1584 and TDA1580 tuning system as given in Fig. 6.

Stand-by mode

Two modes of operation are possible:

1. OFF-STAND-BY
   The receiver is switched-off and a voltage is applied only to V_{SB} (pin 8). The digital section of the IC remains operational, but all the inputs are inactive and the outputs are in a high-impedance state. The digital section only draws current.
2. MW-STAND-BY
   The receiver is set to the medium-wave band. Voltage will be applied to V_{SB} (pin 8), V_T (pin 12) and V_M (pin 10). Furthermore, the IC behaves as for the OFF stand-by mode.

Switch-on operation

It is necessary to apply the required voltage at V_{SB} (pin 8). When the IC supply voltage is applied to V_P the circuit is activated and the operation process is initialized automatically. Before switching off, the active tuning voltage is available at V_{TO} (pin 9) via the D/A converter. That is the tuning voltage representing the previous tuned station which was stored by station preset or detected by search tuning. If the TDA1584 was in the manual mode before switching off or band-switching, then it will remain in the same mode when it is switched on again or band-switched from the AM mode. The result is that the voltage at the tuning-potentiometer slider will be fed to V_M (pin 10). The D/A converter performs the function of a switched-voltage divider, thus the output voltage at V_{TO} (pin 9) depends on the magnitude and stability of the voltage applied to V_T (pin 12; tuning supply voltage).

When used in combination with the TDA1580 (automatic tuning circuit), this circuit utilizes the tuning voltage at V_{TO} to process its switch-on routine and reacts immediately with a mute-control signal. The TDA1584 is set to the stand-by-mode, where the internal oscillator is disabled and the voltage at V_{TO} remains constant.

When the TDA1584 is switched on for the first time (not from the stand-by mode), all the memory locations are loaded with a value corresponding to approximately half the voltage of V_T ($V_T/2$). It is therefore ensured that the receiver is only tuned to an acceptable part of the tuning range.

The start-up of the stand-by supply voltage at V_{SB} (pin 8) must follow a minimum time constant to enable an undisturbed return to the reset routine.

Station selection

A station is selected by operating one of the preset push-buttons at P1 to P4 (pins 1 to 4). After a debounce time, the appropriate memory location is addressed, read and D/A converted, and it is available at V_{TO} (pin 9) as a tuning voltage. The circuit generates a pulse at TON (pin 6) for enabling the TDA1580 to react on the tuning voltage at V_{TO}. If the preset push-button is not further activated, the TDA1584 returns to its stand-by mode.

Search-tuning mode

When the search-tuning function is initialized, the inputs CVN (pin 16; convert not) and MOD (pin 15; search mode) will be controlled by the TDA1580 and their state will be LOW. In this state the TDA1584 waits until CVN goes HIGH again (meanwhile the search function is disabled). The 12-bit counter then is set to zero and it will count upwards in steps, such that the voltage at the D/A converter output increases from zero level upwards. A comparator compares this voltage with that at V_{TI} (from TDA1580 pin 13; tuning output voltage) and when equal, the polarity of the comparator output changes and the counter/memory stops. The digital count information now corresponds to the actual tuning voltage. After that, the TDA1584 returns to the stand-by mode.

FUNCTIONAL DESCRIPTION (continued)

Storing of preset stations

Storing a preset station requires a depression of the station select push-button of at least 2,5 s. The initial presetting is described in "station selection". If the push-button is still activated after 2,5 s, another pulse is generated at TON (pin 6), which causes the TDA1580 to generate a mute signal and to take over the control of the available tuning voltage from the TDA1584. The counter/memory content now appears at the D/A converter output and the digital information corresponding to the tuning voltage is written into the appropriate memory position simultaneously.

After the push-button is released the circuit returns to the stand-by mode. A priority control function ensures that only one push-button depression for presetting can be operated at a time.

Manual tuning

The TDA1584 is switched to the manual tuning mode by depressing the push-button connected to MAN (pin 5). The built-in analogue voltage switch switches the output V_{TO} from the D/A converter output to the input V_M (pin 10), at which the potentiometer-slider voltage is applied. With this voltage at V_{TO} (now equivalent to the voltage at V_M) search tuning can be taken over by the TDA1580 and a LOW-level pulse at output TON (pin 6) is generated. At the same time the output HLDN (pin 14; hold not) goes LOW. The result is that search tuning circuit TDA1580 goes into the continuous take-over mode, e.g. it follows the voltage at V_M without activating the mute control signal. If the tuning potentiometer is no longer activated, it is necessary to activate the a.f.c. of the TDA1580. Consequently the TDA1584 requires further control (see Fig. 6).

Input V_M controls the analogue switch and one input of the window comparator simultaneously. The other window-comparator input is connected to the D/A converter output which, when in the manual tuning mode, is under constant control of the counter. The counter counts up until the comparator detects equal voltage levels at the inputs and it stops the counter/memory. If the voltage at V_M changes as a result of further tuning potentiometer adjustment, then the window comparator switches back again and the counter continues upwards counting. If no voltage equality is detected, the counter counts up to its maximum value and then returns to zero, from which it starts counting up again until voltage equality is detected. Further on, after voltage equality detection, output HLDN goes into the high-impedance state for about 1 s. As a result of this the tuning voltage of the TDA1580 is disconnected from V_{TO} (pin 9) and the search tuning a.f.c. is activated. After the necessary operation delays the TDA1584 returns to the stand-by mode.

Drop-out of the (field strength) input signal

HLDN (pin 14) has two functions. It operates as an output to switch the a.f.c. at pin 8 of the TDA1580 during manual tuning (see "manual tuning" above). When operating in the search-tuning mode HLDN acts as an input. In this mode it reacts to a switching signal which is derived from the field strength dependent input signal. If the system is tuned to a station by search tuning, then the HLDN input voltage is HIGH. If the signal strength drops (e.g. by driving through a tunnel), then HLDN goes LOW. The next processing step is similar to the one described in "switch-on operation", that is, the search-tuning circuit (TDA1580) takes over the voltage at V_{TO}. However, it goes into the continuous take-over mode so that the tuning voltage is clamped constantly at the output of the D/A converter without a.f.c. and the tuning voltage cannot drift because its a.f.c. input (pin 8) is also grounded. When the signal strength returns, the a.f.c. input is released at the TDA1580 tuning circuit and the system automatically locks onto the zero-crossing of the demodulator S-curve.

During repetitive signal strength drop-out, the TDA1584 generates no control instructions, because the search-tuning circuit is in the take-over mode.

CHARACTERISTICS

Measured in the tuning system TDA1584 and TDA1580 (Fig. 6)

parameter	symbol	min.	typ.	max.	unit
Ambient temperature range	T_{amb}	−30	–	+80	°C
DIGITAL SECTION					
Supply 1 (pin 8)					
Supply voltage	V_{SB}	6	14	24	V
Supply current	I_{SB}	–	1,5	3	mA
Stand-by supply voltage range	V_{SB}	3	–	24	V
Stand-by supply current	I_{SB}	–	1,5	3	mA
Response at switch-on			see Fig. 3		
Response at switch-off			see Fig. 4		
Permissible slope of V_{SB} at switch-on (rise time)	t_r	–	–	10	mV/μs
Supply 2 (pin 13)					
Supply voltage	V_P	6	14	24	V
Supply current	I_P	–	6	10	mA
Oscillator (pin 7)					
Frequency with external components: R = 100 kΩ; C = 370 pF	f_{osc}	–	25	–	kHz
Frequency stability throughout supply and temperature ranges	Δf_{osc}	–	± 15	–	%
Inputs P_1 to P_4 and MAN (pins 1 to 4 and 5)					
Input voltage HIGH (stand-by or open circuit)	V_{IH}	3,5	–	V_P	V
or: current HIGH	$-I_{IH}$	–	–	5	μA
Input voltage LOW (active)	V_{IL}	0	–	1,5	V
or: current LOW	$-I_{IL}$	100	200	1000	μA
Inputs CVN and MOD (pins 16, 15)					
Input voltage HIGH	V_{IH}	3,5	–	V_P	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input current HIGH	I_{IL}	–	–	0,5	μA
Input current LOW	$-I_{IL}$	–	–	10	μA
Pin HLDN as input (pin 14) at HLDN output HIGH					
Input voltage HIGH	V_{IH}	1,8	–	V_P	V
Input voltage LOW	V_{IL}	0	–	0,7	V
Input current HIGH	I_{IH}	–	–	1	μA
Input current LOW	$-I_{IL}$	–	–	10	μA

CHARACTERISTICS continued)

parameter	symbol	min.	typ.	max.	unit
Pin HLDN as output (pin 14)					
Output voltage HIGH permissible reverse voltage; open-collector	V_{OH}	–	–	V_P	V
Output voltage LOW at 1 mA	V_{OL}	–	–	0,5	V
Output TON (pin 6)					
Output voltage HIGH permissible reverse voltage; open-collector	V_{OH}	–	–	V_P	V
Output voltage LOW at 200 μA	V_{OL}	–	–	0,3	V
Output leakage current	$\pm I_{LC}$	–	–	1	μA
Delays for					
station presetting at f_{osc} = 25 kHz	t_d	–	2,6	–	s
HLDN output LOW (a.f.c. on)	t_d	–	1,3	–	s
Debounce time (push-button switch)	t_{deb}	–	41	–	ms
ANALOGUE SECTION					
Tuning voltages (pins 9, 10, 11 and 12)					
Supply voltage (pin 12)	V_T	6	–	V_P	V
Input voltage range (pin 11)	V_{TImin}	–	–	0,5	V
	V_{TImax}	V_T-1	–	–	V
Input voltage range (pin 10)	V_{Mmin}	–	–	0,5	V
	V_{Mmax}	V_T-1	–	–	V
Input current (pins 10 and 11)	$-I_I$	–	0,2	1	μA
Output voltage range (pin 9)	V_{TOmin}	–	–	0,5	V
	V_{TOmax}	V_T-1	–	–	V
Output resistance of the analogue switch (pin 9) at I_o = 100 μA)	R_o	–	300	–	Ω
Output current (pin 9)	$\pm I_o$	100	–	–	μA
Offset voltage: $\pm\Delta$ $(V_M - V_{TO})$	V_{IO}	–	–	10	mV
Resolution voltage of the A/D – D/A converter: $\Delta(V_{TO}-V_{TI})$ in the range V_{TO} = 0,5 to V_T-1 V	V_{res}	–	–	7	mV
Maximum conversion time for $V_{TO} = V_T-1$ V; f_{osc} = 25 kHz	t_{con}	–	165	–	ms
Variation of V_{TO} with temperature at V_T constant			see Fig. 5		

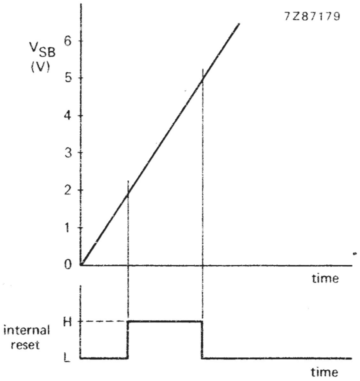


Fig. 3 Response at switch-on.

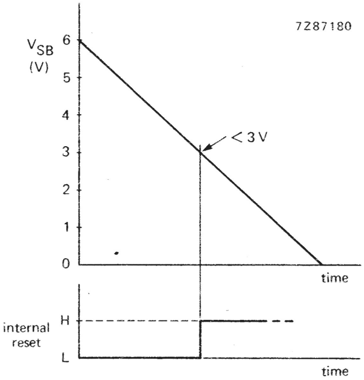


Fig. 4 Response at switch-off.

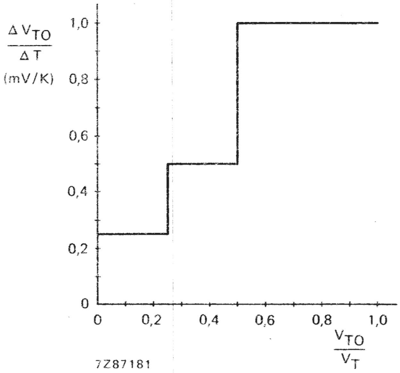


Fig. 5 Variation of V_{TO} with temperature at V_T constant.

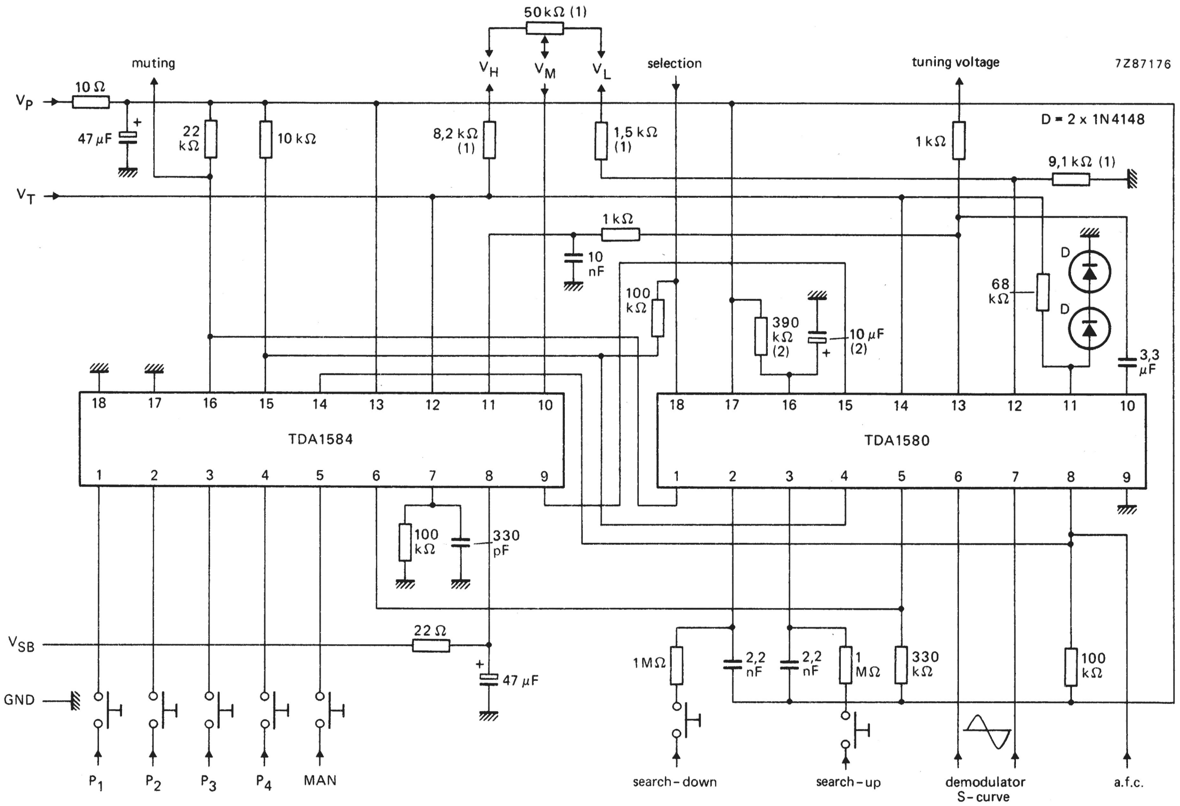

7Z87176
D = 2 x 1N4148
V_P
V_T
V_SB
GND
10 Ω
47 µF
muting
22 kΩ
10 kΩ
50 kΩ (1)
V_H
V_M
V_L
8,2 kΩ (1)
1,5 kΩ (1)
selection
tuning voltage
1 kΩ
9,1 kΩ (1)
1 kΩ
10 nF
100 kΩ
390 kΩ (2)
10 µF (2)
68 kΩ
D
D
3,3 µF
TDA1584
TDA1580
100 kΩ
330 pF
22 Ω
47 µF
1 MΩ
2,2 nF
2,2 nF
1 MΩ
330 kΩ
100 kΩ
P1
P2
P3
P4
MAN
search-down
search-up
demodulator S-curve
a.f.c.

Fig. 6 Application circuit diagram using the TDA1584 and TDA1580 as a complete tuning system; also used as test circuit for the characteristics; the functional description is based on this circuit.

(1) The component values are matched to the required tuning voltage of the FM front-end.

(2) Test time for selection criteria:

time	R	C
100 ms	—	4,7 µF
200 ms	390 kΩ	10 µF
350 ms	180 kΩ	22 µF

DISPLAY/DRIVER CIRCUIT FOR 11 LEDs

The TDA1594 is a monolithic integrated circuit intended to drive 11 LEDs for analogue signal display. Two display modes are possible: as a pointer (only one LED on) or as a bar (a row of LEDs on).

The circuit contains the following functions:

- A/D converter with S-shaped pre-compensated control curve.
- Current control of LED with separate selectable bias current for the display limits.
- External brightness control; e.g. by an LDR (Light Dependent Resistor).
- External adjustable brightness take-over of the display segments.
- High-ohmic control input; diode protected.
- Internal reference voltage (proportional to V_T).

QUICK REFERENCE DATA

Supply voltage range (pin 12)	V_P		7,5 to 23	V
Supply current (pin 12)	I_P	typ.	6	mA
Control voltage range	$\pm V_C$	typ.	100	mV
Reference input voltage range	V_I		2 to $V_P - 4$	V
Adjustable output current	I_O		0 to 25	mA
Output reverse voltage	V_{OR}	typ.	25	V
Output saturation voltage	V_{Osat}	<	2,5	V
Ambient temperature range	T_{amb}		−30 to +80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102C).

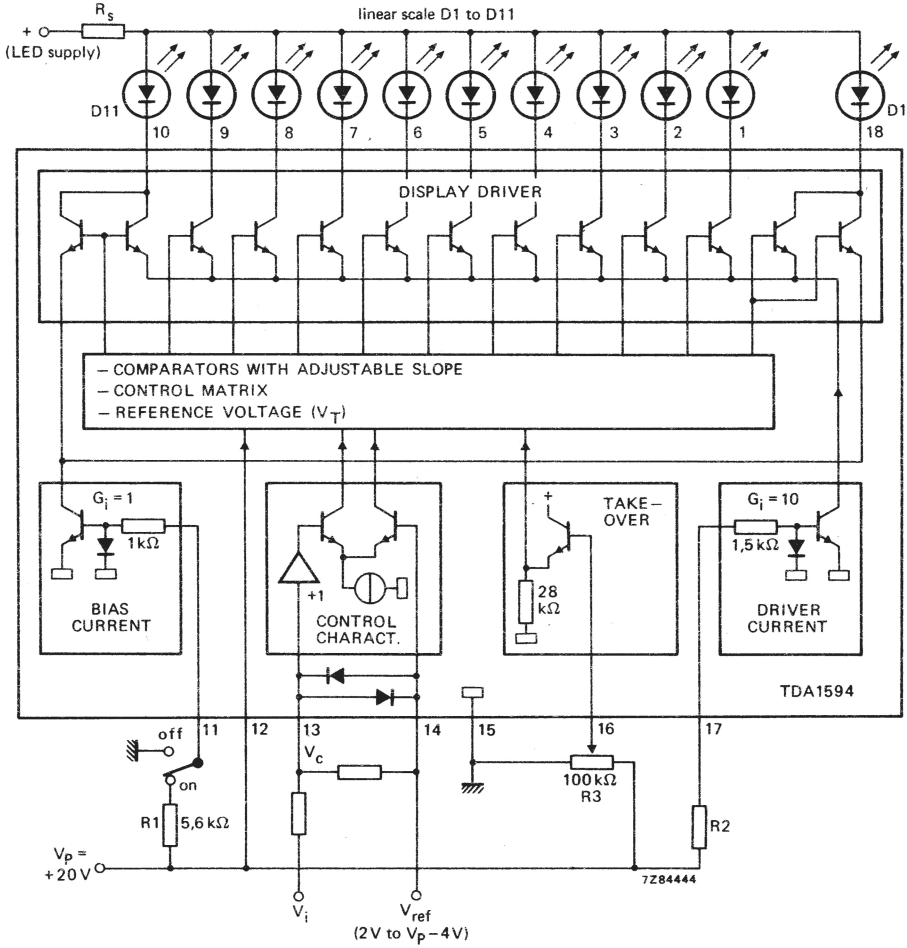

R_s
linear scale D1 to D11
+
(LED supply)
D11
D1
10
9
8
7
6
5
4
3
2
1
18
DISPLAY DRIVER
– COMPARATORS WITH ADJUSTABLE SLOPE
– CONTROL MATRIX
– REFERENCE VOLTAGE (V_T)
G_i = 1
1 kΩ
BIAS CURRENT
+1
CONTROL CHARACT.
+
TAKE-OVER
28 kΩ
G_i = 10
1,5 kΩ
DRIVER CURRENT
TDA1594
off
on
11
12
13
14
15
16
17
V_c
R1
5,6 kΩ
100 kΩ
R3
R2
V_P = +20 V
V_i
V_ref
(2 V to V_P – 4 V)
7Z84444

Fig. 1 Block diagram and external components.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 12)	V_P	max.	23	V
Control voltages (V_c)	$V_{13\text{-}15}$, $V_{14\text{-}15}$	max.	V_P	V
	$-V_{13\text{-}15}$, $-V_{14\text{-}15}$	max.	0	V
	$\pm V_{13\text{-}14}$	max.	0,5	V
	or: $\pm I_{13}$, $\pm I_{14}$	max.	2	mA
Control voltages for display currents	$V_{11\text{-}15}$, $V_{17\text{-}15}$	max.	23	V
Control voltage for transfer	$V_{16\text{-}15}$	max.	V_P	V
Output voltage pins 1 to 10, and 18	V_O	max.	28	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−55 to +150	°C
Operating ambient temperature	T_{amb}		−30 to +80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80	K/W

CHARACTERISTICS at T_{amb} = 25 °C

Supply voltage range (pin 12)	$V_P = V_{12\text{-}15}$		7,5 to 23	V
Supply current				
at $V_{16\text{-}15} = 0$	$I_P = I_{12}$	typ.	4	mA
			2,5 to 5,5	mA
at $V_{16\text{-}15} = V_{12\text{-}15} = 20$ V	$I_P = I_{12}$	typ.	6,5	mA

The following characteristics are measured at V_P = 20 V; T_{amb} = 25 °C unless otherwise specified.

Control inputs

Reference input voltage range				
at $V_{16\text{-}15} = 0$ (smooth take-over)	$V_{13\text{-}15} = V_{14\text{-}15}$	typ.	2 to $V_P - 2$	V
at $V_{16\text{-}15} = V_{12\text{-}15} = 20$ V (switching)	$V_{13\text{-}15} = V_{14\text{-}15}$	typ.	2 to $V_P - 4$	V
Allowable control voltage range	$\pm V_{13\text{-}14}$	typ.	400	mV
Input quiescent current				
at $V_{16\text{-}15} = 0$	$\pm I_{13}$	<	0,1	μA
	I_{14}	typ.	2	μA
		<	3	μA
at $V_{16\text{-}15} = V_{12\text{-}15} = 20$ V	$\pm I_{13}$	<	0,4	μA
	I_{14}	typ.	10	μA
		<	15	μA

CHARACTERISTICS (continued)

Control voltage $V_{13\text{-}14}$ * (input voltages for equal currents at two display driver outputs at $I_{11} = 0$)				
at $I_{18} = I_1$	$-V_c$	typ.	70	mV
			60 to 80	mV
at $I_1 = I_2$	$-V_c$	typ.	48	mV
at $I_2 = I_3$	$-V_c$	typ.	32	mV
at $I_3 = I_4$	$-V_c$	typ.	19,5	mV
at $I_4 = I_5$	$-V_c$	typ.	8	mV
			5 to 11	mV
at $I_5 = I_6$	V_c	typ.	8	mV
			5 to 11	mV
at $I_6 = I_7$	V_c	typ.	19,5	mV
at $I_7 = I_8$	V_c	typ.	32	mV
at $I_8 = I_9$	V_c	typ.	48	mV
at $I_9 = I_{10}$	V_c	typ.	70	mV
			60 to 80	mV
Control voltage for the zero-point display; $V_{16\text{-}15} = 0$ (smooth take-over)				
V_{c5} at $I_{\text{diode }5} = -40$ dB V_{c7} at $I_{\text{diode }7} = -40$ dB	$\Delta V_c = \frac{V_{c7} - V_{c5}}{2}$	>	3	
		typ.	5	

Take-over characteristic

Control voltage range	$V_{16\text{-}15}$		0 to V_P	V
Control voltage (see Figs 3 and 4)				
for smooth take-over	$V_{16\text{-}15}$	typ.	0	
for switched take-over	$V_{16\text{-}15}$	typ.	20	V
		<	V_P	V
Input resistance (pin 16)	R_{i16}	typ.	1	MΩ
Current ratio of adjacent driver outputs at $V_{16\text{-}15} = 0$ (smooth take-over) $I_{11} = 0$; V_c = constant	$\frac{I_n \pm 1}{I_n}$	>	−34	dB
at $V_P = 20$ V (switching); $I_{11} = 0$; $I_n = 30$ mA	$\frac{I_n \pm 1}{I_n}$	>	−70	dB

---

* Proportional to $V_T = \frac{k \cdot T}{q}$.

DEVELOPMENT SAMPLE DATA

Display driver (pins 1 to 10 and 18)				
Output current; adjustable at pin 17	I_O		0 to 30	mA
Saturation voltage at the outputs at $I_O = 25$ mA	V_{Osat}	typ.	2,0	V
		<	2,5	V
Reverse voltage at the outputs at $I_{OR} < 10\ \mu A$	V_{OR}	>	25	V
Driver current adjustment (pin 17)				
Input reference current	I_{17}		0 to 3	mA
Current gain (I_O/I_{17})	G_i	typ.	9,5	
			8 to 11	
Adjustment voltage at $I_O < 10\ \mu A$ (dark)	V_{17-15}	<	0,35	V
at $I_{17} = 2,5$ mA	V_{17-15}	typ.	4,5	V
			3,5 to 5,5	V
Bias current adjustment (pin 11)				
(bias current for optical indication of display limits)				
Output current (adjustable)	I_{10}, I_{18}		0 to 4	mA
Current gain at $I_{11} = 2,5$ mA	G_i	typ.	1,2	
Adjustment voltage at I_{10}, $I_{18} < 10\ \mu A$	V_{11-15}	<	0,35	V
at $I_{11} = 2,5$ mA	V_{11-15}	typ.	3,1	V
			2,2 to 3,5	V

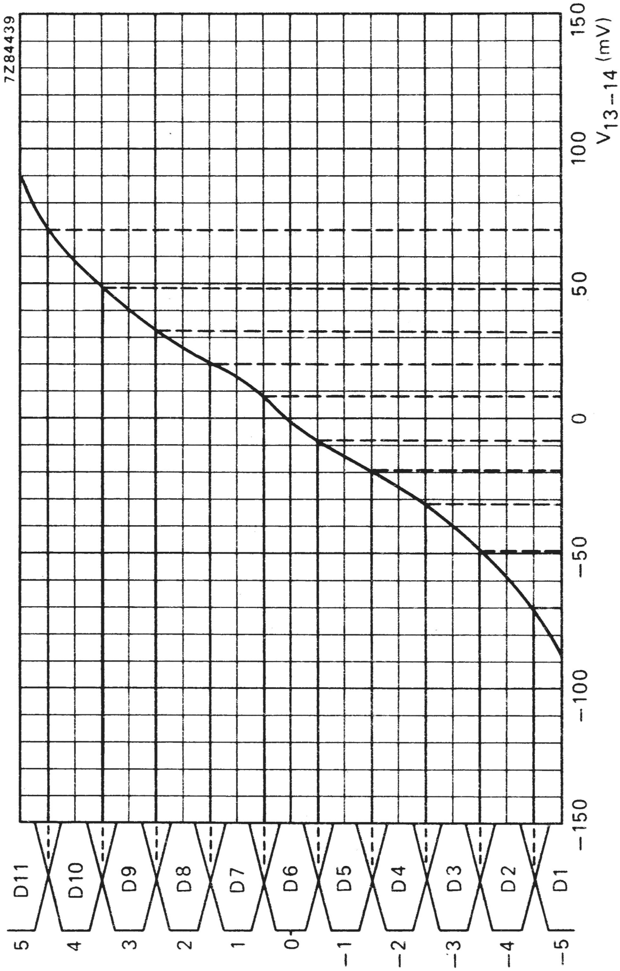


Fig. 2 Control curve.

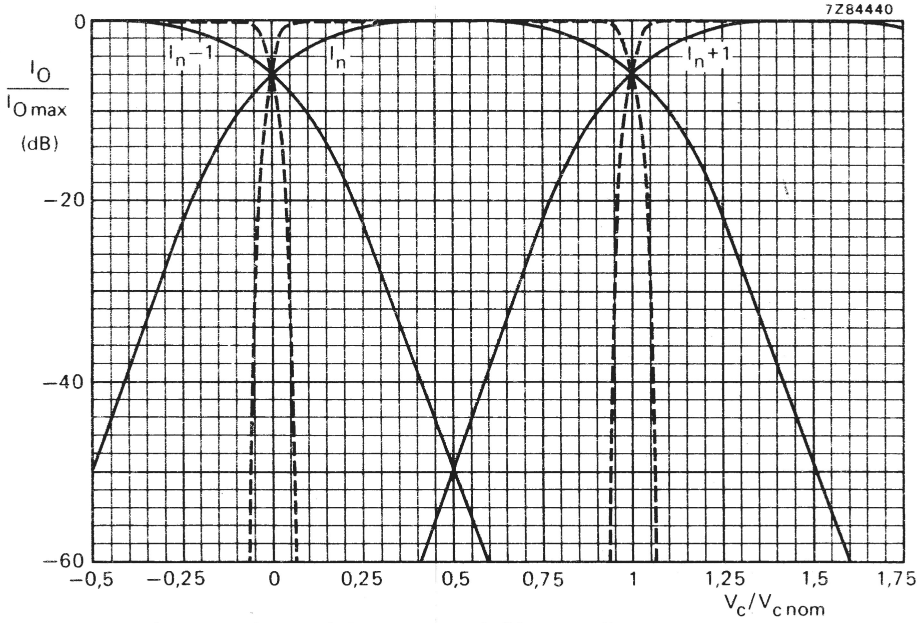


Fig. 3 Display/take-over characteristic; —— smooth ($V_{16\text{-}15} = 0$); - - - - switching ($V_{16\text{-}15} = 20$ V).

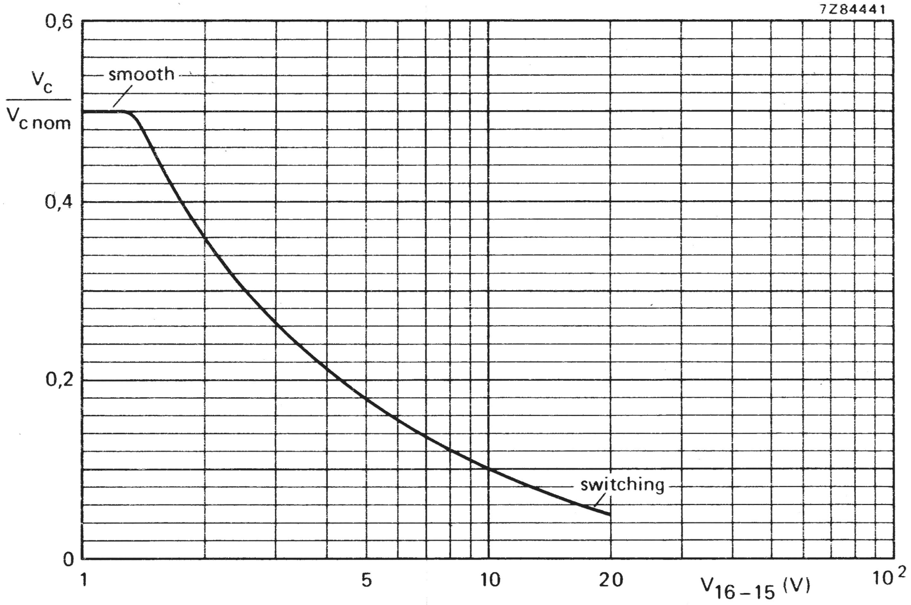


Fig. 4 Adjustment of the display/take-over characteristic; $V_c/V_{c\,nom}$ for $I_O/I_{O\,max}$ is −6 dB to −50 dB.

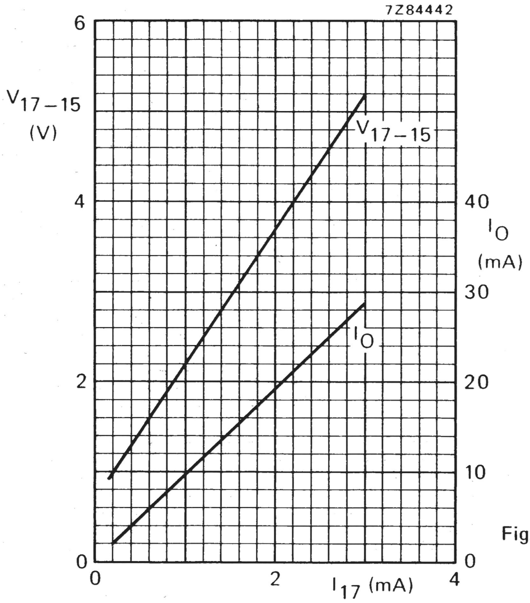


Fig. 5 Display current adjustment.

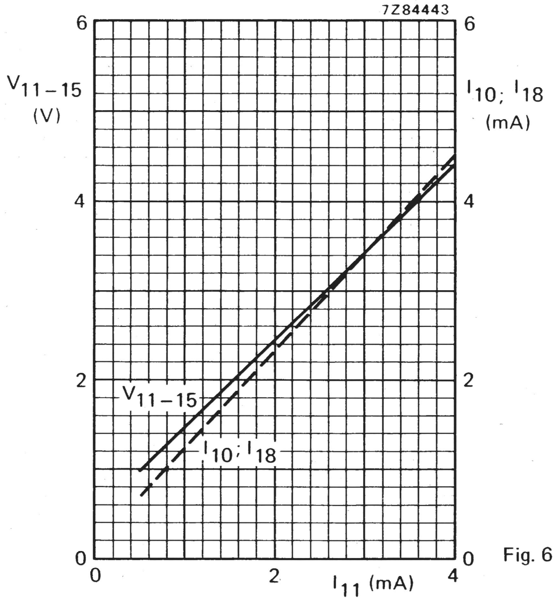
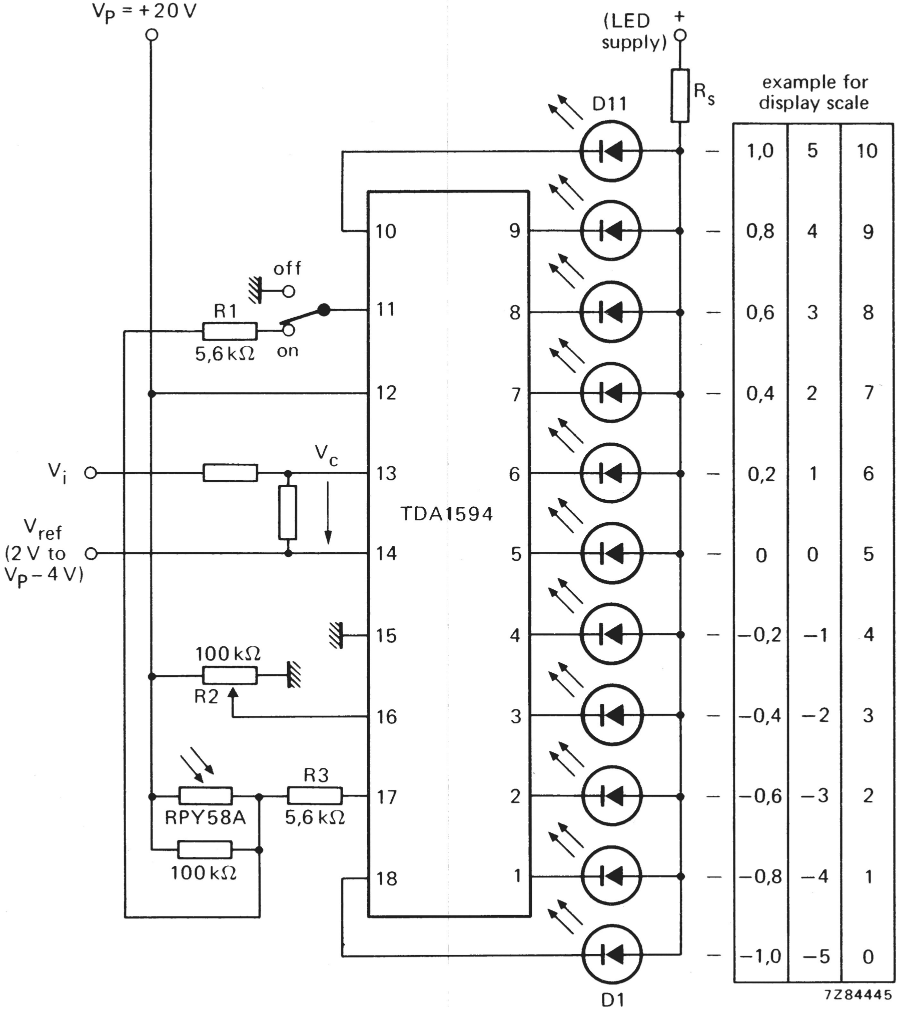


Fig. 6 Bias current adjustment.

APPLICATION INFORMATION


$V_P = +20\,V$
(LED supply)
+
R_s
D11
D1
TDA1594
10
11
12
13
14
15
16
17
18
9
8
7
6
5
4
3
2
1
off
on
R1
5,6 kΩ
V_i
V_c
V_{ref} (2 V to $V_P - 4\,V$)
100 kΩ
R2
RPY58A
R3
5,6 kΩ
100 kΩ
example for display scale
7Z84445

1,0	5	10
0,8	4	9
0,6	3	8
0,4	2	7
0,2	1	6
0	0	5
−0,2	−1	4
−0,4	−2	3
−0,6	−3	2
−0,8	−4	1
−1,0	−5	0

Fig. 7 The TDA1594 used as a pointer (only one LEDs on at a time).

Notes to Fig. 7.

1. Two or more outputs can be connected in parallel to drive a LED when less than 11 LEDs are driven.
2. It is possible to use different coloured LEDs in a bar.

APPLICATION INFORMATION (continued)

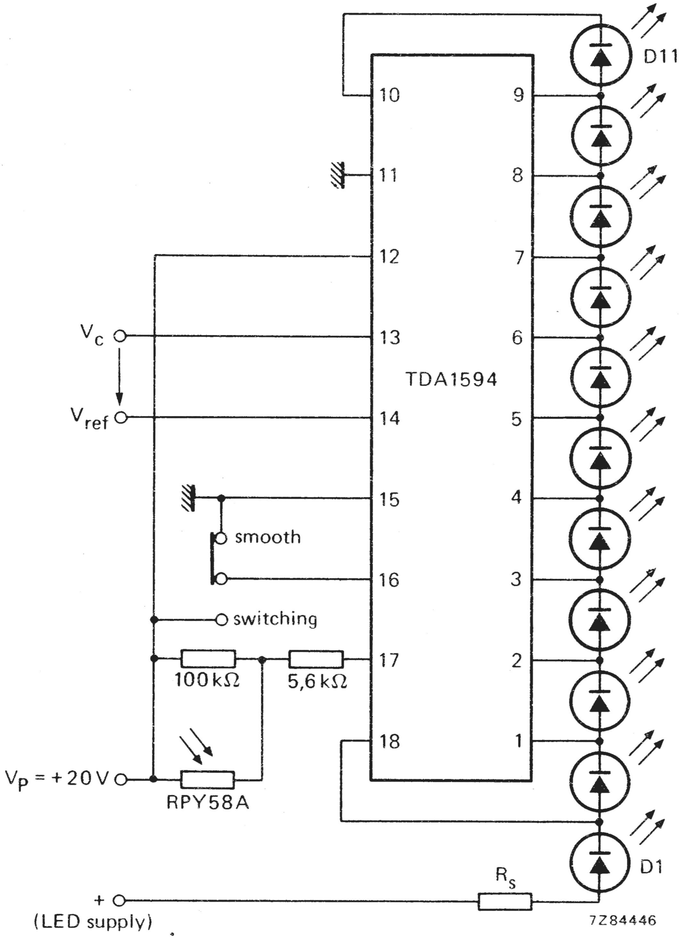

D11
10
9
11
8
12
7
V_c
13
6
TDA1594
V_{ref}
14
5
15
4
smooth
16
3
switching
17
2
100 kΩ
5,6 kΩ
18
1
V_P = +20 V
RPY58A
D1
R_s
+
(LED supply)
7Z84446

Fig. 8 The TDA1594 used as a bar display (a row of LEDs on).

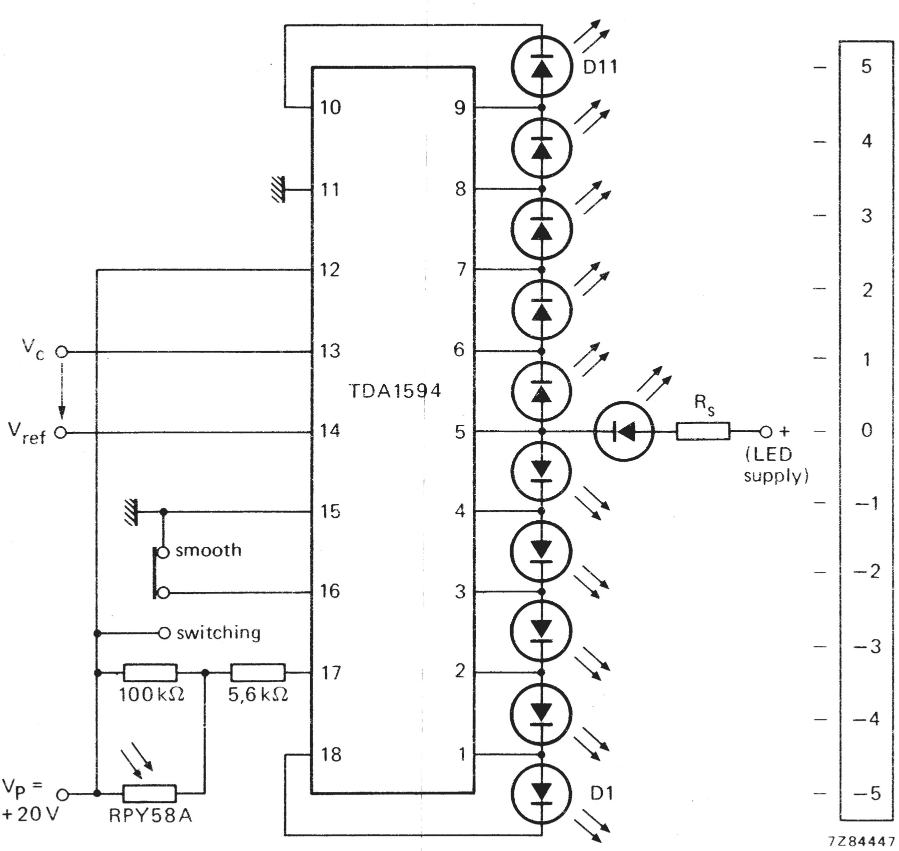

D11
D1
10
11
12
13
14
15
16
17
18
9
8
7
6
5
4
3
2
1
TDA1594
V_c
V_{ref}
smooth
switching
100 kΩ
5,6 kΩ
V_P =
+20 V
RPY58A
R_s
+
(LED
supply)
5
4
3
2
1
0
−1
−2
−3
−4
−5
7Z84447

Fig. 9 The TDA1594 used as a positive/negative bar display.

APPLICATION INFORMATION (continued)

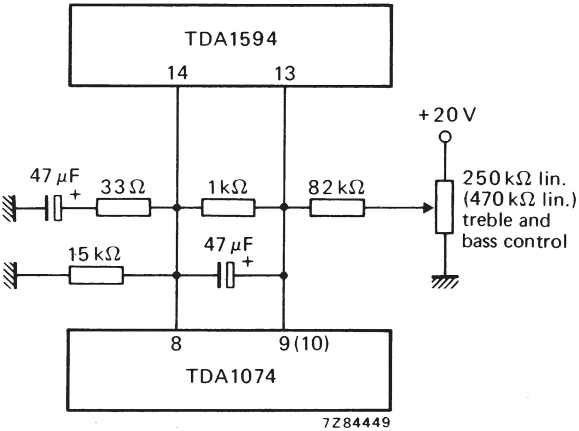

TDA1594
14
13
+20 V
47 μF
+
33 Ω
1 kΩ
82 kΩ
250 kΩ lin.
(470 kΩ lin.)
treble and
bass control
15 kΩ
47 μF
+
8
9 (10)
TDA1074
7Z84449

Fig. 10 The TDA1594 controlled by the treble/bass circuit TDA1074; common control voltage.

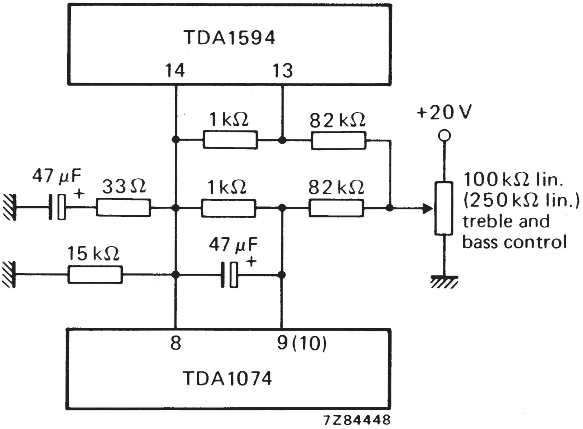

TDA1594
14
13
1 kΩ
82 kΩ
+20 V
47 μF
+
33 Ω
1 kΩ
82 kΩ
100 kΩ lin.
(250 kΩ lin.)
treble and
bass control
15 kΩ
47 μF
+
8
9 (10)
TDA1074
7Z84448

Fig. 11 The TDA1594 controlled by the treble/bass circuit TDA1074; separate control voltage.

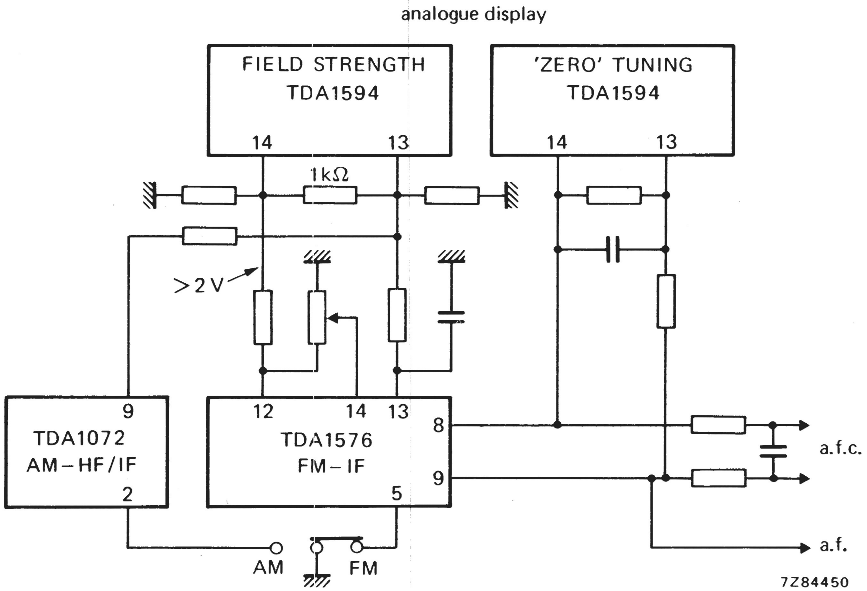

analogue display
FIELD STRENGTH
TDA1594
14
13
'ZERO' TUNING
TDA1594
14
13
1kΩ
>2V
9
TDA1072
AM–HF/IF
2
12
14
13
TDA1576
FM–IF
5
8
9
AM
FM
a.f.c.
a.f.
7Z84450

Fig. 12 Example of a field-strength and tuning display in an AM/FM radio receiver using two TDA1594 circuits.

5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastic package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 35	V
Repetitive peak output current	I_{ORM}	<	1,5	A
Output power at d_{tot} = 10%				
V_P = 18 V; R_L = 8 Ω	P_o	typ.	4,5	W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5	W
Total harmonic distortion at P_o < 2 W; R_L = 8 Ω	d_{tot}	typ.	0,3	%
Input impedance	$\lvert Z_i \rvert$	typ.	45	kΩ
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25	mA
Sensitivity for P_o = 2,5 W; R_L = 8 Ω	V_i	typ.	55	mV
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110B).

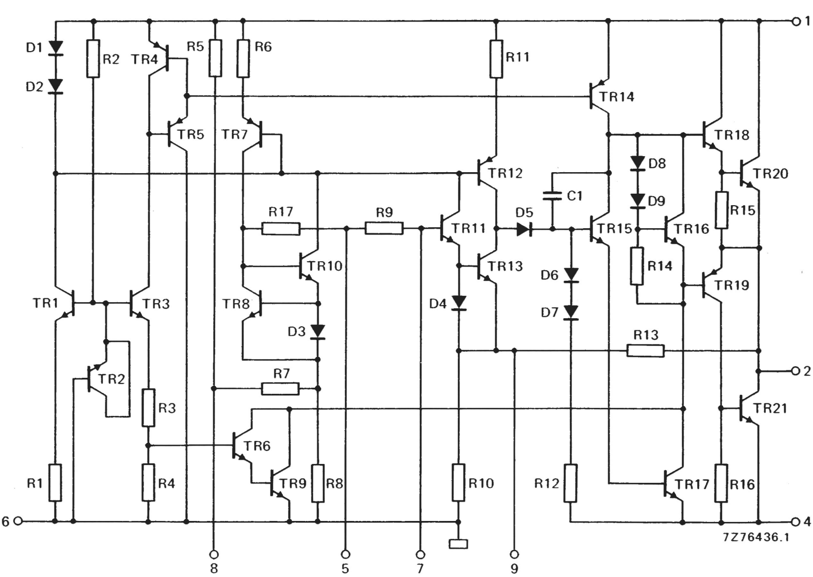

D1
D2
R2
TR4
R5
R6
R11
TR14
TR5
TR7
TR18
D8
TR12
TR20
C1
D9
R17
R9
D5
R15
TR11
TR15
TR16
TR10
TR13
R14
D6
TR1
TR3
TR8
D4
TR19
D7
D3
R13
TR2
R7
R3
TR6
TR9
R1
R4
R8
R10
R12
TR17
R16
TR21
1
2
4
6
8
5
7
9
7Z76436.1

Fig. 1 Circuit diagram; pin 3 not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35	V
Non-repetitive peak output current	I_{OSM}	max.	3	A
Repetitive peak output current	I_{ORM}	max.	1,5	A
Total power dissipation	see derating curves Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature	T_{amb}	−25 to + 150		°C

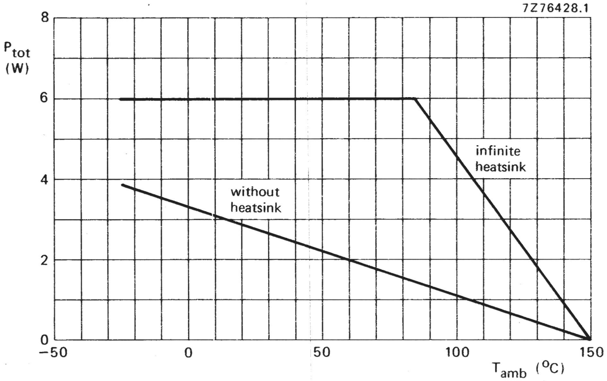


Fig. 2 Power derating curves.

HEATSINK EXAMPLE

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C maximum; T_j = 150 °C (max. for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,2 W).
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150 - 60}{2,2} = 41\ \text{K/W}.$$

Since $R_{th\,j\text{-}tab}$ = 11 K/W and $R_{th\,tab\text{-}h}$ = 1 K/W, $R_{th\,h\text{-}a}$ = 41 − (11 + 1) = 29 K/W.

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 35	V
Repetitive peak output current	I_{ORM}	<	1,5	A
Total quiescent current at $V_P = 18$ V	I_{tot}	typ.	25	mA

A.C. CHARACTERISTICS

$T_{amb} = 25\ ^oC$; $V_P = 18$ V; $R_L = 8\ \Omega$; f = 1 kHz unless otherwise specified; see also Fig. 3

A.F. output power at $d_{tot} = 10\%$				
$V_P = 18$ V; $R_L = 8\ \Omega$	P_o	>	4	W
		typ.	4,5	W
$V_P = 12$ V; $R_L = 8\ \Omega$	P_o	typ.	1,7	W
$V_P = 8{,}3$ V; $R_L = 8\ \Omega$	P_o	typ.	0,65	W
$V_P = 20$ V; $R_L = 8\ \Omega$	P_o	typ.	6	W
$V_P = 25$ V; $R_L = 15\ \Omega$	P_o	typ.	5	W
Total harmonic distortion at $P_o = 2$ W	d_{tot}	typ.	0,3	%
		<	1	%
Frequency response		>	15	kHz
Input impedance	$\|Z_i\|$	typ.	45	kΩ *
Noise output voltage at $R_S = 5$ kΩ; B = 60 Hz to 15 kHz	V_n	typ.	0,2	mV
		<	0,5	mV
Sensitivity for $P_o = 2{,}5$ W	V_i	typ.	55	mV
			44 to 66	mV

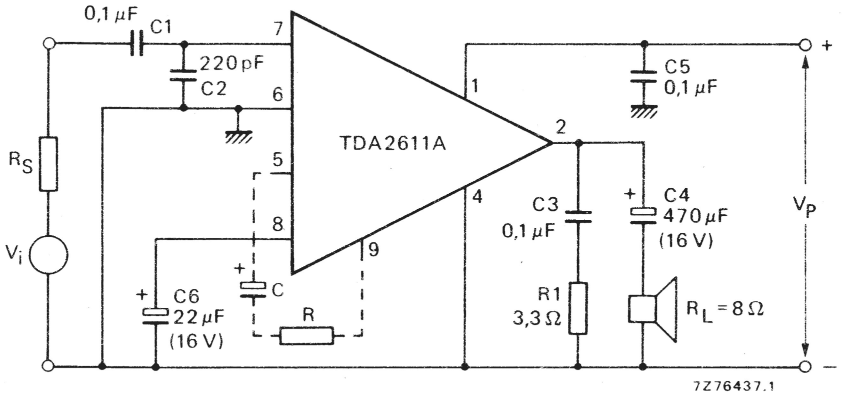

0,1 µF
C1
7
220 pF
C2
6
TDA2611A
5
8
9
1
2
4
C5
0,1 µF
+
−
R_S
V_i
+
C6
22 µF
(16 V)
+
C
R
C3
0,1 µF
R1
3,3 Ω
+
C4
470 µF
(16 V)
R_L = 8 Ω
V_P
7Z76437.1

Fig. 3 Test circuit; pin 3 not connected.

---

* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).

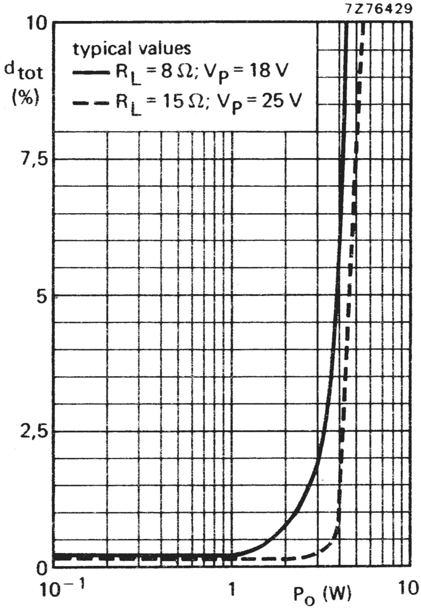


Fig. 4 Total harmonic distortion as a function of output power.

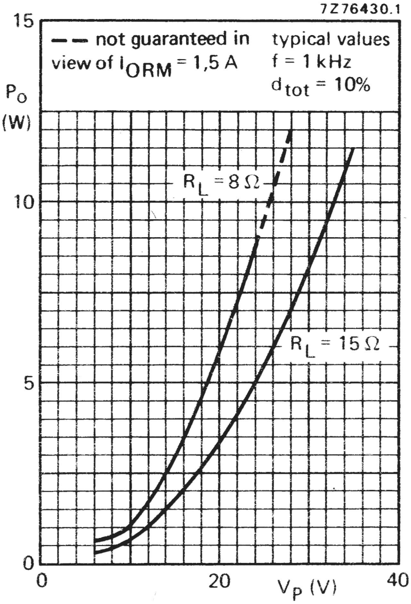


Fig. 5 Output power as a function of supply voltage.

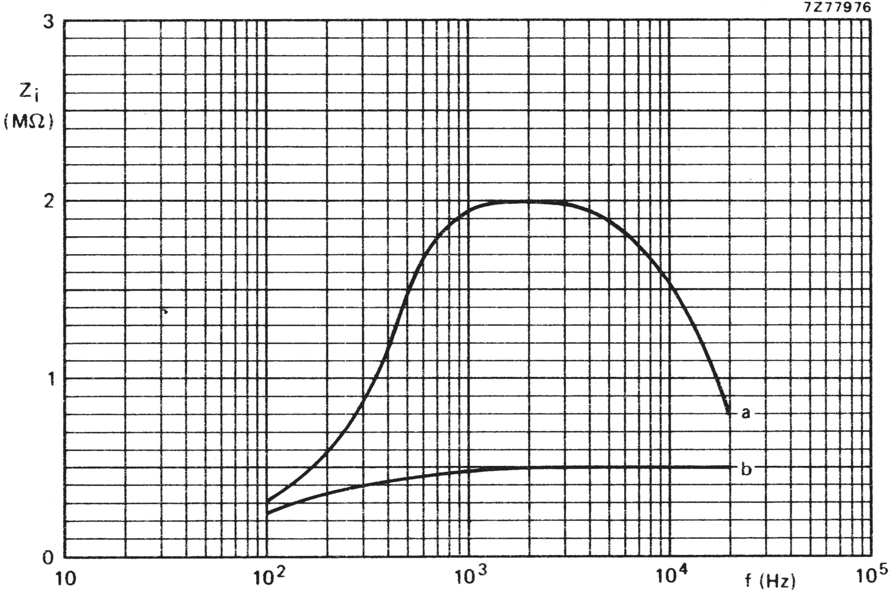


Fig. 6 Input impedance as a function of frequency; curve a for C = 1 μF, R = 0 Ω; curve b for C = 1 μF, R = 1 kΩ; circuit of Fig. 3; C2 = 10 pF; typical values.

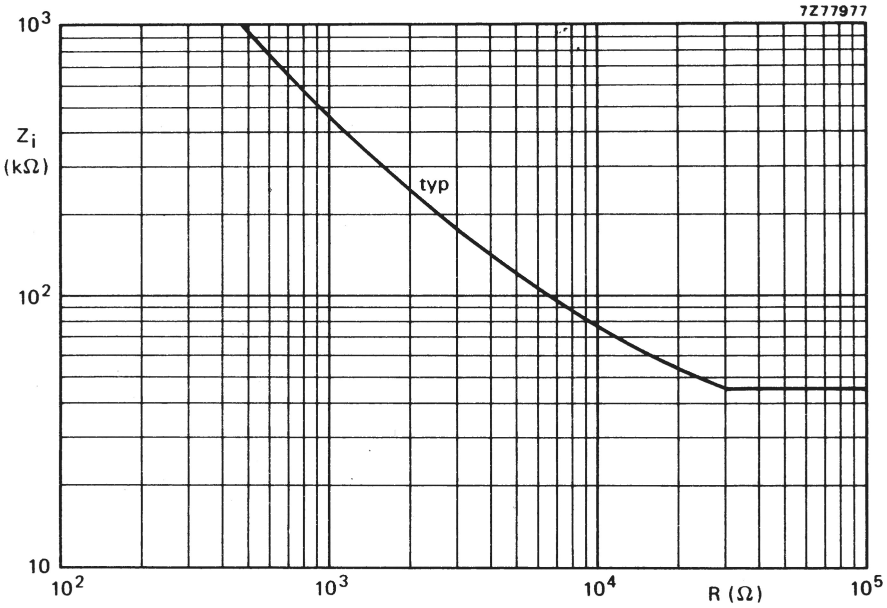


Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

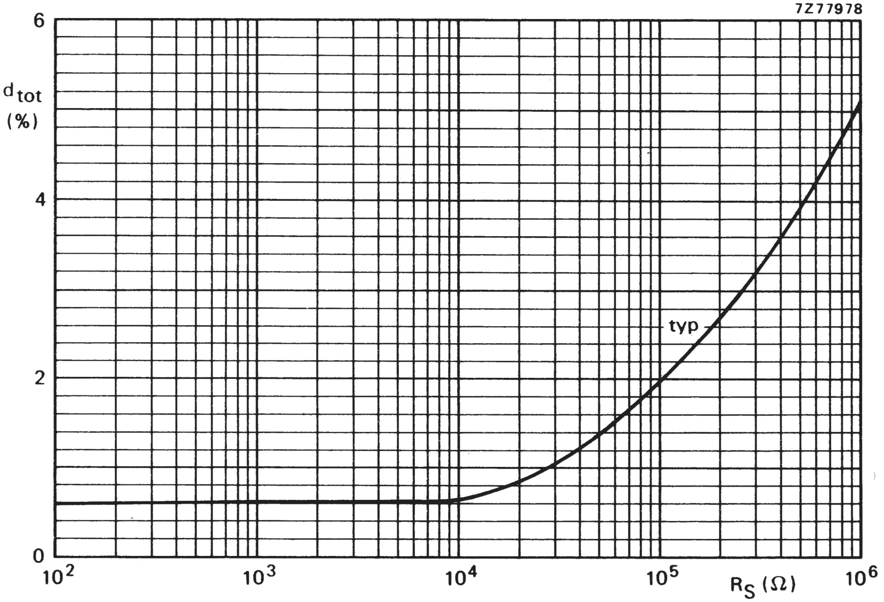
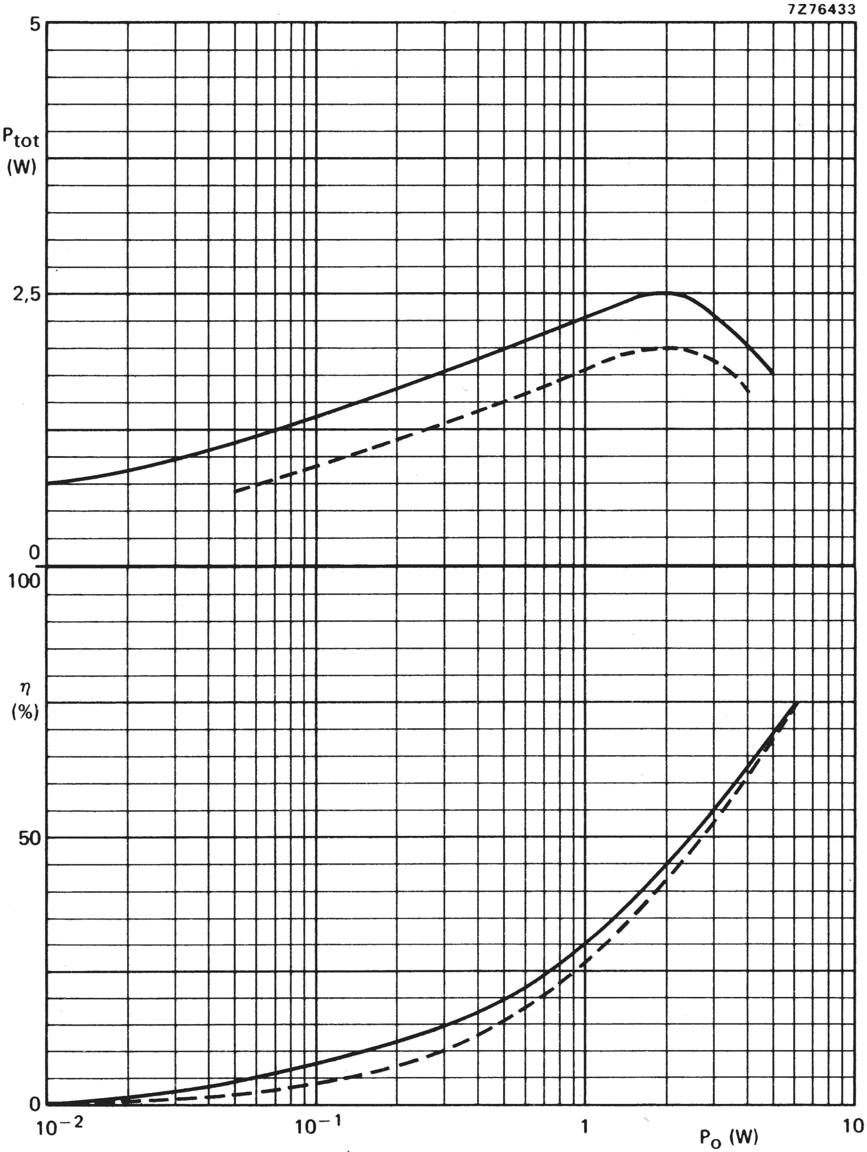


Fig. 8 Total harmonic distortion as a function of R_S in the circuit of Fig. 3; P_o = 3,5 W; f = 1 kHz.



——— $V_P = 25$ V; $R_L = 15\,\Omega$; f = 1 kHz

— — $V_P = 18$ V; $R_L = 8\,\Omega$; f = 1 kHz

Fig. 9 Total power dissipation and efficiency as a function of output power.

APPLICATION INFORMATION

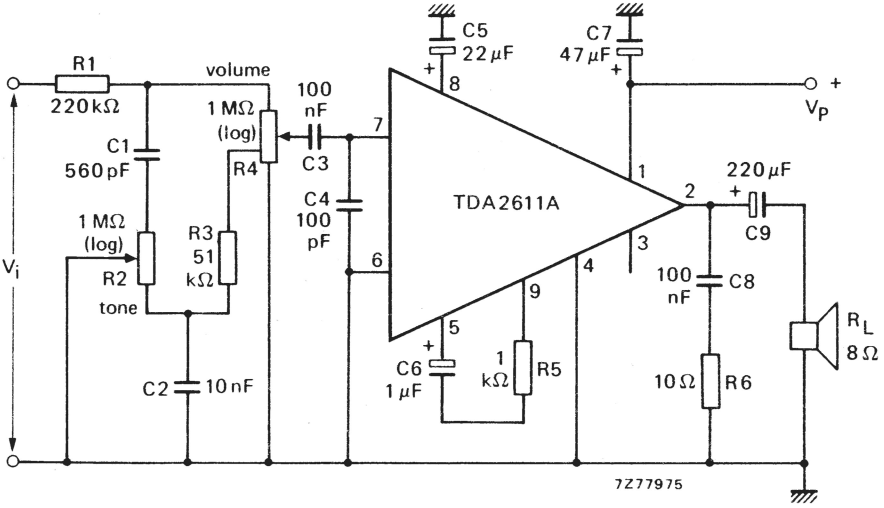

R1
220kΩ
C1
560pF
volume
1 MΩ
(log)
R4
100
nF
C3
C4
100
pF
7
6
1 MΩ
(log)
R2
tone
R3
51
kΩ
C2
10nF
Vi
C5
22 μF
8
C7
47 μF
+
Vp
TDA2611A
1
2
3
4
9
5
C6
1 μF
1
kΩ
R5
220 μF
C9
100
nF
C8
10 Ω
R6
RL
8 Ω
7Z77975

Fig. 10 Ceramic pickup amplifier circuit.

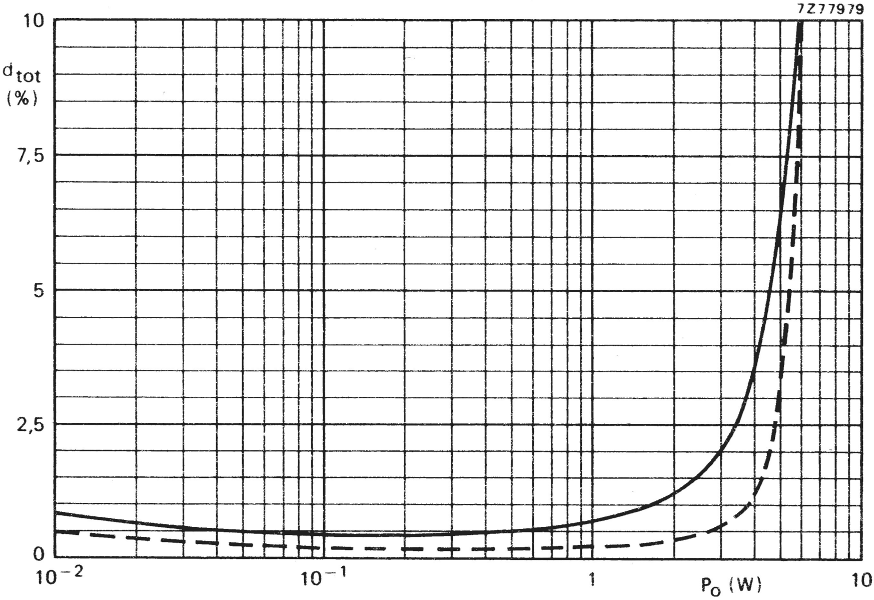


Fig. 11 Total harmonic distortion as a function of output power; —— with tone control; – – – without tone control; in circuit of Fig. 10; typical values.

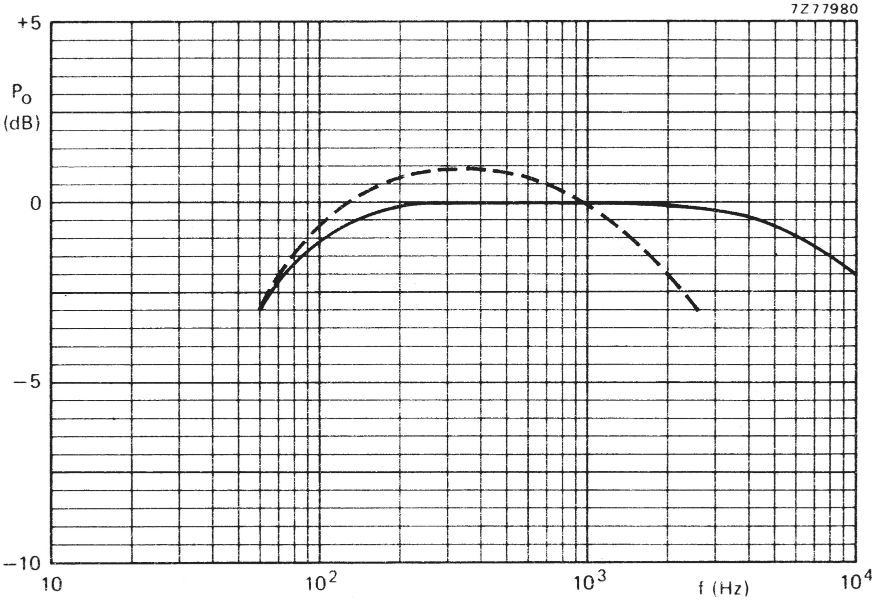


Fig. 12 Frequency characteristics of the circuit of Fig. 10; —— tone control max. high; – – – tone control min. high; P_o relative to 0 dB = 3 W; typical values.

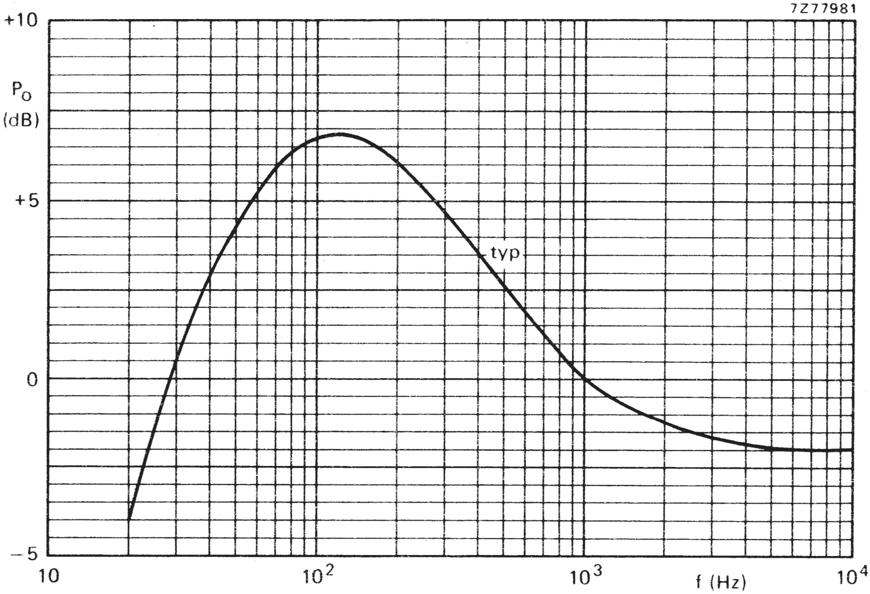


Fig. 13 Frequency characteristic of the circuit of Fig. 10; volume control at the top; tone control max. high.

INTEGRATED AM/FM RADIO RECEIVER CIRCUIT

The TDA5700 is for use in high quality battery or mains-fed a.m. and a.m./f.m. receivers as well as small low-cost a.m. portable receivers. The IC incorporates: a.m. mixer, oscillator, i.f. amplifier, a.g.c. amplifier, a.m. detector and capacitor, f.m./i.f. limiting amplifier and stable base bias for f.m. front-end. The TDA5700 is pin compatable, with the h.f. part of the TBA570A and can be used with conventional coils or ceramic resonators.
The combination of a good sound quality (d_{tot}) and quality of reception (a.g.c.) makes the IC well suitable for universal application of one basic printed-circuit board in a wide range of receiver designs.

QUICK REFERENCE DATA

Applicable supply voltage range of receiver	V_S		2,7 to 12	V
Supply voltage range (pin 8)	V_P		3,4 * to 5,4	V
Ambient temperature	T_{amb}		25	°C
Supply voltage (pin 8)	V_P	nom.	5,4	V
Total quiescent current	I_{tot}	typ.	9	mA
A.M. performance (at pin 2)				
Sensitivity for V_o = 30 mV	V_i	3,0 to	12	μV
for V_o = 30 mV; range 1**	V_i	5,5 to	12	μV
for V_o = 30 mV; range 2**	V_i	3,0 to	6,5	μV
R.F. input voltage for S/N = 26 dB	V_i	typ. <	16 20	μV μV
for V_o = 10 mV	V_i	typ.	2,5	μV
A.G.C. range; change of r.f. input voltage for 10 dB expansion in audio range		typ.	65	dB
R.F. signal handling d_{tot} = 10%; m = 0,8	V_i	typ.	300	mV
F.M. performance (at pin 2)				
R.F. input voltage 3 dB before limiting	V_i	typ.	180	μV

* Minimum supply voltage for guaranteed oscillator operation: V_P = 2,5 V (see Fig. 3).

** There are two ranges of sensitivity measured, and indicated by either ‘1’ or ‘2’ on the package. Ordering a specific range is not possible.
For designs requiring a lower spread of sensitivity, these ranges can be used adapting the application.

PACKAGE OUTLINES

TDA5700: 16-lead DIL: plastic (SOT-38).
TDA5700Q: 16-lead QIL; plastic (SOT-58).

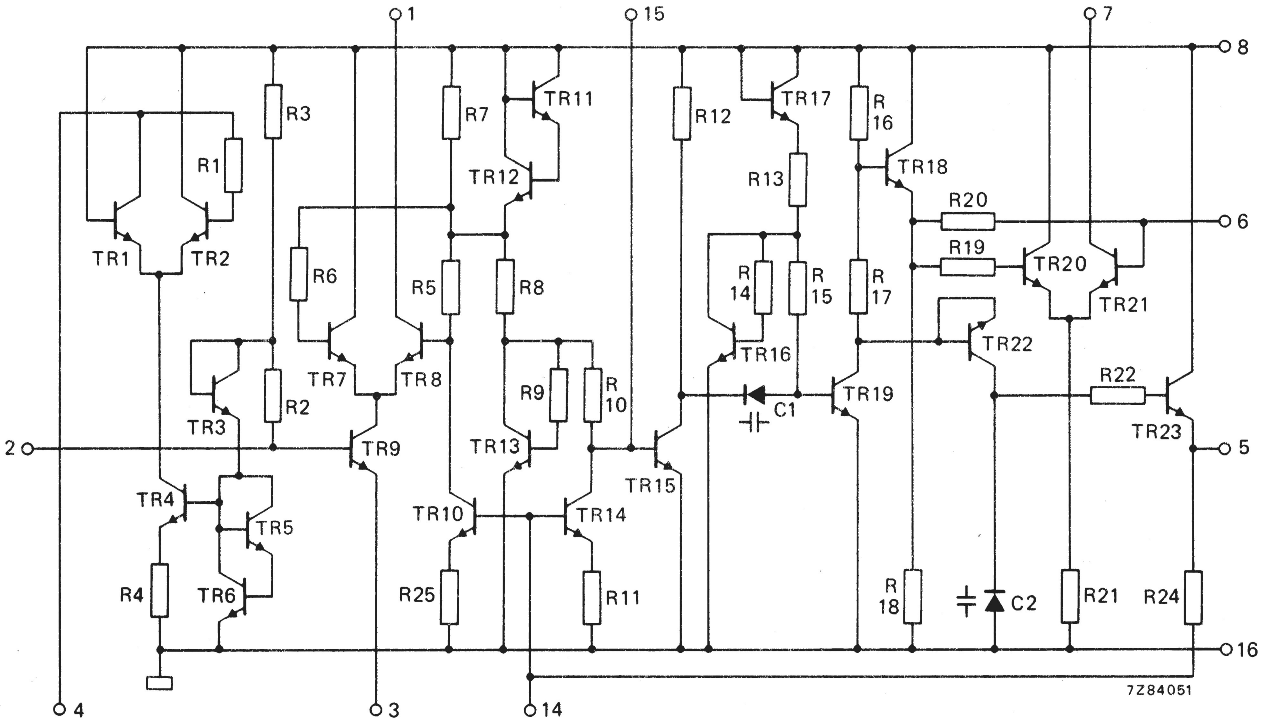

1
15
7
8
6
5
16
2
4
3
14
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
TR9
TR10
TR11
TR12
TR13
TR14
TR15
TR16
TR17
TR18
TR19
TR20
TR21
TR22
TR23
R1
R2
R3
R4
R5
R6
R7
R8
R9
R 10
R11
R12
R13
R 14
R 15
R 16
R 17
R 18
R19
R20
R21
R22
R24
R25
C1
C2
7Z84051

Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	$V_{8\text{-}16} = V_P$	max.	7 V
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature $V_{8;\,4;\,7;\,1\text{-}16} = 7$ V; see also derating curve Fig. 2	T_{amb}		−20 to + 85 °C

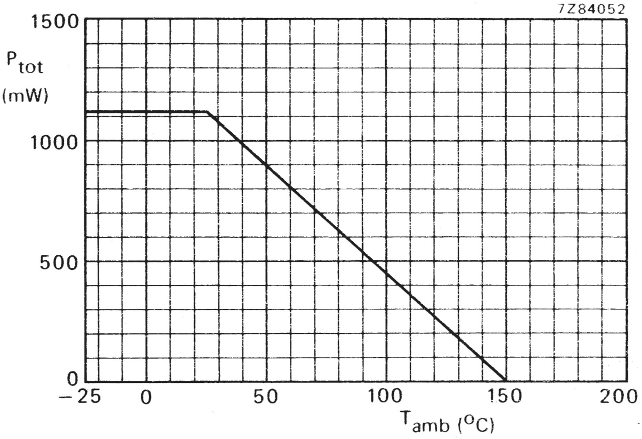


Fig. 2 Total power dissipation derating curve.

DESIGN DATA

Characteristics of integrated components are determined by process and layout data.

Pins not under measuring condition should not be connected.

Pins 9, 10, 11, 12 and 13 are not allowed to be connected

Voltage pins 1 and 7	$V_{1\text{-}16}$ $V_{7\text{-}16}$	max.	12 V*
Voltage pin 4	$V_{4\text{-}16}$	min. max.	$V_8 - 0,5$ V* $V_8 + 0,5$ V*
Voltage pin 8	$V_{8\text{-}16} = V_P$	max.	7 V*
Voltage pin 3	$V_{3\text{-}16}$	max.	3 V*
Voltage pin 5	$V_{5\text{-}16}$	max.	4 V*
Voltage pin 14	$V_{14\text{-}16}$	max.	1 V*
Current pin 2, 6 and 15	I_2; I_6; I_{15}	max.	80 μA*

D.C. CHARACTERISTICS

$T_{amb} = 25\ ^oC$

Total quiescent current			
$V_P = 5,4$ V	I_{tot}	typ.	9 mA
$V_P = 3,4$ V	I_{tot}	typ.	8 mA
Applicable supply voltage range of receiver	V_S		2,7 to 12 V**
Recommended supply voltage range for full performance (pin 8)	V_P		3,4▲ to 5,4 V
Base bias voltage for f.m. front-end total external load current at pin 2: $-I_2 = 150\ \mu A$	$V_{2\text{-}16}$	typ.	1,2 V

A.C. CHARACTERISTICS

$T_{amb} = 25\ ^oC$; $V_P = 5,4$; I_E (TR9) = 1 mA; unless otherwise specified

			0,45	1	10,7 MHz
Input conductance at pin 2	g_{ie}	typ.	–	0,3	0,4 mA/V
Output conductance at pin 1	g_{oe}	typ.	10	–	40 μA/V
Input conductance at pin 15	g_{ie}	typ.	0,5	–	1,0 mA/V

---

* Tolerated minimum for voltages 0 V; for currents 0 mA.

** Adjustable by a dropping resistor in the V_S-line; see also maximum tolerated voltages for pins 1, 4, 7 and 8 in design data above.

▲ Minimum supply voltage for guaranteed oscillator operation: $V_P = 2,5$ V.

A.M. performance (in test circuit Fig. 3)

	$V_{8\text{-}16} = V_P$		5,4 V	3,4 V (note 4)	
Signal-to-noise ratio at V_i = 20 μV (notes 1 and 2)	S/N	>	26	26	dB
R.F. input voltage for S/N = 26 dB	V_i	typ.	16	16	μV
		<	20	20	μV
R.F. input voltage for 30 mV (a.f.)					
across volume control	V_i		3,0 to 12		μV
range 1	V_i		5,5 to 12		μV
range 2	V_i		3,0 to 6,5		μV
A.F. voltage across volume control at 100 μV (r.f.) input voltage (notes 1 and 2)	V_o	typ.	100	100	mV
Signal-to-noise ratio at 1 mV (r.f.) input voltage (notes 1 and 2)	S/N	typ.	46	49	dB
A.G.C. range (change in r.f. input voltage for 10 dB expansion in audio range) (notes 1 and 2)		typ.	65	65	dB
R.F. signal handling capability at 80% modulation; $d_{tot} < 10\%$ (note 1)	V_i	typ.	300	100	mV
Total harmonic distortion of h.f. part over most of a.g.c. range; m = 0,3; f_m = 1 kHz	d_{tot}	typ.	1	1	%
I.F. selectivity	Sg	typ.	33	33	dB
I.F. bandwidth (3 dB)	B	typ.	5	5	kHz

F.M. performance (in test circuit Fig. 4)

T_{amb} = 25 °C; V_P = 5,4 V; f_o = 10,7 MHz; Δf = ±22,5 kHz; f_m = 1 kHz; R_S = 25 Ω; unless otherwise specified.

Sensitivity for an f.m. signal 3 dB before limiting				
at pin 2	V_i	typ.	180	μV
at pin 15	V_i	typ.	400	μV
A.F. output voltage across a load of 100 kΩ	V_o	typ.	140	mV
Signal-to-noise ratio over most of signal range	S/N	typ.	65	dB
A.F. signal distortion 3 dB before i.f. limiting (note 3)	d_{tot}	typ.	0,5	%

Notes

1. a. A.F. signal: measured across volume control.
   b. R.F. signal: measured at pin 2 at source impedance of 25 Ω.
   c. f_o = 1 MHz; f_m = 400 Hz.
2. m = 0,3.
3. Δf = ± 40 kHz; measured with V_o at maximum.
4. Minimum supply voltage for guaranteed oscillator operation: V_P = 2,5 V.

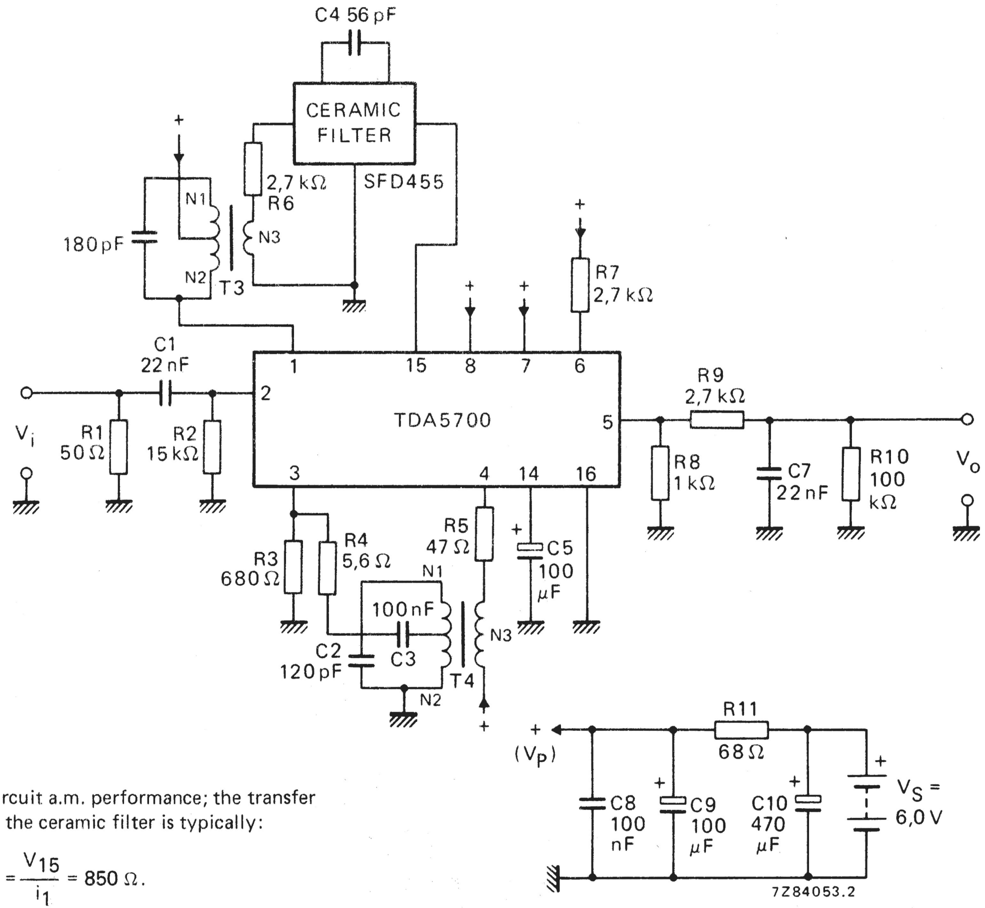

C4 56 pF
CERAMIC FILTER
SFD455
2,7 kΩ
R6
N3
N1
N2
T3
180 pF
+
C1
22 nF
Vi
R1
50 Ω
R2
15 kΩ
1
2
3
15
8
7
6
5
4
14
16
TDA5700
R7
2,7 kΩ
R9
2,7 kΩ
R8
1 kΩ
C7
22 nF
R10
100
kΩ
Vo
R3
680 Ω
R4
5,6 Ω
R5
47 Ω
C5
100
μF
100 nF
C3
C2
120 pF
T4
+
(Vp)
R11
68 Ω
C8
100
nF
C9
100
μF
C10
470
μF
VS =
6,0 V
7Z84053.2

Fig. 3 Test circuit a.m. performance; the transfer impedance of the ceramic filter is typically:

$$Z_{tr} = \frac{V_{15}}{i_1} = 850\ \Omega.$$

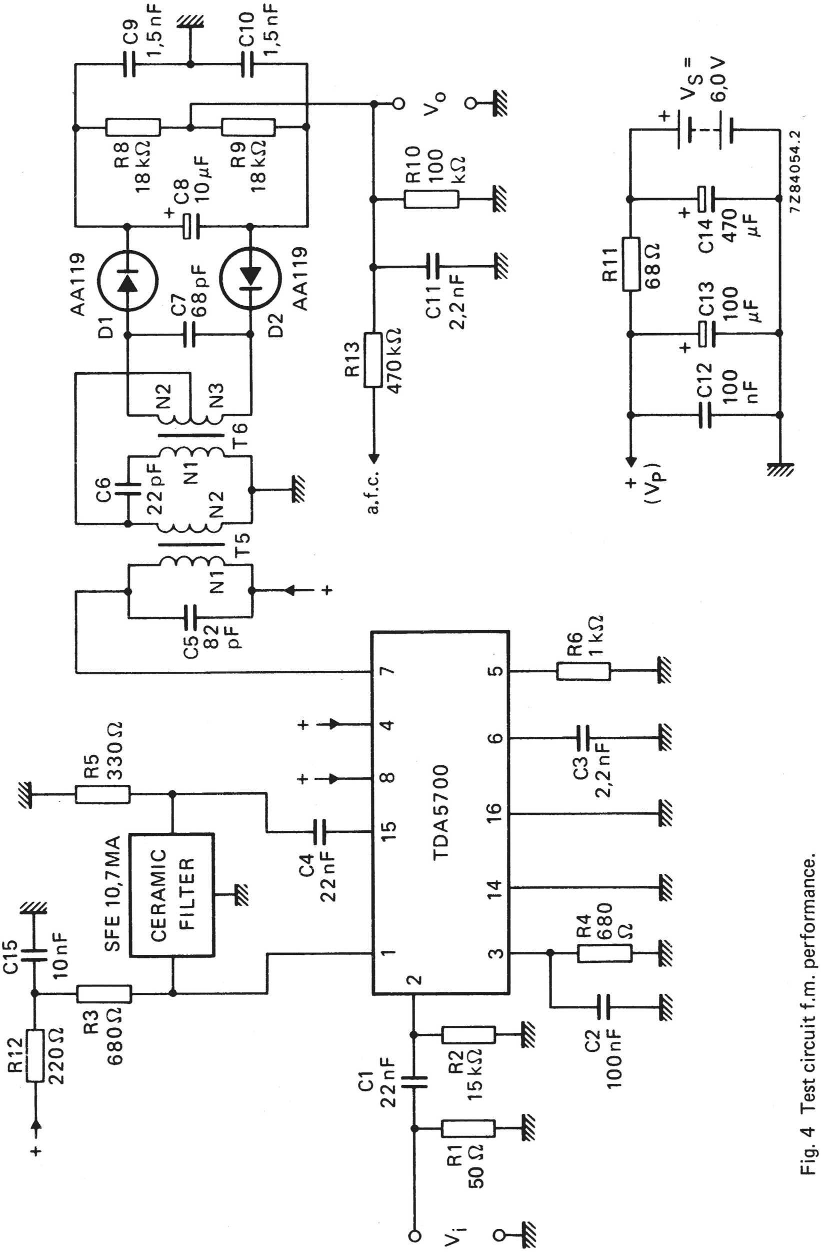

C9
1,5 nF
C10
1,5 nF
R8
18 kΩ
R9
18 kΩ
C8
10 μF
V_o
R10
100
kΩ
V_S =
6,0 V
AA119
D1
C7
68 pF
AA119
D2
C11
2,2 nF
R13
470 kΩ
a.f.c.
R11
68 Ω
C14
470
μF
C13
100
μF
C12
100
nF
+ (V_P)
7Z84054.2
N2
N3
T6
C6
22 pF
N1
N2
T5
N1
C5
82
pF
+
R5
330 Ω
SFE 10,7MA
CERAMIC
FILTER
C4
22 nF
TDA5700
R6
1 kΩ
C3
2,2 nF
R4
680
Ω
C2
100 nF
C15
10 nF
R12
220 Ω
R3
680 Ω
C1
22 nF
R2
15 kΩ
R1
50 Ω
V_i
1
2
3
4
5
6
7
8
14
15
16

Fig. 4 Test circuit f.m. performance.

APPLICATION INFORMATION

F.M. performance of the complete f.m. circuit (measured in Figs 5, 6 and 7 at $V_S = 9$ V)

Sensitivity for an f.m. signal 3 dB before limiting at 75 Ω aerial input of the f.m. front-end (note 1)	V_i	typ.	4 μV
Sensitivity for 26 dB S/N ratio at 75 Ω aerial input of the f.m. front-end (note 1)	V_i	typ.	3 μV
A.F. output voltage across a volume control of 100 kΩ at an i.f. signal beyond limiting	V_o	typ.	140 mV
Signal-to-noise over most of the signal range	S/N	typ.	70 dB
A.M. suppression over most of the signal range (note 2)	S/N	typ.	60 dB
I.F. selectivity (note 3)	S_{300}	typ.	55 dB
I.F. bandwidth (3 dB; note 3)	B	typ.	180 kHz
A.F. distortion at an i.f. signal level 3 dB before limiting (note 4)	d_{tot}	typ.	0,5 %

Notes

1. Aerial e.m.f. (V_i) at $f_o = 98$ MHz; $R_S = 75$ Ω; Δf = ±22,5 kHz; $f_m = 1$ kHz.
2. A.M. signal: m = 0,3; $f_m = 1$ kHz.
   F.M. signal: $f_o = 10,7$ MHz; Δf = ± 75 kHz; $f_m = 70$ Hz.
   Carrier simultaneously modulated with a.m. and f.m.
3. Including the ratio detector, measured at N1 of the secondary coil (T6) of the ratio detector.
   Level of measurement: 3 dB before limiting.
4. $f_o = 98$ MHz; Δf = 40 kHz; $f_m = 1$ kHz.
   Measurement carried out selectively to avoid noise influence on meter reading.

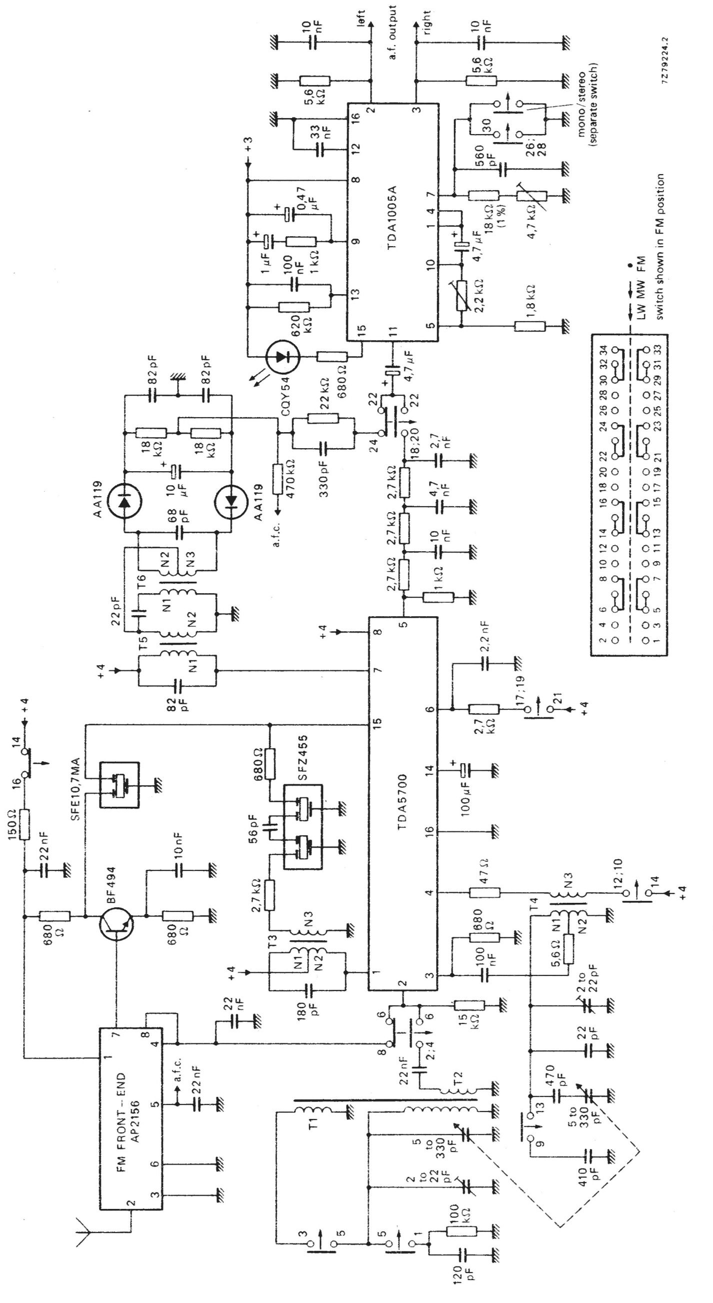

TDA5700
TDA1005A
FM FRONT-END
AP2156
BF494
SFE10,7MA
SFZ455
CQY54
AA119
AA119
T1
T2
T3
T4
T5
T6
N1
N2
N3
a.f.c.
a.f. output
left
right
mono/stereo
(separate switch)
LW MW FM
switch shown in FM position
+4
+3
150 Ω
22 nF
680 Ω
10 nF
680 Ω
2,7 kΩ
56 pF
180 pF
82 pF
22 pF
18 kΩ
10 μF
68 pF
470 kΩ
330 pF
22 kΩ
680 Ω
620 kΩ
100 nF
1 μF
1 kΩ
0,47 μF
33 nF
5,6 kΩ
10 nF
4,7 μF
2,2 kΩ
1,8 kΩ
18 kΩ (1%)
4,7 kΩ
560 pF
2,7 nF
4,7 nF
1 kΩ
2,2 nF
100 μF
47 Ω
5,6 Ω
2 to 22 pF
470 pF
5 to 330 pF
410 pF
120 pF
100 kΩ
15 kΩ
7Z79224.2

Fig. 5 Circuit diagram of an a.m./f.m. stereo receiver using TDA5700.
For audio output stages see Fig. 7.

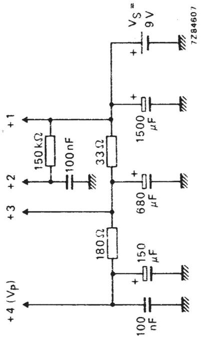

V_S = 9 V
+1
+2
+3
+4 (V_P)
150 kΩ
100 nF
33 Ω
1500 μF
680 μF
180 Ω
150 μF
100 nF
7Z84607

Fig. 6 Supply circuit of Figs 5 and 7.

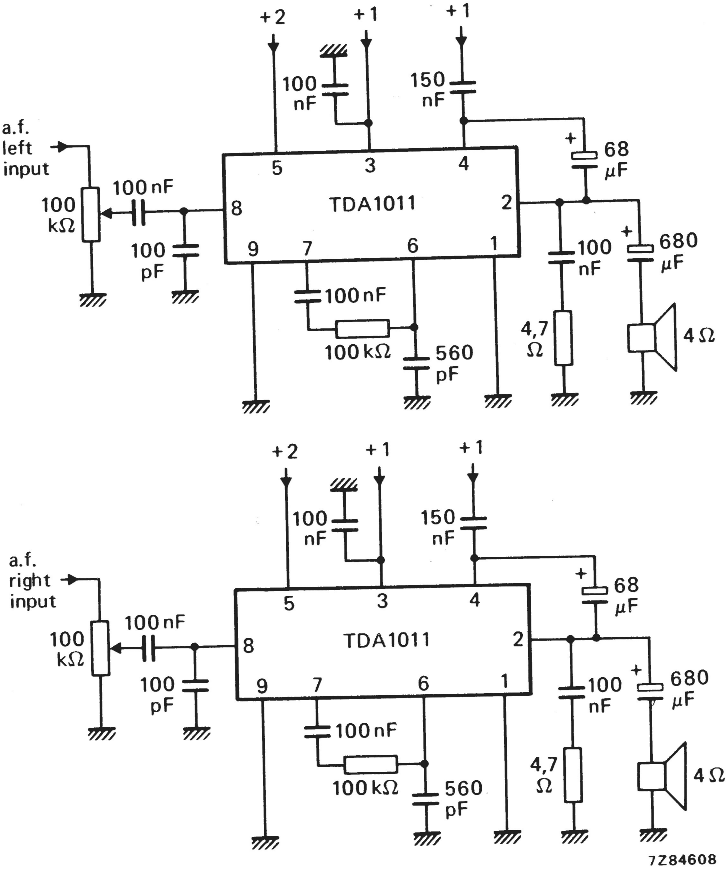

+2
+1
+1
100 nF
150 nF
a.f. left input
100 kΩ
100 nF
100 pF
5
3
4
8
TDA1011
2
9
7
6
1
68 μF
100 nF
680 μF
100 nF
100 kΩ
560 pF
4,7 Ω
4 Ω
+2
+1
+1
100 nF
150 nF
a.f. right input
100 kΩ
100 nF
100 pF
5
3
4
8
TDA1011
2
9
7
6
1
68 μF
100 nF
680 μF
100 nF
100 kΩ
560 pF
4,7 Ω
4 Ω
7Z84608

Fig. 7 Stereo output stages of Fig. 5. For supply circuit see Fig. 6.

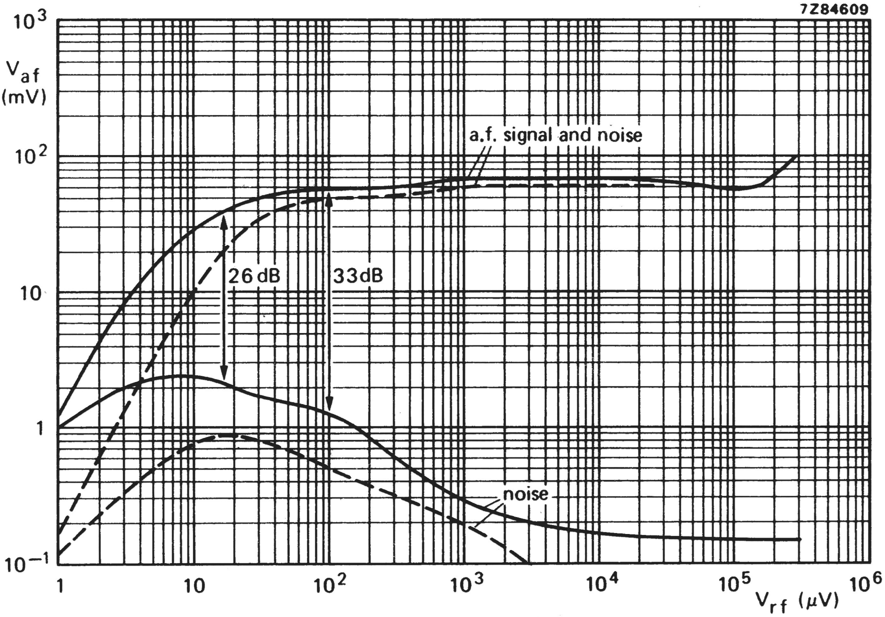


Fig. 8 Typical S/N curves for a.m. reception (see Fig. 5); a.f. voltage at a.m. detector output (pin 5) with slider of volume control at the lower end (ground) as a function of r.f. input voltage at pin 2. —— $V_P = 5,4$ V; ––– $V_P = 3,2$ V; $f_o = 1$ MHz; $f_m = 400$ Hz; $m = 30\%$; $R_S \approx 25\ \Omega$ (pin 2).

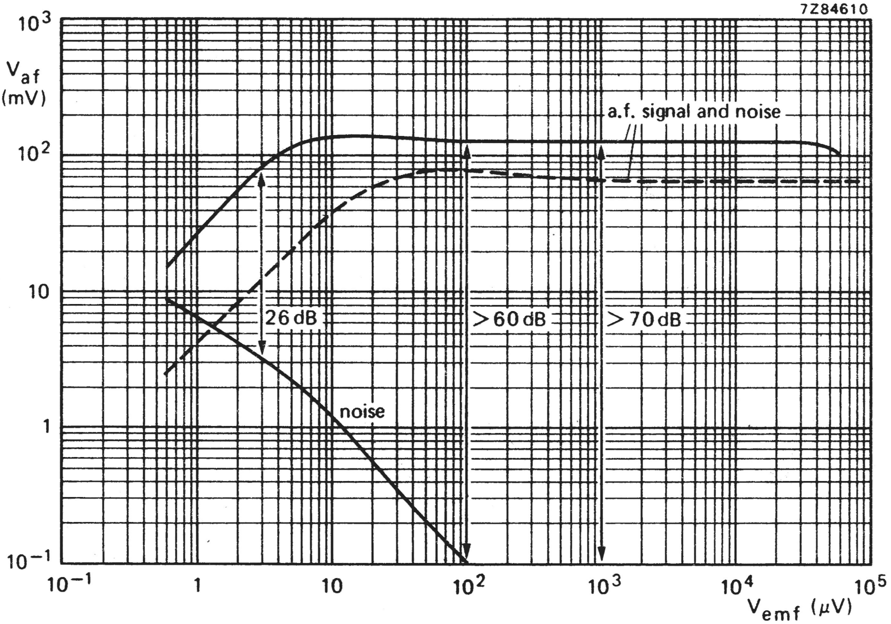
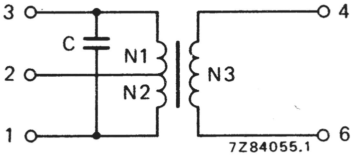


Fig. 9 Typical S/N curves for f.m. reception (see Fig. 5); a.f. voltage at f.m. detector output with slider of volume control at the lower end (ground) as a function of aerial e.m.f. from a source with R_S = 50 Ω to the 75 Ω input of the f.m. front-end.

—— V_P = 5,2 V; – – – V_P = 3 V; f_o = 98 MHz; Δf = ±22,5 kHz; f_m = 1 kHz.

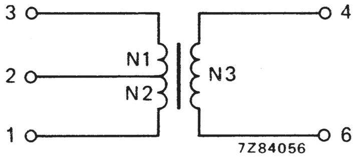
COIL DATA

A.M. – i.f. coils (Figs 3 and 5)


3
C
N1
2
N2
N3
1
4
6
7Z84055.1

N1 = 86
N2 = 60
N3 = 8
C = 180 pF

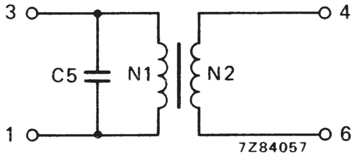
Fig. 10 I.F. bandpass filter (T3). TOKO sample no. 7 MCS-A 3544 EK. L = 680 μH at 455 kHz; Q_o = 110.


3
N1
2
N2
N3
1
4
6
7Z84056

N1 = 55
N2 = 2
N3 = 9

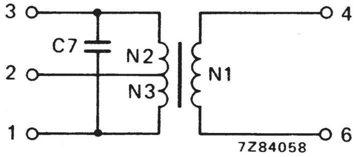
Fig. 11 Oscillator coil (T4). TOKO sample no. 7 BOS-A 3498 EK. L = 115 μH at 796 kHz; Q_o = 110.

F.M. – i.f. coils (Figs 4 and 5)


3
C5
N1
N2
1
4
6
7Z84057

N1 = 11
N2 = 5
C5 = 82 pF

Fig. 12 Primary ratio detector coil (T5). TOKO sample no. 119 ACS-A 3503 AO. L = 2,7 μH at 10,7 MHz; Q_o = 90.


3
C7
N2
2
N3
N1
1
4
6
7Z84058

N3 = 6
N2 = 6
N1 = 2
C7 = 68 pF

Fig. 13 Secondary ratio detector coil (T6). TOKO sample no. 119 ACS-A 3258 EK. L = 3,25 μH at 10,7 MHz; Q_o = 85.

AM CAR RADIO RECEIVER CIRCUIT

The TEA5550 is an a.m. radio circuit, primarily intended for use in car radios.
The IC can reduce the costs in a car radio due to the following features:

- minimum periphery
- no extra r.f.-prestage is necessary
- ceramic i.f. filter is used
- simple on/off switching method allows inexpensive band switching in a.m./f.m. radios

The TEA5550 incorporates the following functions:

- a double balanced mixer with large signal handling range and common mode rejection properties
- a 'one-pin' oscillator, permitting the use of variable capacitance diode tuning
- an i.f. amplifier, designed for ceramic filters
- an a.m. envelope detector
- a.g.c. stages
- a voltage stabilizer, for supplying the internal circuit current and an external current up to 20 mA
- a simple d.c. switch for a.m./f.m. radios

QUICK REFERENCE DATA

Supply voltage range; unstabilized (pin 8)	V_P		10,2 to 18	V
Supply voltage; stabilized (pin 9)*	V_{stab}	typ.	7,5 to 9	V
Ambient temperature	T_{amb}	typ.	25	°C
Supply voltage (pin 8)	V_P	typ.	14,4	V
R.F. condition: f_i = 1 MHz; m = 0,3; f_m = 1 kHz				
R.F. input voltage (pin 1)				
V_o = 30 mV	V_i	typ.	4	μV
S/N = 26 dB	V_i	typ.	16	μV
S/N = 46 dB	V_i	typ.	160	μV
A.F. output voltage (pin 10)				
V_i = 10 mV	V_o	typ.	180	mV
Total harmonic distortion over most of the a.g.c. range; m = 0,8	THD	typ.	1,2	%
R.F. signal handling				
THD = 10%; m = 0,8	V_i	typ.	400	mV
A.G.C. range; change of r.f. input voltage for 10 dB change of a.f. output voltage (reference V_{i1} = 200 mV)	V_{i1}/V_{i2}	typ.	86	dB

* Pins 8 and 9 have to be short-circuited externally.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

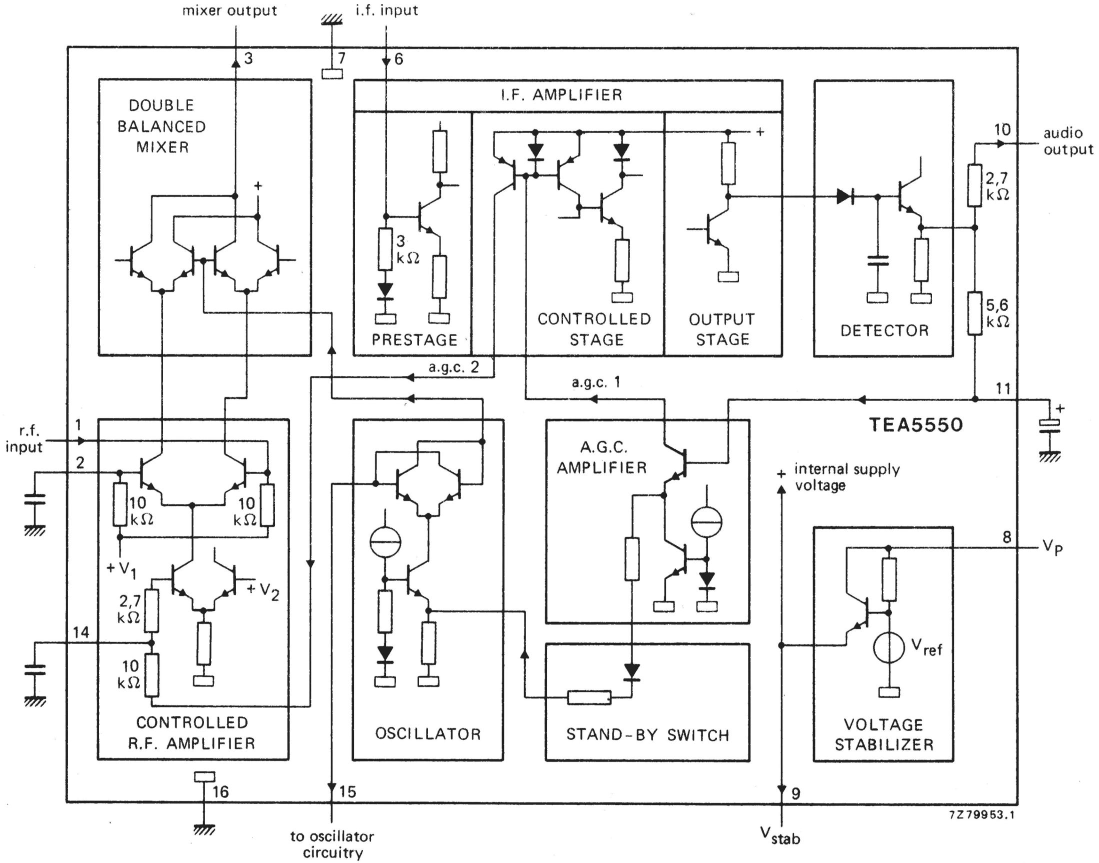

mixer output
i.f. input
3
7
6
DOUBLE
BALANCED
MIXER
I.F. AMPLIFIER
PRESTAGE
CONTROLLED
STAGE
OUTPUT
STAGE
DETECTOR
3
kΩ
+
10
audio
output
2,7
kΩ
5,6
kΩ
11
a.g.c. 2
a.g.c. 1
TEA5550
r.f.
input
1
2
10
kΩ
10
kΩ
+ V1
+ V2
2,7
kΩ
14
10
kΩ
CONTROLLED
R.F. AMPLIFIER
OSCILLATOR
A.G.C.
AMPLIFIER
STAND-BY SWITCH
+ internal supply
voltage
8
VP
Vref
VOLTAGE
STABILIZER
16
15
9
to oscillator
circuitry
Vstab
7Z79953.1

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages				
pin 8	$V_P = V_{8\text{-}16}$	max.	24	V
pin 3	$V_{3\text{-}16}$	max.	24	V
Non-repetitive peak output current (pin 9)	I_{9SM}	max.	100	mA
Total power dissipation	P_{tot}	max.	1100	mW
Storage temperature	T_{stg}		−65 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 85	°C

Note

Pins 4, 5, 12 and 13 are not allowed to be connected.

D.C. CHARACTERISTICS at $V_i = 0$

$V_P = 14{,}4$ V; $T_{amb} = 25$ °C; measured in Fig. 2

Supply voltage range (unstabilized)*	V_P		10,2 to 18	V
Voltage at pin 9; $-I_9 = 0$	$V_{9\text{-}16} = V_{stab}$	typ.	8,7	V
			8 to 9,2	V
Change in stabilization voltage (pin 9)				
at $-I_9 = 0$ to 20 mA	$\Delta V_{9\text{-}16} = \Delta V_{stab}$	typ.	50	mV
at $V_P = 10{,}2$ to 14,4 V	$\Delta V_{9\text{-}16} = \Delta V_{stab}$	typ.	300	mV
Voltage at pin 10	$V_{10\text{-}16}$	typ.	1,1	V
Voltage at pins 1 and 2	$V_{1\text{-}16} = V_{2\text{-}16}$	typ.	5,0	V
Voltage at pin 15	$V_{15\text{-}16}$	typ.	V_{stab}	
Total supply current; $-I_9 = 0$	I_{tot}	typ.	20	mA
Current drain				
pin 3	I_3	typ.	1	mA
pin 15	I_{15}	typ.	0,2	mA
Current supplied from pin 9	$-I_9$	<	20	mA
Power consumption; $-I_9 = 0$	P	typ.	300	mW

---

* A stabilized supply voltage of 7,5 to 9 V can also be applied at pin 9 (pin 8 short-circuited to pin 9).

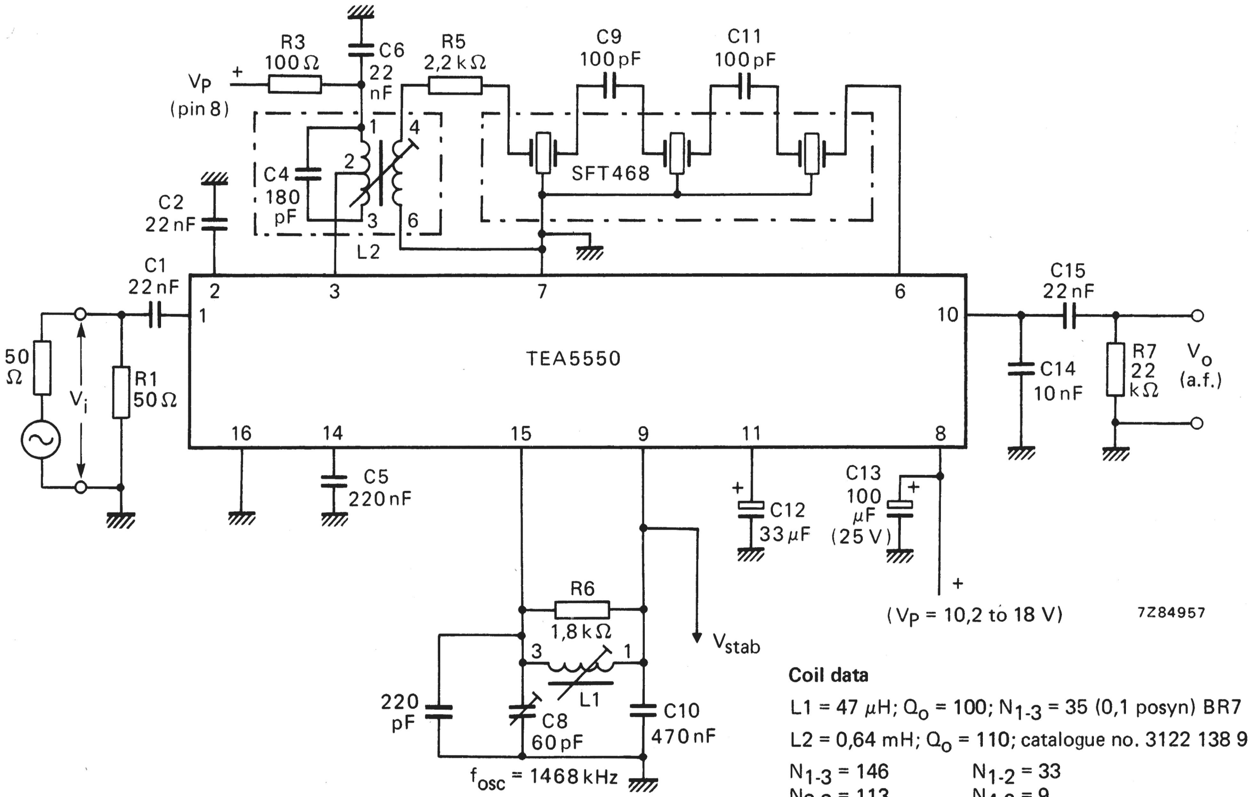
A.C. CHARACTERISTICS

V_P = 14,4 V; T_{amb} = 25 °C; r.f. condition: f_i = 1 MHz, m = 0,3, f_m = 1 kHz; transfer impedance of the i.f. filter $Z_{tr} = v_6/i_3$ = 850 Ω (loaded with 3 kΩ); measured in Fig. 2; unless otherwise specified

R.F. input voltage; V_o = 30 mV	V_i		1,5 to 6,5	μV
R.F. sensitivity at R_S = 25 Ω for:				
S + N/N = 6 dB	V_i	typ.	1,3	μV
S + N/N = 20 dB	V_i	typ.	8	μV
S + N/N = 26 dB	V_i	typ. <	16 20	μV μV
S + N/N = 46 dB	V_i	typ.	160	μV
S + N/N = 50 dB	V_i	typ.	350	μV
Input conductance at pin 1				
V_i = 0,1 mV	g_{ie}	typ.	0,2	mS
V_i = 100 mV	g_{ie}	typ.	0,1	mS
Input conductance at pin 6	g_{ie}	typ.	0,3	mS
Output capacitance at pin 15	C_{oe}	typ.	20	pF
A.G.C. range; change of r.f. input voltage for 10 dB change of a.f. output voltage (reference V_{i1} = 200 mV)	V_{i1}/V_{i2}	typ.	86	dB
A.F. output voltage				
V_i = 10 mV	V_o	> typ.	140 180	mV mV
Spread of a.f. output voltage	ΔV_o	typ.	± 2	dB
A.F. output impedance (pin 10)	$\lvert Z_o \rvert$	typ.	2,7	kΩ
Total harmonic distortion at m = 0,8				
V_i = 16 μV	THD	<	2,5	%
over most of the a.g.c. range (see also Figs 3 and 10)	THD	typ.	1,2	%
V_i = 25 mV	THD	typ.	3,5	%
R.F. signal handling capability				
THD = 10%; m = 0,8	V_i	> typ.	350 400	mV mV
I.F. suppression at V_o = 30 mV	α	> typ.	20 35	dB* dB*
Oscillator voltage				
$V_{9\text{-}16}$ = 8 V; f_{osc} = 1468 kHz	$V_{15\text{-}8}$	typ. <	250 300	mV mV

---

* $\alpha = 20 \log \frac{V_{ia}}{V_{ib}}$, where: V_{ia} is input voltage at f = 468 kHz and V_{ib} is input voltage at f = 1 MHz.


TEA5550
R3
100 Ω
VP
(pin 8)
+
C6
22
nF
R5
2,2 kΩ
C9
100 pF
C11
100 pF
SFT468
C2
22 nF
C4
180
pF
L2
1
2
3
4
6
C1
22 nF
1
2
3
7
6
10
16
14
15
9
11
8
50
Ω
Vi
R1
50 Ω
C5
220 nF
C12
33 µF
C13
100
µF
(25 V)
C14
10 nF
C15
22 nF
R7
22
kΩ
Vo
(a.f.)
R6
1,8 kΩ
Vstab
L1
C8
60 pF
220
pF
C10
470 nF
fosc = 1468 kHz
(VP = 10,2 to 18 V)
7Z84957

Coil data

L1 = 47 µH; Q_o = 100; $N_{1\text{-}3}$ = 35 (0,1 posyn) BR7

L2 = 0,64 mH; Q_o = 110; catalogue no. 3122 138 91481

$N_{1\text{-}3}$ = 146	$N_{1\text{-}2}$ = 33
$N_{2\text{-}3}$ = 113	$N_{4\text{-}6}$ = 9

The transfer impedance of the i.f. filter is:

$Z_{tr} = v_6/i_3 = 850\ \Omega$ ($R_L = 3\ k\Omega$).

Fig. 2 AM test circuit.

APPLICATION INFORMATION

Figures 4 and 7 show the circuit diagrams of single-tuned and double-tuned AM channels respectively, using the TEA5550 and an r.f.-tuning unit (type ALPS). The i.f. filter consists of a single-tuned coil in combination with a ceramic filter (type SFT468).

Typical performance (measured in Figs 4 and 7)

V_P = 14,4 V; T_{amb} = 25 °C; aerial signal conditions: f_o = 1 MHz; m = 0,3; f_m = 1 kHz (dummy aerial as shown in Figs 4 and 7)

		Fig. 4 single-tuning	Fig. 6 double-tuning	
R.F. input voltage for:				
S + N/N = 6 dB	V_i	4	4	μV
S + N/N = 26 dB	V_i	47	49	μV
A.F. output voltage (R_L = R6 = 22 kΩ) V_i = 1 mV	V_o	160	160	mV
Signal-to-noise ratio V_i = 1 mV	S/N	>50	>50	dB
A.G.C. range; change of r.f. input voltage for 10 dB change of a.f. output voltage (reference V_{i1} = 200 mV); see Figs 3 and 10	V_{i1}/V_{i2}	88	88	dB
R.F. signal handling capability THD $<$ 10%; m = 0,8; see Figs 3 and 10	V_i	1,5	1,5	V
Total harmonic distortion (over most of the a.g.c. range); m = 0,8; see Figs 3 and 10	THD	1,2	1,2	%
Oscillator voltage measured across the tank circuit	V_{osc}	250	250	mV
Total selectivity (r.f. and i.f.)	S_9	44	46	dB
Total bandwidth (r.f. and i.f.)	B_{3dB}	4,1	4,4	kHz
I.F. suppression at V_i = 20 μV				
tuned frequency = 600 kHz	α	55	75	dB
= 1600 kHz	α	58	85	dB
Image rejection at V_i = 20 μV				
tuned frequency = 600 kHz		50	72	dB
= 1000 kHz		46	68	dB
= 1400 kHz		42	64	dB
Whistle at V_i = 5 mV				
2 x i.f.-tweet		−40	−40	dB
3 x i.f.-tweet		−48	−48	dB

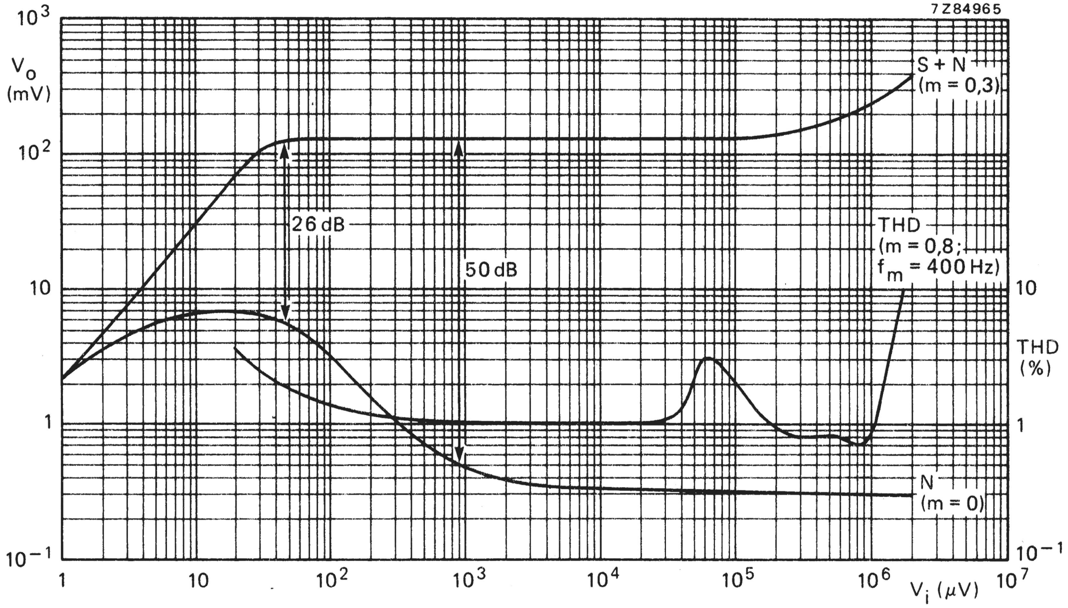


Fig. 3 Typical signal and noise output voltages (V_o is a.f. output voltage) as a function of the input voltage V_i. Also shown is the total harmonic distortion (THD). These curves are for a single-tuned AM channel; the dummy aerial is as shown in Fig. 4; f_o = 1 MHz; f_m = 1 kHz; m = 0,3 (unless otherwise specified).

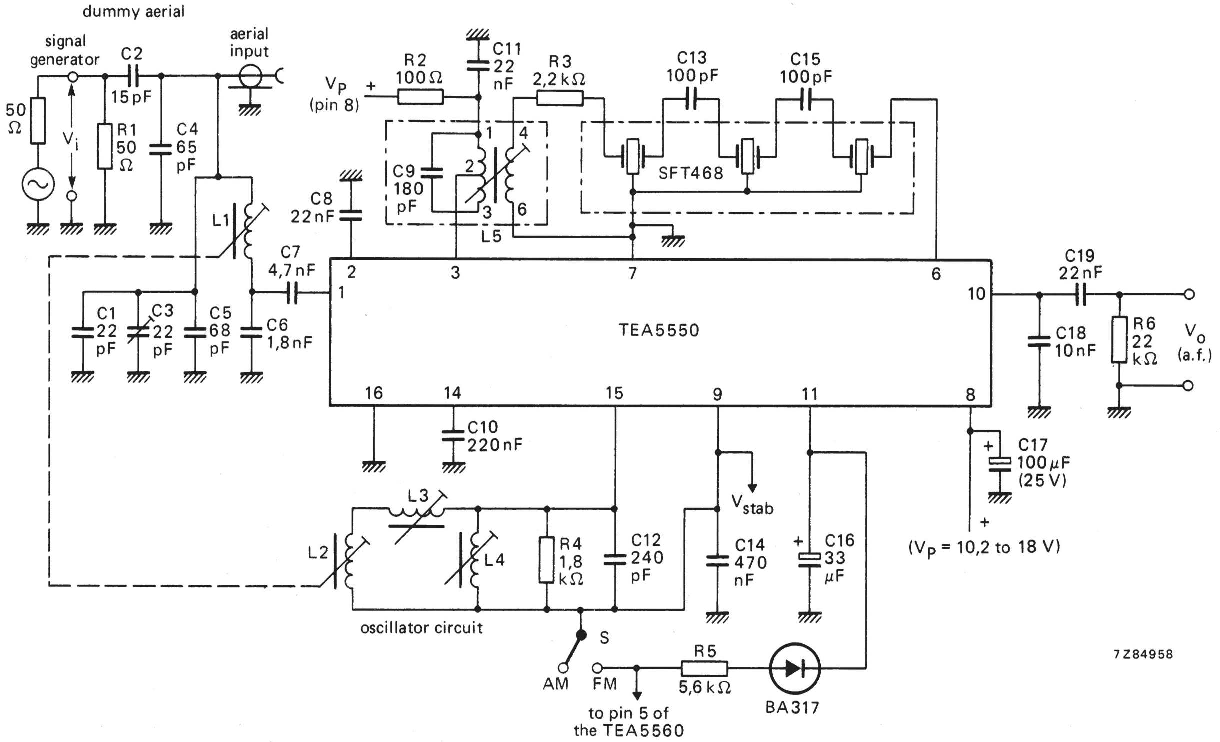

dummy aerial
signal generator
50 Ω
R1 50 Ω
C2 15 pF
C4 65 pF
V_i
aerial input
V_P + (pin 8)
R2 100 Ω
C11 22 nF
R3 2,2 kΩ
C13 100 pF
C15 100 pF
SFT468
C9 180 pF
L5
1
2
3
4
6
C8 22 nF
L1
C7 4,7 nF
C1 22 pF
C3 22 pF
C5 68 pF
C6 1,8 nF
TEA5550
1
2
3
7
6
10
16
14
15
9
11
8
C10 220 nF
C19 22 nF
C18 10 nF
R6 22 kΩ
V_o (a.f.)
C17 100 µF (25 V)
+
+
(V_P = 10,2 to 18 V)
L2
L3
L4
R4 1,8 kΩ
C12 240 pF
V_{stab}
C14 470 nF
C16 33 µF
+
oscillator circuit
S
AM
FM
to pin 5 of the TEA5560
R5 5,6 kΩ
BA317
7Z84958

Fig. 4 Typical application circuit diagram for a single-tuned AM channel in car radio receivers using the TEA5550; S is AM/FM switch; for printed-circuit board see Figs 5 and 6.

Coil data: L1, L2 = tuning coils, ALPS unit MMK IIEII (for coil connections see Fig. 5)
L3 = trimming coil (4,7 µH); catalogue number 3122 138 27460
L4 = padding coil (200 µH); catalogue number 3111 118 23510
L5 = i.f. coil; catalogue number 3122 138 91481

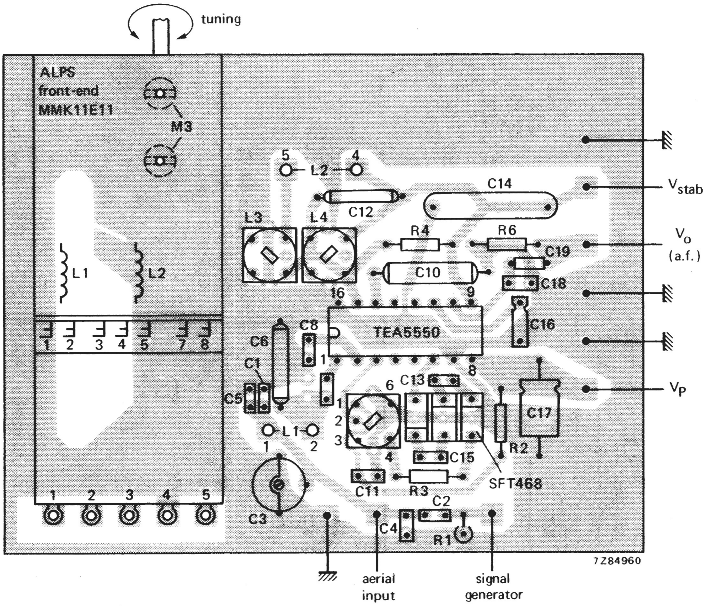

tuning
ALPS
front-end
MMK11E11
M3
L1
L2
1
2
3
4
5
7
8
1
2
3
4
5
5
L2
4
C12
C14
Vstab
L3
L4
R4
R6
Vo
(a.f.)
C19
C10
C18
16
9
TEA5550
C16
C6
C8
1
8
C1
C5
6
C13
1
2
3
4
Vp
C17
L1
1
2
C15
R2
SFT468
C11
R3
C2
C3
C4
R1
7Z84960
aerial
input
signal
generator

Fig. 5 Printed-circuit board component side, showing component layout.
For circuit diagram see Fig. 4.

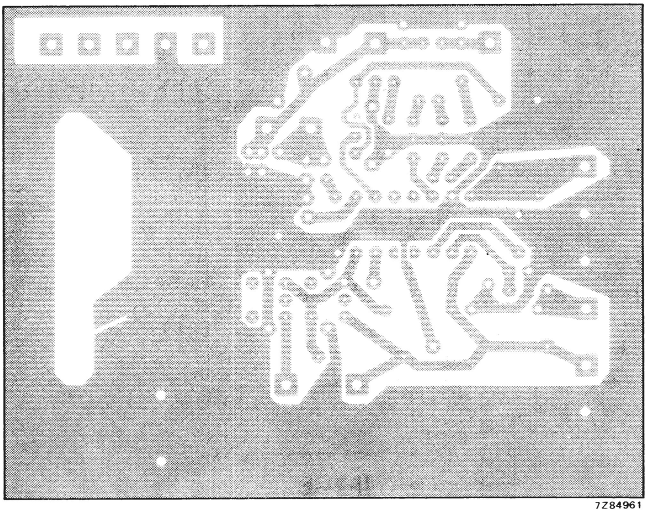


Fig. 6 Printed-circuit board showing track side.

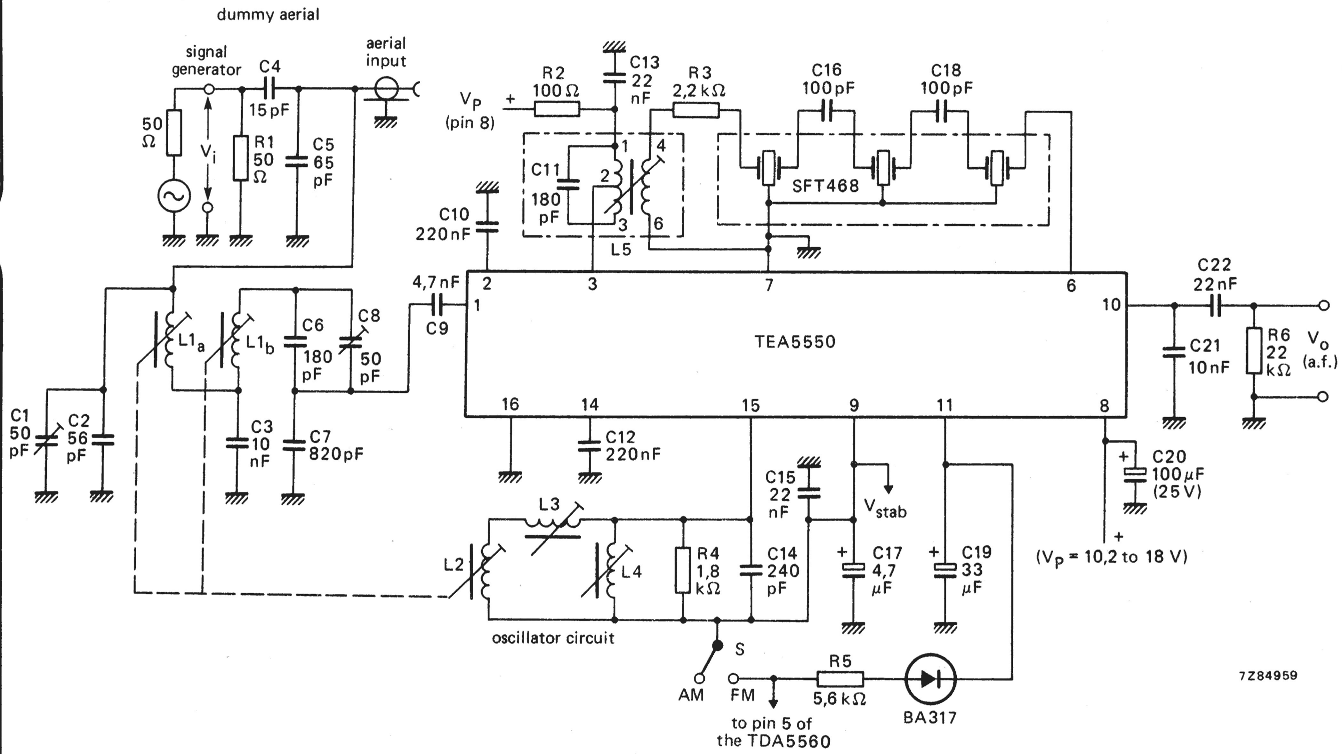

dummy aerial
signal generator
50 Ω
V_i
C4 15 pF
R1 50 Ω
C5 65 pF
aerial input
V_P + (pin 8)
R2 100 Ω
C13 22 nF
R3 2,2 kΩ
C16 100 pF
C18 100 pF
SFT468
C11 180 pF
L5
1
2
3
4
6
C10 220 nF
4,7 nF
C9
TEA5550
2
3
7
6
10
1
16
14
15
9
11
8
C22 22 nF
C21 10 nF
R6 22 kΩ
V_o (a.f.)
$L1_a$
$L1_b$
C6 180 pF
C8 50 pF
C1 50 pF
C2 56 pF
C3 10 nF
C7 820 pF
C12 220 nF
C15 22 nF
V_{stab}
C20 100 μF (25 V)
+
(V_P = 10,2 to 18 V)
L2
L3
L4
R4 1,8 kΩ
C14 240 pF
C17 4,7 μF
C19 33 μF
oscillator circuit
S
AM
FM
R5 5,6 kΩ
BA317
to pin 5 of the TDA5560
7Z84959

Fig. 7 Typical application circuit diagram for a double-tuned AM channel in car radio receivers using the TEA5550; S is AM/FM switch; for printed-circuit board see Figs 8 and 9.

Coil data: $L1_a$, $L1_b$, L2 = tuning coils, ALPS unit MMK IIEII (for coil connections see Fig. 8)
L3 = trimming coil (4,7 μH); catalogue number 3122 138 27460
L4 = padding coil (200 μH); catalogue number 3111 118 23510
L5 = i.f. coil; catalogue number 3122 138 91481

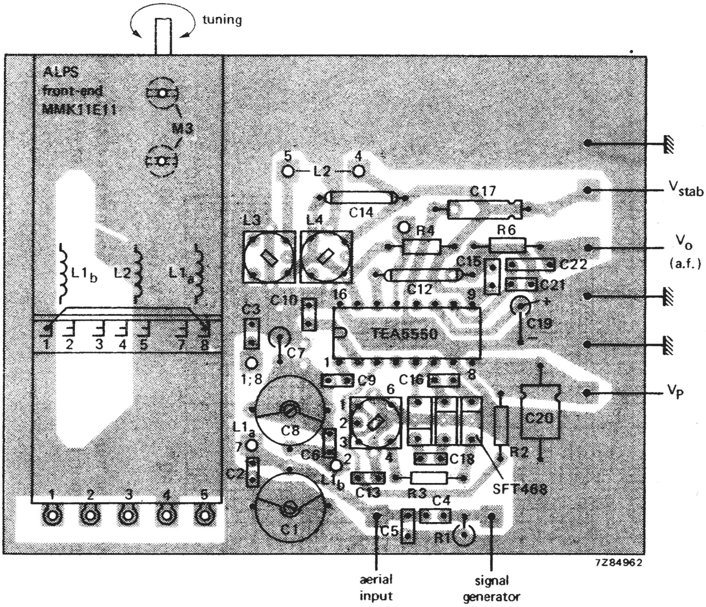

tuning
ALPS
front-end
MMK11E11
M3
L1b
L2
L1a
1
2
3
4
5
7
8
5
L2
4
C14
C17
L3
L4
R4
R6
C15
C22
C12
C21
C10
16
9
C3
TEA5550
C19
+
−
C7
1
8
1;8
C9
C16
6
L1a
C8
1
2
3
C20
7
C6
2
4
C18
R2
C2
L1b
C13
R3
SFT468
C4
C1
C5
R1
1
2
3
4
5
Vstab
Vo
(a.f.)
VP
7Z84962
aerial
input
signal
generator

Fig. 8 Printed-circuit board component side, showing component layout.
For circuit diagram see Fig. 7.

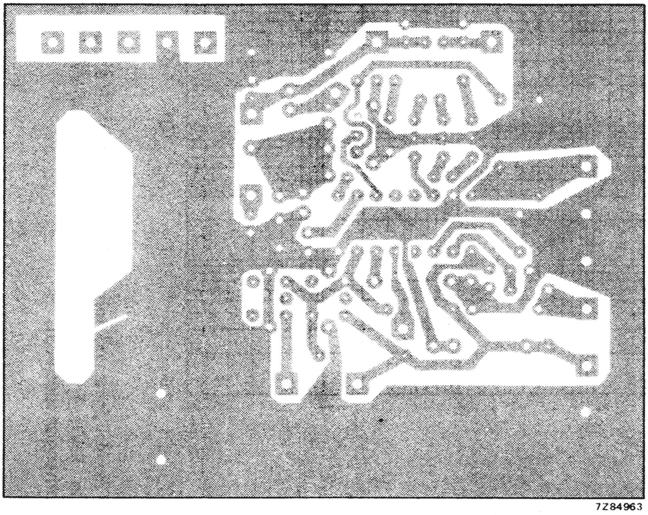


Fig. 9 Printed-circuit board showing track side.

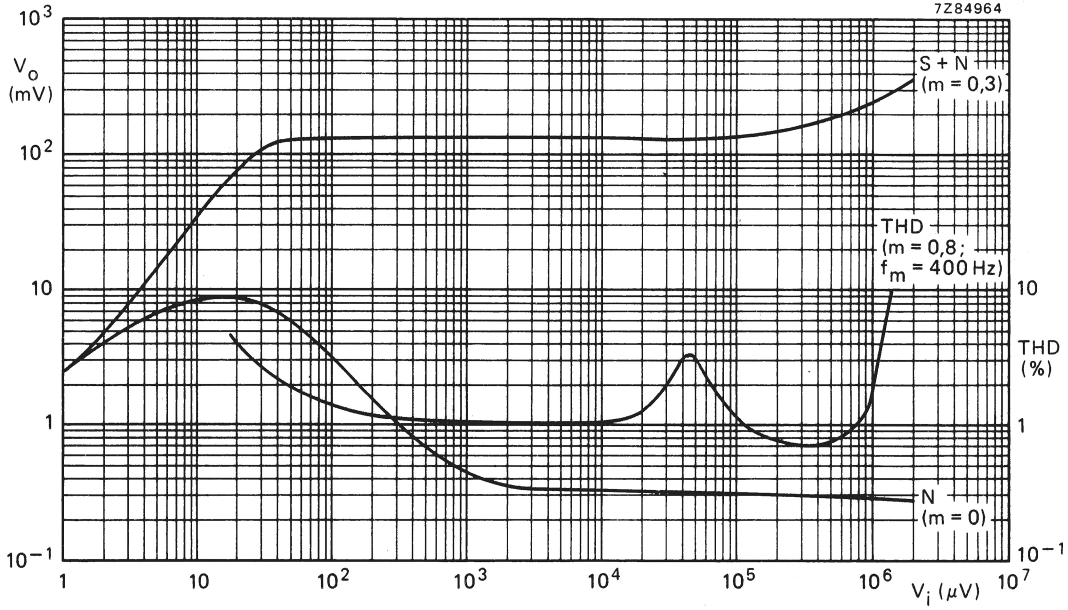


Fig. 10 Typical signal and noise output voltages (V_o is a.f. output voltage) as a function of the input voltage V_i. Also shown is the total harmonic distortion (THD). These curves are for a double-tuned AM channel; the dummy aerial is shown in Fig. 7; f_o = 1 MHz; f_m = 1 kHz; m = 0,3 (unless otherwise specified).

FM/IF SYSTEM

GENERAL DESCRIPTION

The TEA5560 is a monolithic integrated FM/IF system circuit, intended for car radios and home-receivers equipped with a ratio detector.

The system incorporates the following functions:

- a three-stage i.f. limiting amplifier
- a 15 dB field-strength dependent muting circuit
- a field-strength dependent d.c. voltage for e.g.:
  mono/stereo switching
  channel separation control of a stereo decoder
  an indicator ($I_{max} \leqslant 1$ mA)
- standby ON/OFF switching circuit
- a voltage stabilizer, for the internal circuit current and an external current up to 15 mA
- adjustable gain ($\Delta G = 15$ dB)

QUICK REFERENCE DATA

Supply voltage range (pin 6)	V_P		10,2 to 18	V
Ambient temperature	T_{amb}	typ.	25	°C
Supply voltage (pin 6)	V_P	typ.	14,4	V
Frequency	f_o		10,7	MHz
Sensitivity (3 dB limiting)	V_i	typ.	150	µV
Signal-to-noise ratio for $V_i = 10$ mV	S/N	typ.	80	dB
A.F. output voltage at $\Delta f = \pm 22{,}5$ kHz	V_o	typ.	200	mV
Total harmonic distortion; $\Delta f = \pm 22{,}5$ kHz	THD	typ.	0,3	%
A.M. suppression AM signal: $m = 0{,}3$; $f_m = 1$ kHz FM signal: $\Delta f = \pm 22{,}5$ kHz; $f_m = 70$ Hz for $V_i = 1$ mV	AMS	typ.	50	dB

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142). The tab (on top of the package) is connected to pin 9.

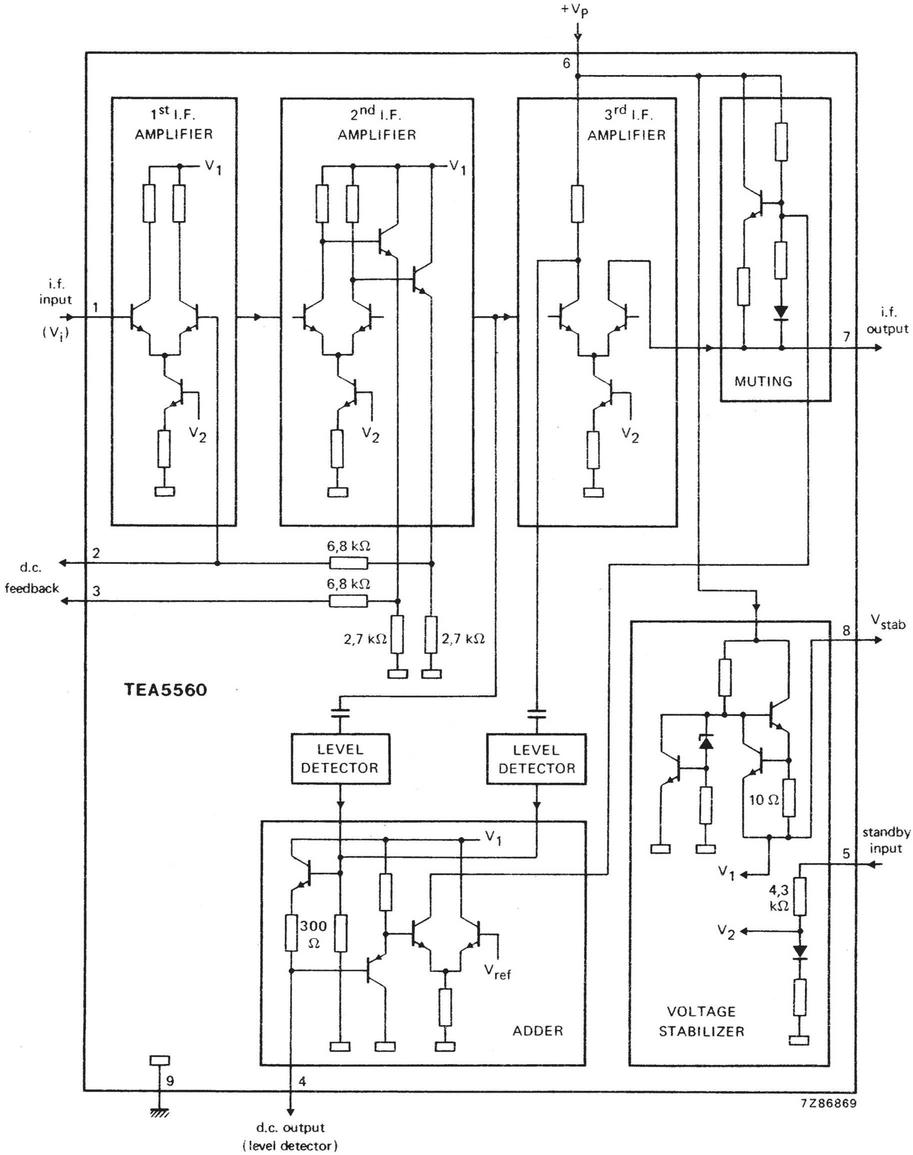

+VP
6
1st I.F. AMPLIFIER
2nd I.F. AMPLIFIER
3rd I.F. AMPLIFIER
MUTING
V1
V2
i.f. input
(Vi)
1
i.f. output
7
d.c. feedback
2
3
6,8 kΩ
6,8 kΩ
2,7 kΩ
2,7 kΩ
TEA5560
Vstab
8
LEVEL DETECTOR
LEVEL DETECTOR
300 Ω
Vref
ADDER
10 Ω
standby input
5
4,3 kΩ
VOLTAGE STABILIZER
9
4
d.c. output (level detector)
7Z86869

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages				
pin 6	$V_P = V_{6\text{-}9}$	max.	24	V
pin 7	$V_{7\text{-}9}$	max.	24	V
Voltage at pin 4	$V_{4\text{-}9}$	max.	6	V
Voltage at pin 5	$V_{5\text{-}9}$	max.	9	V
Non-repetitive peak output current (pin 8)	$-I_{8SM}$	max.	100	mA
Total power dissipation	P_{tot}	max.	1000	mW
Storage temperature range	T_{stg}	−55 to + 150		°C
Operating ambient temperature range	T_{amb}	−30 to +85		°C

THERMAL RESISTANCE

From junction to ambient (in free air) $R_{th\ j\text{-}amb}$ = 75 K/W

D.C. CHARACTERISTICS

V_P = 14,4 V; T_{amb} = 25 °C; measured in Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 6)					
Supply voltage *	$V_P = V_{6-9}$	10,2	14,4	18,0	V
Voltages					
at pin 8; $-I_8 = 0$ **	V_{8-9}	7,5	8,0	8,5	V
at pin 8 when $-I_8$ increases from 0 to 15 mA	ΔV_{8-9}	–	200	300	mV
at pin 8 when V_P reduces from 14,4 V to 10,2 V	ΔV_{8-9}	–	–	1,0	V
at pin 8 when V_P increases from 14,4 V to 18,0 V	ΔV_{8-9}	–	–	200	mV
at pin 4 (level detector)	V_{4-9}	–	–	100	mV
at pins 1, 2 and 3	$V_{1,2,3-9}$	–	2,4	–	V
Currents					
Total supply current; $-I_8 = 0$	I_{tot}	15	20	30	mA
Current supplied from pin 8	$-I_8$	–	–	15	mA
Stand-by current; $V_{5-9} = 0$	I_{sb}	8	11	14	mA
Current into pin 5	I_5	1,0	1,5	2,0	mA
Current into pin 7	I_7	–	3,0	–	mA
Power consumption					
at $-I_8 = 0$	P	–	300	–	mW

---

* A stabilized supply voltage of 7 to 9 V can also be applied at pin 5 and 6 (linked); for this application pin 8 must not be connected.

** The temperature coefficient of the stabilized voltage at pin 8 is typical −2,3 mV/K.

A.C. CHARACTERISTICS

V_P = 14,4 V; T_{amb} = 25 °C; V_i = 1 mV; f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 1 kHz; measured in Fig. 2; unless otherwise specified

parameter	symbpl	min.	typ.	max.	unit
I.F. part and ratio detector					
Sensitivity					
at –3 dB before limiting (pin 1); (without muting) *	V_i	105	150	210	µV
Signal-to-noise S + N/S measured in a bandwidth of 60 Hz to 15 kHz					
at V_i = 20 µV	S/N	40	45	–	dB
at V_i = 150 µV	S/N	–	65	–	dB
at V_i = 1 mV	S/N	–	78	–	dB
at V_i = 10 mV	S/N	–	80	–	dB
A.F. output voltage					
Δf = ± 22,5 kHz	V_o	–	200	–	mV
Δf = ± 75 kHz	V_o	–	600	–	mV
Total harmonic distortion					
Δf = ± 22,5 kHz	THD	–	0,3	–	%
Δf = ± 75 kHz	THD	–	2,0	–	%
AM suppression					
f_m = 1 kHz; m = 0,3 (for AM)					
f_m = 70 kHz; Δf = ± 22,5 kHz (for FM)					
at V_i = 150 µV	AMS	–	40	–	dB
at V_i = 1 mV	AMS	–	50	–	dB
at V_i = 10 mV	AMS	–	55	–	dB
Level detector circuit					
D.C. output voltage (pin 4)					
at V_i = 200 µV	$V_{4\text{-}9}$	–	1,9	–	V
at V_i = 500 µV	$V_{4\text{-}9}$	–	2,8	–	V
at V_i = 1 mV	$V_{4\text{-}9}$	–	3,5	–	V
at V_i = 3 mV	$V_{4\text{-}9}$	–	5,0	–	V
at V_i = 10 mV	$V_{4\text{-}9}$	–	5,7	–	V
Muting circuit (see also Fig. 5)					
Change in output voltage at V_i = 3 µV (with and without muting) *	α_{vo}	10	15	–	dB
Input voltage at a change in output voltage of ≤ 1 dB* (V_i at α_{vo} ≤ 1 dB)	V_i	–	–	250	µV

---

* With muting $V_{4\text{-}9} < 0{,}3$ V; without muting $V_{4\text{-}9}$ = 1,2 to 6 V.

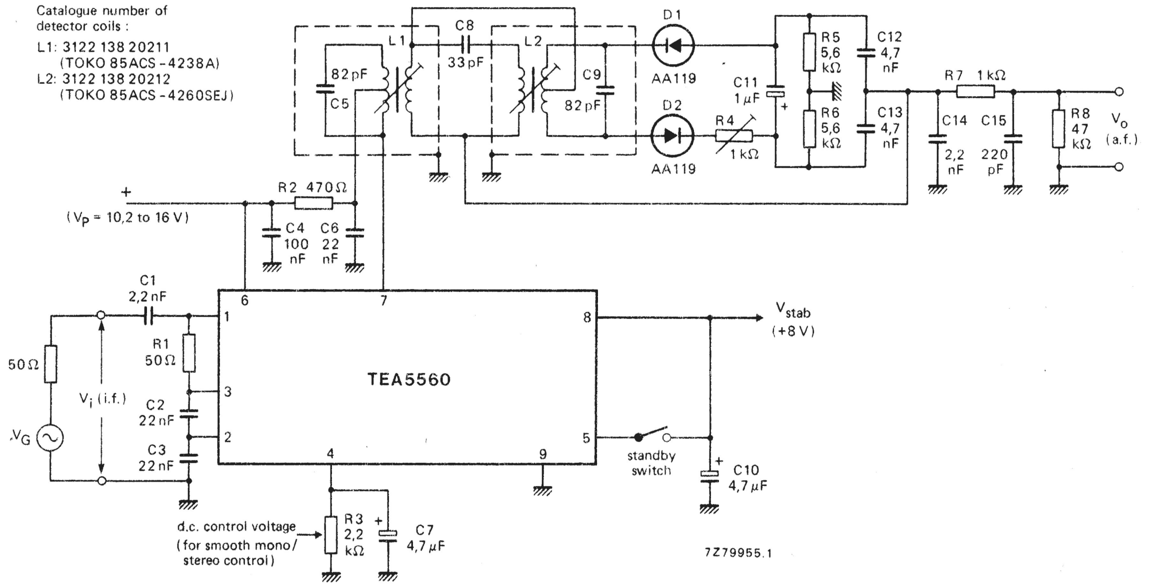

Catalogue number of detector coils :
L1: 3122 138 20211 (TOKO 85ACS-4238A)
L2: 3122 138 20212 (TOKO 85ACS-4260SEJ)
C5 82 pF
L1
C8 33 pF
L2
C9 82 pF
D1 AA119
D2 AA119
C11 1 μF
R4 1 kΩ
R5 5,6 kΩ
R6 5,6 kΩ
C12 4,7 nF
C13 4,7 nF
R7 1 kΩ
C14 2,2 nF
C15 220 pF
R8 47 kΩ
V$_o$ (a.f.)
+
(V$_P$ = 10,2 to 16 V)
R2 470 Ω
C4 100 nF
C6 22 nF
C1 2,2 nF
R1 50 Ω
C2 22 nF
C3 22 nF
50 Ω
V$_G$
V$_i$ (i.f.)
TEA5560
1
2
3
4
5
6
7
8
9
V$_{stab}$ (+8 V)
standby switch
C10 4,7 μF
d.c. control voltage (for smooth mono/stereo control)
R3 2,2 kΩ
C7 4,7 μF
7Z79955.1

Fig. 2 FM test circuit.

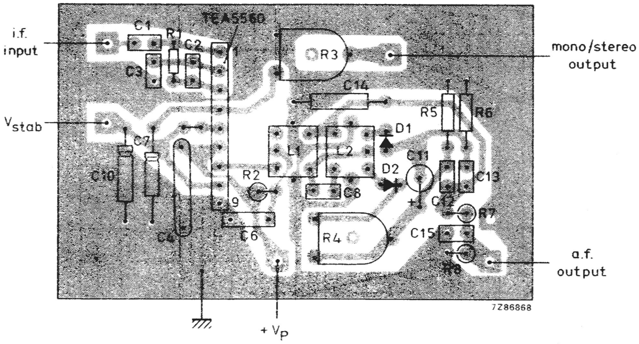

i.f. input
TEA5560
C1
R1
C2
C3
1
R3
mono/stereo output
C14
R5
R6
V_stab
D1
C7
L1
L2
C11
C10
D2
C13
R2
C8
9
C12
R7
C4
C6
R4
C15
R8
a.f. output
+V_P
7Z86868

Fig. 3 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 2.

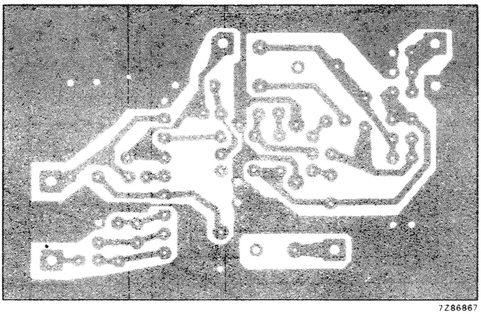
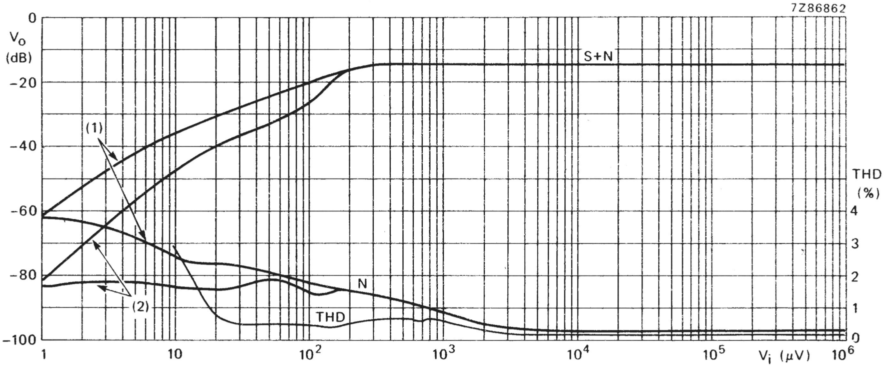


Fig. 4 Printed-circuit board showing track side.



(1) Without muting.
(2) With muting.

Fig. 5 A.F. output voltage (V_o); reference level 0 dB = 1 V, and the total harmonic distortion (THD) as a function of the i.f. input voltage (V_i). Measured in the test circuit Fig. 2 at $\Delta f = \pm$ 22,5 kHz; f_m = 1 kHz.

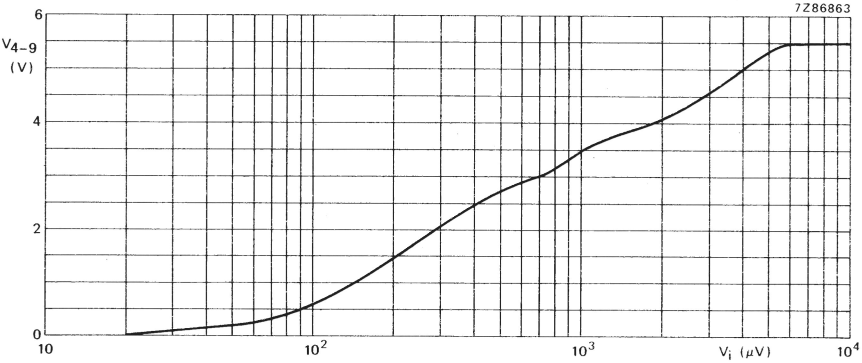
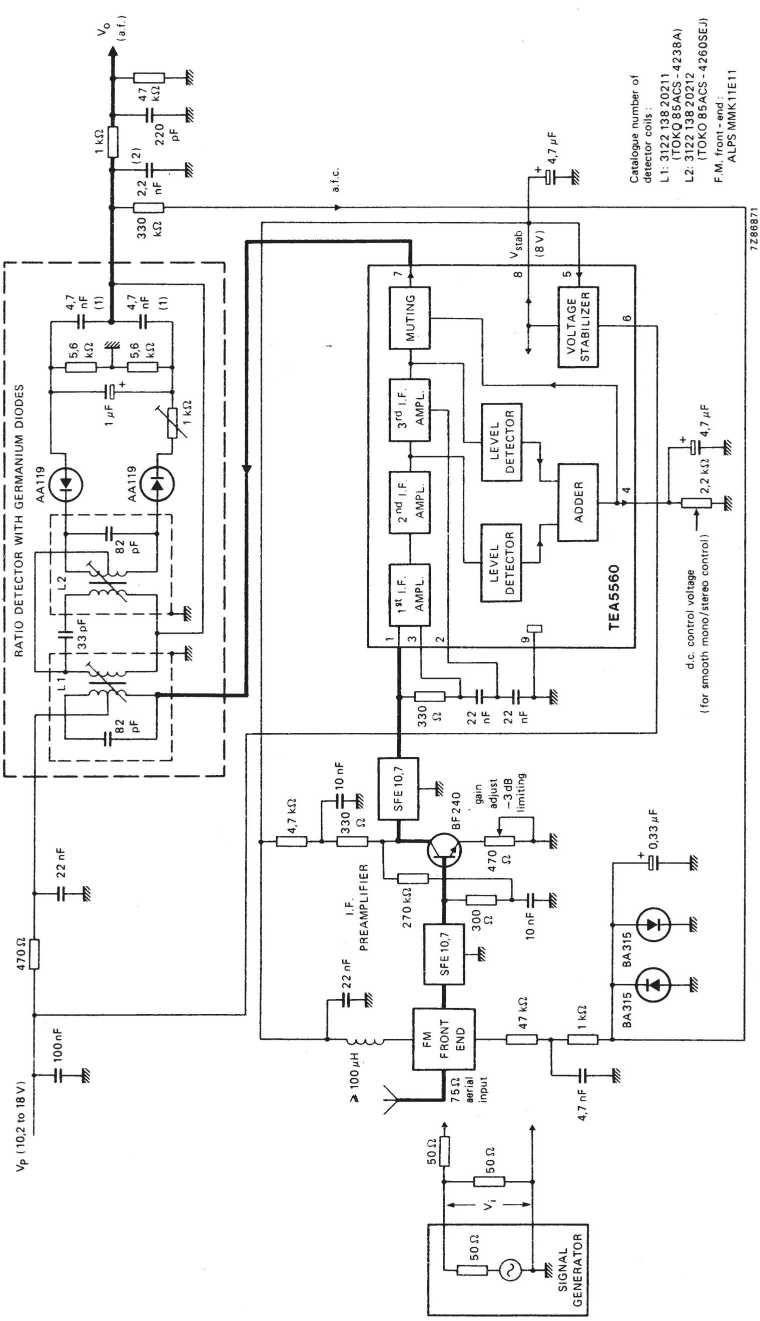


Fig. 6 Level detector d.c. output voltage (pin 4) as a function of the i.f. input voltage. Measured in test circuit Fig. 2.

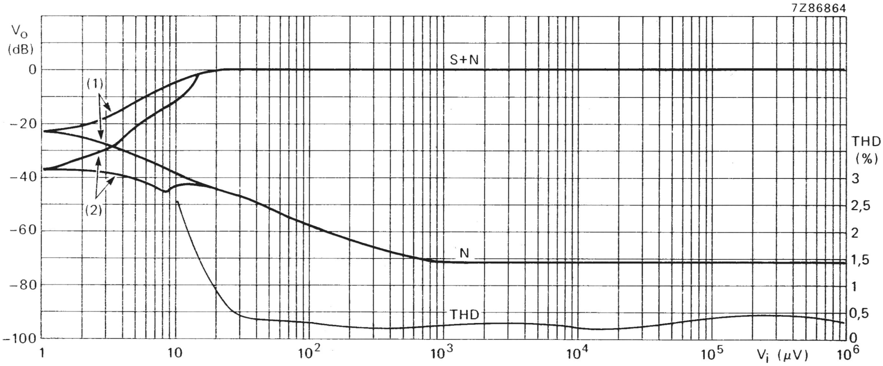
APPLICATION INFORMATION


Vo (a.f.)
47 kΩ
220 pF
1 kΩ
(2)
2,2 nF
330 kΩ
a.f.c.
4,7 µF
Catalogue number of detector coils:
L1: 3122 138 20211 (TOKO 85ACS-4238A)
L2: 3122 138 20212 (TOKO 85ACS-4260SEJ)
F.M. front-end: ALPS MMK11E11
7Z86871
RATIO DETECTOR WITH GERMANIUM DIODES
4,7 nF (1)
5,6 kΩ
1 µF
1 kΩ
AA119
82 pF
L2
33 pF
L1
Vstab (8 V)
8
5
7
MUTING
VOLTAGE STABILIZER
6
3rd I.F. AMPL.
2nd I.F. AMPL.
1st I.F. AMPL.
LEVEL DETECTOR
ADDER
4
TEA5560
1
3
2
9
2,2 kΩ
d.c. control voltage (for smooth mono/stereo control)
330 Ω
22 nF
SFE 10,7
10 nF
BF 240
gain adjust −3 dB limiting
470 Ω
4,7 kΩ
270 kΩ
300 Ω
I.F. PREAMPLIFIER
0,33 µF
BA315
22 nF
470 Ω
100 nF
Vp (10,2 to 18 V)
FM FRONT END
≥ 100 µH
75 Ω aerial input
47 kΩ
4,7 nF
50 Ω
Vi
SIGNAL GENERATOR

(1) Stereo application 220 pF.
(2) Stereo application 390 pF.

Fig. 7 FM channel for (car) radios using the TEA5560 and a ratio detector with AA119 germanium diodes.

APPLICATION INFORMATION (continued)



(1) Without muting.
(2) With muting.

Fig. 8 Signal and noise (S + N) and noise (N); reference level 0 dB = 200 mV, and the total harmonic distortion (THD) as a function of the aerial input voltage (V_i). Measured in application circuit Fig. 7 at $\Delta f = \pm$ 22,5 kHz; f_m = 1 kHz.

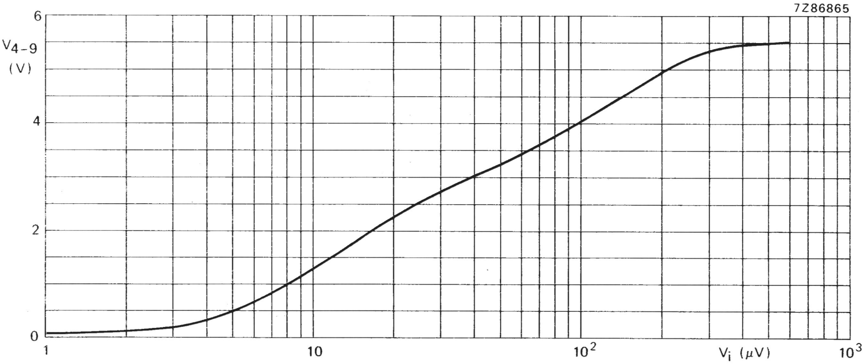
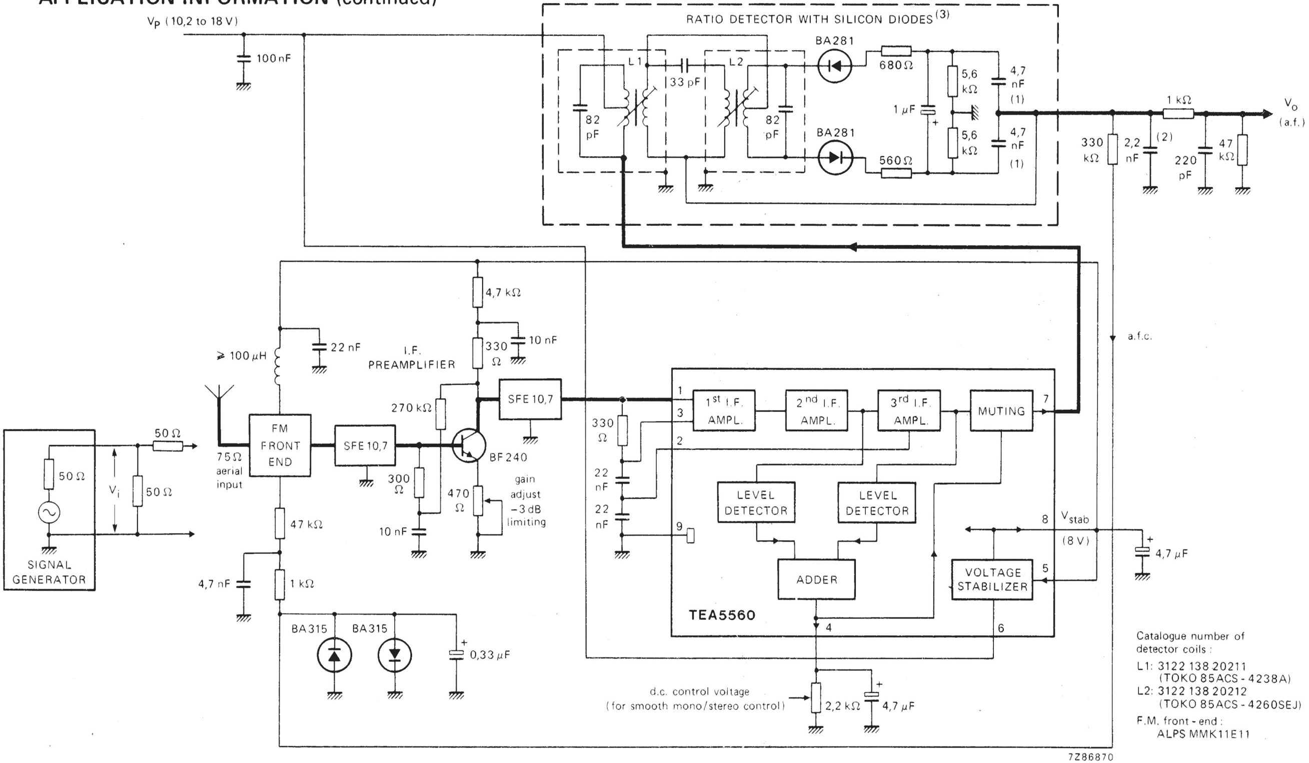


Fig. 9 Level detector d.c. output voltage (pin 4) as a function of the aerial input voltage. Measured in application circuit Fig. 7.

APPLICATION INFORMATION (continued)


V_P (10,2 to 18 V)
100 nF
RATIO DETECTOR WITH SILICON DIODES (3)
L1
L2
33 pF
82 pF
82 pF
BA281
BA281
680 Ω
560 Ω
1 μF
5,6 kΩ
5,6 kΩ
4,7 nF (1)
4,7 nF (1)
1 kΩ
V_o (a.f.)
330 kΩ
2,2 nF (2)
220 pF
47 kΩ
a.f.c.
4,7 kΩ
10 nF
330 Ω
22 nF
≥ 100 μH
I.F. PREAMPLIFIER
270 kΩ
SFE 10,7
SFE 10,7
FM FRONT END
75 Ω aerial input
BF 240
300 Ω
470 Ω
gain adjust −3 dB limiting
10 nF
50 Ω
50 Ω
50 Ω
V_i
SIGNAL GENERATOR
47 kΩ
4,7 nF
1 kΩ
BA315
BA315
0,33 μF
330 Ω
22 nF
22 nF
1st I.F. AMPL.
2nd I.F. AMPL.
3rd I.F. AMPL.
MUTING
LEVEL DETECTOR
LEVEL DETECTOR
ADDER
VOLTAGE STABILIZER
TEA5560
1
2
3
4
5
6
7
8
9
V_stab (8 V)
4,7 μF
d.c. control voltage (for smooth mono/stereo control)
2,2 kΩ
4,7 μF
7Z86870

Catalogue number of detector coils:
L1: 3122 138 20211
(TOKO 85ACS - 4238A)
L2: 3122 138 20212
(TOKO 85ACS - 4260SEJ)
F.M. front-end:
ALPS MMK11E11

(1) Stereo application 220 pF.

(2) Stereo application 390 pF.

(3) Further detailed information of using silicon diodes is available on request.

Fig. 10 FM channel for (car) radios using the TEA5560 and a ratio detector with BA281 silicon diodes.

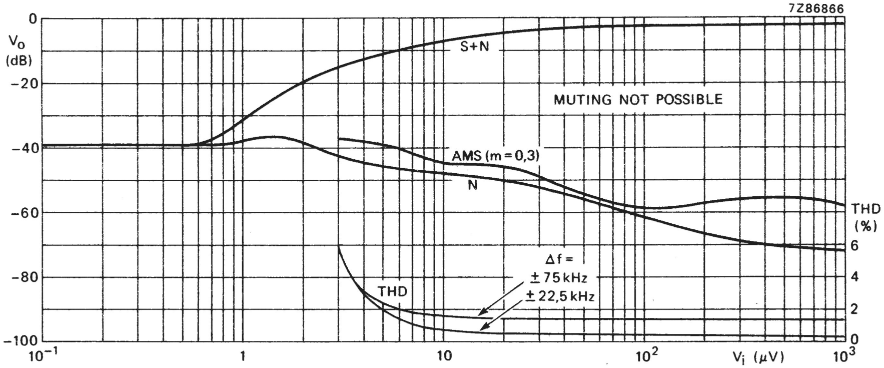


Fig. 11 Signal and noise (S + N) and noise (N); reference level 0 dB = 245 mV, AM suppression (AMS) and total harmonic distortion (THD) as a function of the aerial input voltage (V_i). Measured in application circuit Fig. 10 at Δf = ± 22,5 kHz; f_m = 1 kHz; for AM suppression m = 0,3; Δf = ± 22,5 kHz.

AM/FM RADIO RECEIVER CIRCUIT

GENERAL DESCRIPTION

The TEA5570 is a monolithic integrated radio circuit for use in portable receivers and clock radios. The IC is also applicable to mains-fed AM and AM/FM receivers and car radio-receivers. Apart from the AM/FM switch function the IC incorporates for AM a double balanced mixer, 'one-pin' oscillator, i.f. amplifier with a.g.c. and detector, and a level detector for tuning indication. The FM circuitry comprises i.f. stages with a symmetrical limiter for a ratio detector. A level detector for mono/stereo switch information and/or indication complete the FM part.

Features

- Simple d.c. switching for AM to FM by only one d.c. contact to ground (no switch contacts in the i.f. channel, a.f. or level detector outputs)
- AM and FM gain control
- Low current consumption (I_{tot} = 6 mA)
- Low voltage operation (V_P = 2,7 to 9 V)
- Ability to handle large AM signals; good i.f. suppression
- Applicable for inductive, capacitive and diode tuning
- Double smoothing of a.g.c. line
- Short-wave range up to 30 MHz
- Lumped or distributed i.f. selectivity with coil and/or ceramic filters
- AM and a.g.c. output voltage control
- Distribution of PCB wiring provides good frequency stability
- Economic design for 'AM only' receivers

QUICK REFERENCE DATA (at T_{amb} = 25 °C)

Supply voltage	$V_P = V_{7-16}$	typ.	5,4	V
Supply current	I_7	typ.	6,2	mA
AM performance (pin 2) for m = 0,3				
Sensitivity				
at V_o = 10 mV	V_i	typ.	1,7	μV
at S/N = 26 dB	V_i	typ.	16	μV
A.F. output voltage at V_i = 1 mV	V_o	typ.	100	mV
Total harmonic distortion at V_i = 1 mV	THD	typ.	0,5	%
FM performance (pin 1) for $\Delta f = \pm$ 22,5 kHz				
limiting sensitivity, −3 dB	V_i	typ.	110	μV
Signal-to-noise ratio for V_i = 1 mV	S/N	typ.	65	dB
A.F. output voltage at V_i = 1 mV	V_o	typ.	100	mV
Total harmonic distortion at V_i = 1 mV	THD	typ.	0,3	%
AM suppression at V_i = 10 mV	AMS	typ.	50	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

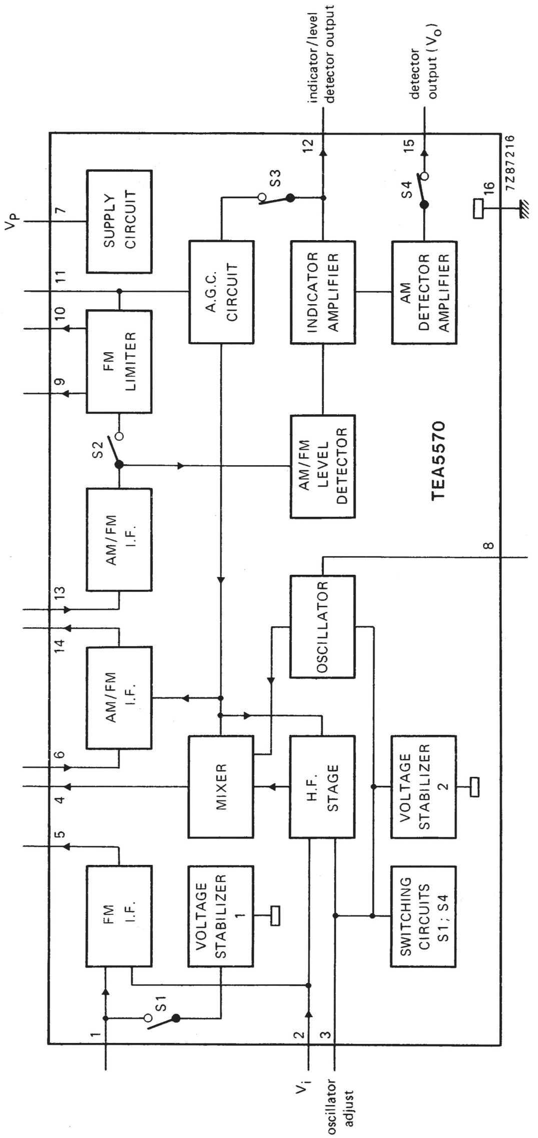

indicator/level detector output
detector output (V_o)
12
15
S3
S4
16
7Z87216
V_P
7
SUPPLY CIRCUIT
11
10
9
FM LIMITER
A.G.C. CIRCUIT
INDICATOR AMPLIFIER
AM DETECTOR AMPLIFIER
S2
AM/FM LEVEL DETECTOR
TEA5570
AM/FM I.F.
13
14
8
OSCILLATOR
AM/FM I.F.
6
4
5
MIXER
H.F. STAGE
VOLTAGE STABILIZER 2
FM I.F.
VOLTAGE STABILIZER 1
SWITCHING CIRCUITS S1; S4
S1
1
2
3
V_i
oscillator adjust

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 7)	$V_P = V_{7\text{-}16}$	max.	12 V
Voltage at pins 4, 5, 9 and 10 to pin 16 (ground)	$V_{n\text{-}16}$	max.	12 V
Voltage range at pin 8	$V_{8\text{-}16}$		$V_P \pm 0,5$ V
Current into pin 5	I_5	max.	3 mA
Total power dissipation	P_{tot}	see Fig. 2	
Storage temperature range	T_{stg}	−55 to +150	°C
Operating ambient temperature range	T_{amb}	−30 to +85	°C

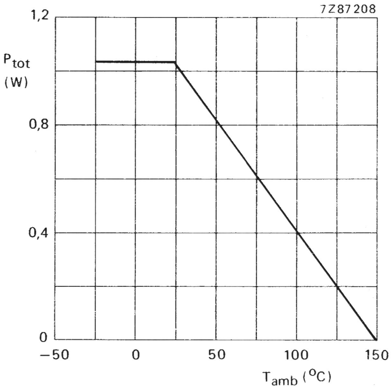


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

V_P = 6 V; T_{amb} = 25 °C; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 7)					
Supply voltage (note 1)	$V_P = V_{7\text{-}16}$	2,4	5,4	9,0	V
Voltages					
at pin 1 (FM)	$V_{1\text{-}16}$	–	1,42	–	V
at pin 1; $-I_1$ = 50 μA (FM)	$V_{1\text{-}16}$	–	1,28	–	V
at pins 2 and 3 (AM)	$V_{2,3\text{-}16}$	–	1,42	–	V
at pin 6	$V_{6\text{-}16}$	–	0,7	–	V
at pin 11	$V_{11\text{-}16}$	–	1,4	–	V
at pin 13	$V_{13\text{-}16}$	–	0,7	–	V
at pin 14	$V_{14\text{-}16}$	–	4,3	–	V
Currents					
Supply current	I_7	4,2	6,2	8,2	mA
Current supplied from pin 1 (FM)	$-I_1$	–	–	50	μA
Current supplied from pin 12	$-I_{12}$	–	–	20	μA
Current supplied from pin 15	$-I_{15}$	–	30	–	μA
Current into pin 4 (AM)	I_4	–	0,6	–	mA
Current into pin 5 (FM) (note 4)	I_5	–	0,35	–	mA
Current into pin 8 (AM)	I_8	–	0,3	–	mA
Current into pins 9, 10 (FM)	$I_{9,10}$	–	0,65	–	mA
Current into pin 14	I_{14}	–	0,4	–	mA
Power consumption	P	–	40	–	mW

A.C. CHARACTERISTICS

AM performance

V_P = 6 V; T_{amb} = 25 °C; r.f. condition: f_i = 1 MHz, m = 0,3, f_m = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/I_4$ = 2,7 kΩ; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
R.F. sensitivity (pin 2)					
at V_o = 30 mV	V_i	3,5	5,0	7,0	μV
at S + N/N = 6 dB	V_i	—	1,3		μV
at S + N/N = 26 dB	V_i	—	16	20	μV
at S + N/N = 50 dB	V_i	—	1	—	mV
Signal handling (THD ≤ 10% at m = 0,8)	V_i	200	—	—	mV
A.F. output voltage at V_i = 1 mV	V_o	80	100	125	mV
Total harmonic distortion					
at V_i = 100 μV to 100 mV (m = 0,3)	THD	—	0,5	—	%
at V_i = 2 mV (m = 0,8)	THD	—	1,0	2,5	%
at V_i = 200 mV (m = 0,8)	THD	—	4,0	10	%
I.F. suppression at V_o = 30 mV (note 2)	α	26	35	—	dB
Oscillator voltage (pin 8; note 3)					
at f_{osc} = 1455 kHz	$V_{8\text{-}16}$	120	160	200	mV
Indicator current (pin 12) at V_i = 1 mV	I_{12}	—	200	230	μA

FM performance

V_P = 6 V; T_{amb} = 25 °C; i.f. condition: f_i = 10,7 MHz, Δf = ± 22,5 kHz, f_m = 1 kHz; transfer impedance of the i.f. filter $|Z_{tr}| = v_6/i_5$ = 275 Ω; measured in Fig. 10; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
I.F. part					
I.F. sensitivity (adjustable; note 4)					
Input voltage					
at −3 dB before limiting	V_i	90	110	130	μV
at S + N/N = 26 dB	V_i	—	6	—	μV
at S + N/N = 65 dB	V_i	—	1	—	mV
A.F. output voltage at V_i = 1 mV	V_o	80	100	125	mV
Total harmonic distortion at V_i = 1 mV	THD	—	0,3	—	%
AM suppression (note 5)	AMS	—	50	—	dB
Indicator/level detector (pin 12)					
Indicator current	I_{12}	—	250	325	μA
D.C. output voltage					
at V_i = 300 μV	$V_{12\text{-}16}$	—	0,25	—	V
at V_i = 2 mV	$V_{12\text{-}16}$	—	1,0	—	V
AM to FM switch					
Switching current at $V_{3\text{-}16}$ < 1 V	$-I_3$	—	—	400	μA

Notes to characteristics

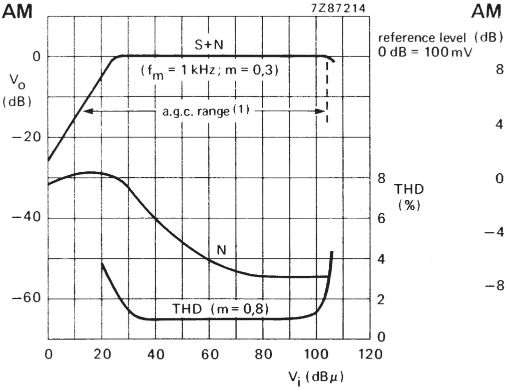
1. Oscillator operates at $V_{7\text{-}16} > 2{,}25$ V.
2. I.F. suppression is defined as the ratio $\alpha = 20 \log \frac{V_{i1}}{V_{i2}}$ where: V_{i1} is the input voltage at f = 455 kHz and V_{i2} is the input voltage at f = 1 MHz.
3. Oscillator voltage at pin 8 can be preset by R_{osc} (see Fig. 10).
4. Maximum current into pin 5 can be adjusted by R1 (see Fig. 10); $I_5 = \frac{V_{3\text{-}16}}{R1} - I_3$ when $V_{3\text{-}16} = 800$ mV; $I_3 = 400\ \mu A$.
5. AM suppression is measured with $f_m = 1$ kHz, m = 0,3 for AM; $f_m = 400$ Hz, $\Delta f = \pm 22{,}5$ kHz for FM.

Facility adaptation

Facility adaptation is achieved as follows (see Fig. 10):

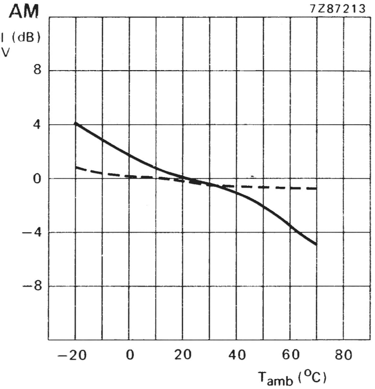
Facility	Component
FM sensitivity	R1 fixes the current at pin 5 ($I_5 = \frac{V_{3\text{-}16}}{R1} - 400\ \mu A$) (gain adjustable ± 10 dB; see note 4)
AM sensitivity	R11 and coil tapping
AM oscillator biasing	R_{osc}
AM output voltage	R7, R11
AM a.g.c. setting	R7

Typical graphs



(1) A.G.C. range (figure of merit, FOM).

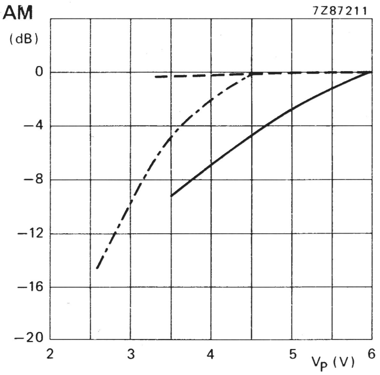
Fig. 3 Signal, noise and distortion as a function of input voltage (V_i). Measured at f_i = 1 MHz in test circuit Fig. 10.



——— sensitivity (V_i) at V_o = 30 mV; m = 0,3.

– – – – output voltage (V_o) at V_i = 2 mV; m = 0,3.

Fig. 4 Sensitivity (V_i), output voltage (V_o) as a function of temperature behaviour (T_{amb}). Measured at f_i = 1 MHz in test circuit Fig. 10.



——— sensitivity (V_i) at V_o = 30 V; m = 0,3: 6,0 V application.

—·—·— sensitivity (V_i) at V_o = 30 mV; m = 0,3: 4,5 V application.

– – – – output voltage (V_o) at V_i = 0,2 mV; m = 0,3.

Fig. 5 Sensitivity (V_i) and output voltage (V_o) as a function of supply voltage (V_P). Measured at f_i = 1 MHz in test circuit Fig. 10, for application V_P = 6 V. Also shown is the sensitivity for V_P = 4,5 V application (Fig. 16).

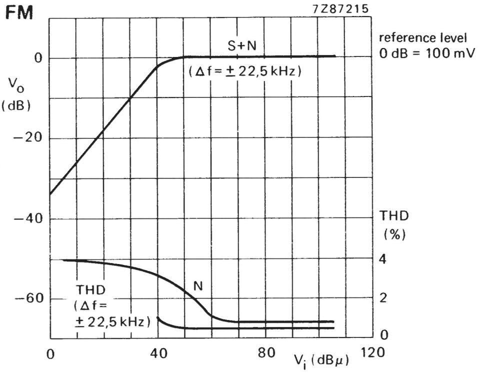
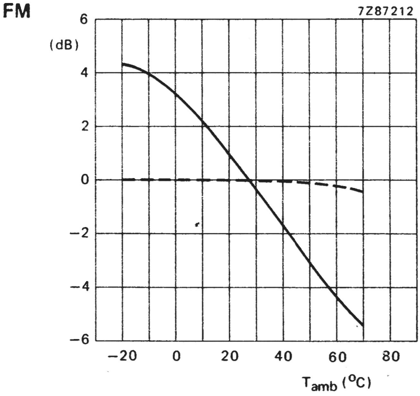


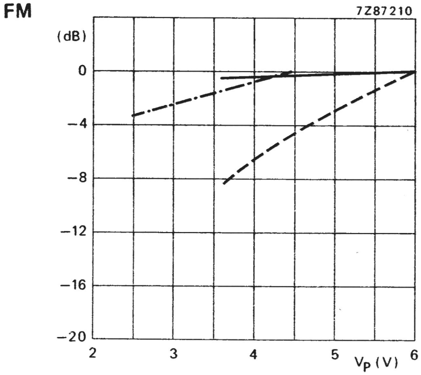
Fig. 6 Signal, noise and distortion as a function of input voltage (V_i). Measured at f_i = 10,7 MHz in test circuit Fig. 10.



——— sensitivity at −3 dB limiting.

– – – – output voltage (V_o) at V_i = 1 mV; Δf = ± 22 kHz.

Fig. 7 Sensitivity (V_i), output voltage (V_o) as a function of temperature behaviour (T_{amb}). Measured at f_i = 10,7 MHz in test circuit Fig. 10.



——— sensitivity at −3 dB limiting: V_P = 6,0 V application.

–·–·– sensitivity at −3 dB limiting: V_P = 4,5 V application.

– – – – output voltage (V_o) at V_i = 1 mV; Δf = ± 22,5 kHz.

Fig. 8 Sensitivity (V_i) and output voltage (V_o) as a function of supply voltage (V_P). Measured at f_i = 10,7 MHz in test circuit Fig. 10.

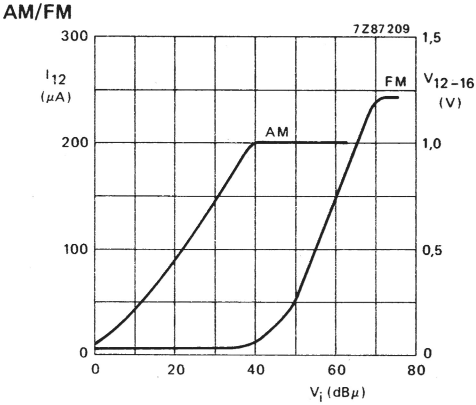


Fig. 9 Indicator output current (I_{12}) and d.c. output voltage ($V_{12\text{-}16}$): AM f_i = 1 MHz; FM f_i = 10,7 MHz as a function of input voltage (V_i). Measured in Fig. 10; V_P = 6 V; $R_{12\text{-}16}$ = 5 kΩ.

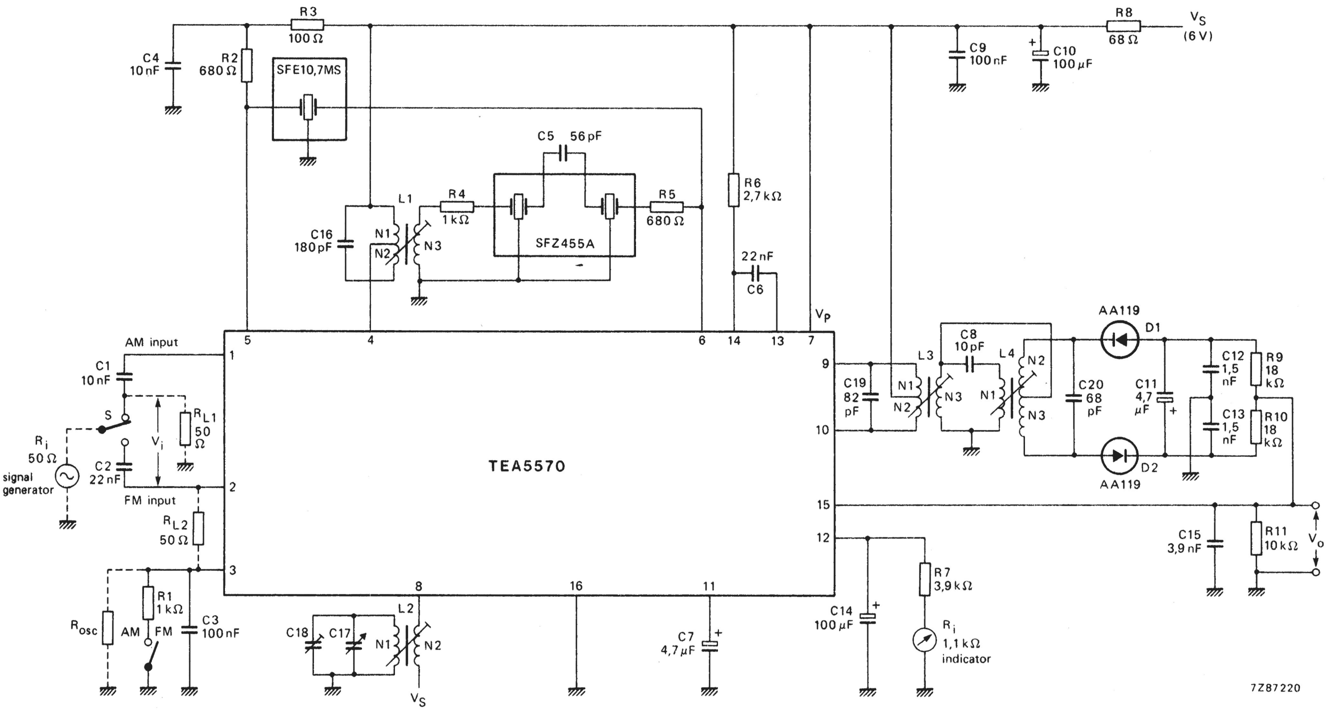

R3
100 Ω
R8
68 Ω
V_S
(6 V)
C4
10 nF
R2
680 Ω
SFE10,7MS
C9
100 nF
C10
100 µF
C5 56 pF
R6
2,7 kΩ
L1
R4
1 kΩ
R5
680 Ω
C16
180 pF
N1
N2
N3
SFZ455A
22 nF
C6
V_P
AA119
D1
AM input
C1
10 nF
S
R_{L1}
50 Ω
V_i
R_i
50 Ω
signal generator
C2
22 nF
FM input
R_{L2}
50 Ω
TEA5570
5
4
6
14
13
7
1
2
3
9
10
15
12
8
16
11
C8
10 pF
L3
L4
C19
82 pF
C20
68 pF
C11
4,7 µF
C12
1,5 nF
C13
1,5 nF
R9
18 kΩ
R10
18 kΩ
D2
AA119
C15
3,9 nF
R11
10 kΩ
V_o
R1
1 kΩ
R_{osc}
AM
FM
C3
100 nF
C18
C17
L2
V_S
C7
4,7 µF
C14
100 µF
R7
3,9 kΩ
R_i
1,1 kΩ
indicator
7Z87220

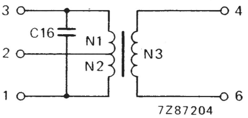
Fig. 10 Test circuit.

Coil data

The transfer impedance of the i.f. filter is:
AM: $|Z_{tr}| = v_6/i_4 =$ 2,7 kΩ (SFZ 455A).
FM: $|Z_{tr}| = v_6/i_5 = 275\ \Omega$ (SFE 10,7 MS).
See also Figs 11, 12, 13 and 14.

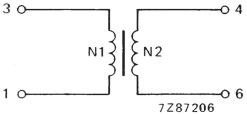
COIL DATA

AM i.f. coils (Fig. 10)


3
2
1
C16
N1
N2
N3
4
6
7Z87204

N1 = 73
N2 = 73
N3 = 9
C16 = 180 pF (internal)
Wire = 0,07 mm dia.

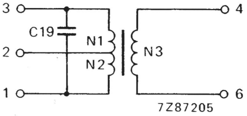
Fig. 11 I.F. bandpass filter (L1). TOKO sample no. 7 MC-7 P.


3
1
N1
N2
4
6
7Z87206

N1 = 90
N2 = 7
Wire = 0,07 mm dia.

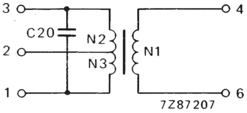
Fig. 12 Oscillator coil (L2). TOKO sample no. 7 BR-7 P.

FM i.f. coils (Fig. 10)


3
2
1
C19
N1
N2
N3
4
6
7Z87205

N1 = 5
N2 = 5
N3 = 4
C19 = 82 pF (internal)
Wire = 0,1 mm dia.

Fig. 13 Primary ratio detector coil (L3). TOKO sample no. 119 AN-7 P.

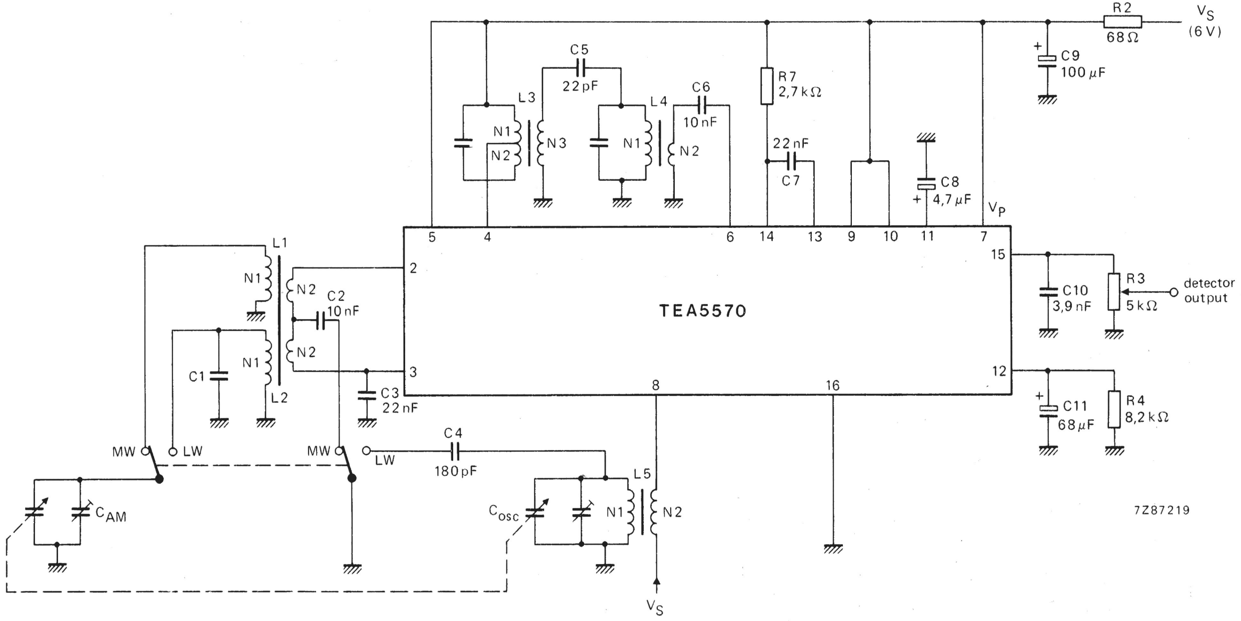

3
2
1
C20
N2
N3
N1
4
6
7Z87207

N1 = 2
N2 = 6
N3 = 6
C20 = 68 pF (internal)
Wire = 0,1 mm dia.

Fig. 14 Secondary ratio detector coil (L4). TOKO sample no. 119 AN-7 P.

APPLICATION INFORMATION

Figs 15 and 17 show the circuit diagrams for the application of 6 V AM MW/LW and 4,5 V AM/FM channels respectively, using the TEA5570. Fig. 16 shows the circuitry of the TEA5570.


R2
68 Ω
V_S
(6 V)
C9
100 μF
C5
22 pF
L3
N1
N2
N3
L4
N1
N2
C6
10 nF
R7
2,7 kΩ
22 nF
C7
C8
4,7 μF
V_P
5
4
6
14
13
9
10
11
7
15
2
3
12
8
16
TEA5570
L1
N1
N2
C2
10 nF
N2
N1
L2
C1
C3
22 nF
C10
3,9 nF
R3
5 kΩ
detector output
C11
68 μF
R4
8,2 kΩ
MW
LW
MW
LW
C4
180 pF
L5
N1
N2
C_{AM}
C_{osc}
V_S
7Z87219

Coil data

L3 N1 = 73
N2 = 73
N3 = 9
C = 180 pF

L4 N1 = 146
N2 = 9
C = 180 pF

L5 N1 = 90
N2 = 6

Fig. 15 Typical application circuit for 6 V AM MW/LW reception using the TEA5570.

APPLICATION INFORMATION (continued)

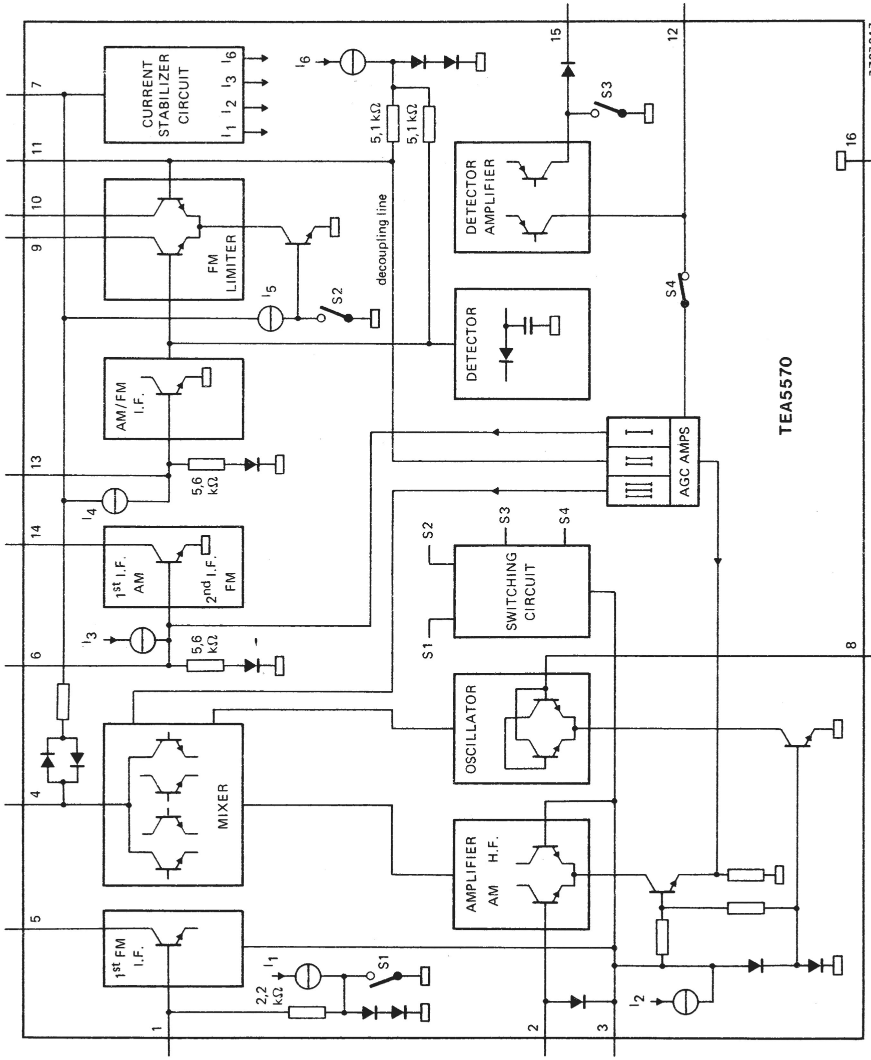
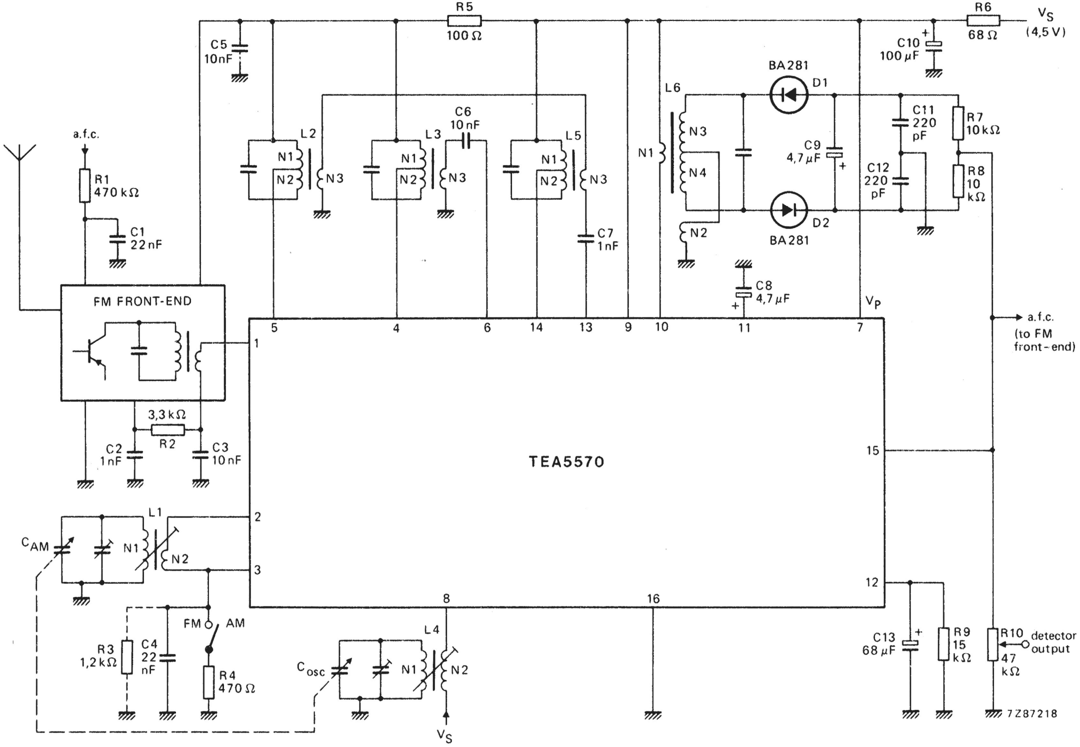

CURRENT STABILIZER CIRCUIT
I_1 I_2 I_3 I_6
I_6
5,1 kΩ
5,1 kΩ
decoupling line
FM LIMITER
I_5
S2
AM/FM I.F.
I_4
5,6 kΩ
1^{st} I.F. AM
2^{nd} I.F. FM
I_3
5,6 kΩ
MIXER
1^{st} FM I.F.
I_1
S1
2,2 kΩ
DETECTOR
DETECTOR AMPLIFIER
S3
S4
AGC AMPS
I II III
SWITCHING CIRCUIT
S1 S2 S3 S4
OSCILLATOR
AMPLIFIER AM H.F.
I_2
TEA5570
7Z87217
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

Fig. 16 TEA5570 circuit diagram.


R5
100 Ω
R6
68 Ω
V_S
(4,5 V)
C5
10nF
C10
100 μF
BA281
D1
L6
L2
N1
N2
N3
L3
C6
10 nF
L5
C7
1nF
C9
4,7 μF
C11
220
pF
C12
220
pF
R7
10 kΩ
R8
10
kΩ
N4
D2
BA281
a.f.c.
R1
470 kΩ
C1
22 nF
C8
4,7 μF
V_P
a.f.c.
(to FM
front-end)
FM FRONT-END
3,3 kΩ
R2
C2
1 nF
C3
10 nF
TEA5570
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
L1
C_{AM}
FM
AM
R3
1,2 kΩ
C4
22
nF
R4
470 Ω
C_{osc}
L4
C13
68 μF
R9
15
kΩ
R10
47
kΩ
detector
output
7Z87218

Coil data

	L2	L3	L4	L5	L6
N1	3	33	90	33	50
N2	8	113	6	113	50
N3	1	9		9	4,5
N4					6,5
C	82 pF	180 pF			82 pF

Fig. 17 Typical application circuit for 4,5 V AM/FM reception using the TEA5570 with coils and single-tuned ratio detector (with silicon diodes).

DETAILED APPLICATION INFORMATION WILL BE SUPPLIED ON REQUEST.

PLL STEREO DECODER

The TEA5580 is a PLL stereo decoder. It is suitable for portable radios, radio recorders, medium-fi and car radio receivers. The circuit incorporates the following functions.

- A **voltage-controlled oscillator** (f = 228 kHz) from which the 19, 38, 57 and 114 kHz signals are obtained via I^2L logic.
- A **phase-locked-loop system** to lock the VCO to the 19 kHz pilot tone in the stereo signal. The phase detector in the loop system also suppresses phase distortion due to the 57 kHz pilot signal from VWF transmitters (traffic warning system in Germany).
- **A pilot presence detector and an automatic mono/stereo switch.**
- **Two demodulators**, one driven by the 38 kHz decoding signal for the stereo matrix, the second driven by a 114 kHz signal which suppresses the third harmonic of the multiplex signal (MUX). These prevent distortion caused by strong adjacent transmitters.
- **A matrix and two output buffers**, for the left and right output signals.
- **An input amplifier**, the gain of which can be adjusted by the external input resistor.
- **A pilot cancelling circuit**, for extra suppression of the pilot signal.
- **An SDS circuit (signal dependent stereo)** for a smooth changeover from stereo to mono on weak signals.
- **A driver output stage** for a stereo LED indicator.
- **A stabilizer**, for operation over a wide supply voltage range.

The stereo decoder is compensated for a typical i.f. filter with a roll-off frequency of 50 kHz (2 dB down at 38 kHz).

QUICK REFERENCE DATA

Applicable supply voltage range	V_S		3,6 to 16	V
Supply voltage (pin 9)	V_P	nom.	6	V
Ambient temperature	T_{amb}	typ.	25	°C
Total quiescent current	I_{tot}	typ.	10	mA
Measured at $V_{i(p-p)} = 1$ V (MUX with 27 mV pilot)				
Overall gain	G_o	typ.	0 to 20	dB
Output channel unbalance	V_{1-5}/V_{2-5}	$<$	± 1	dB
Output voltage (r.m.s. value)	V_{1-5}/V_{2-5}	typ.	0,4	V
Total harmonic distortion (300 Hz to 20 kHz)	THD	typ.	0,2	%
Signal-to-noise ratio, DIN A-curve	S/N	typ.	80	dB
Channel separation	α	typ.	40	dB
Carrier suppression at: f = 19 kHz (adjusted)	α_{19}	typ.	50	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

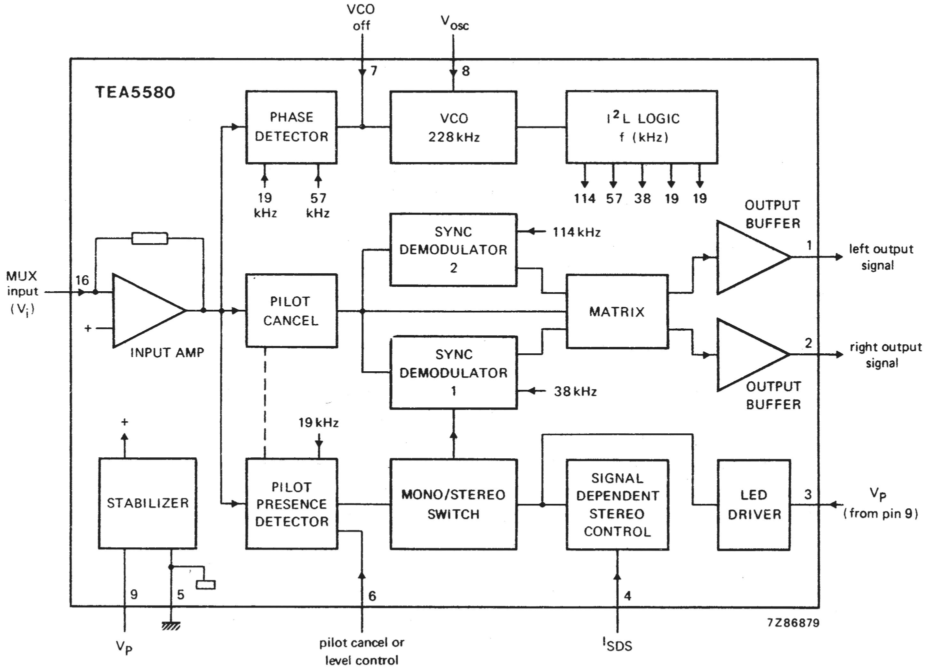

VCO off
Vosc
7
8
TEA5580
PHASE DETECTOR
VCO 228 kHz
I²L LOGIC f (kHz)
114 57 38 19 19
19 kHz
57 kHz
OUTPUT BUFFER
SYNC DEMODULATOR 2
114 kHz
1
left output signal
MUX input (Vi)
16
+
INPUT AMP
PILOT CANCEL
MATRIX
SYNC DEMODULATOR 1
38 kHz
2
right output signal
OUTPUT BUFFER
+
19 kHz
STABILIZER
PILOT PRESENCE DETECTOR
MONO/STEREO SWITCH
SIGNAL DEPENDENT STEREO CONTROL
LED DRIVER
3
VP (from pin 9)
9
5
6
4
VP
pilot cancel or level control
ISDS
7Z86879

Fig. 1 Block diagram.

DEVELOPMENT SAMPLE DATA

A.C. CHARACTERISTICS

Measured in circuit of Fig. 2 at $V_P = 6$ V, $V_{i(p\text{-}p)} = 1$ V (MUX with 27 mV pilot)

Input impedance (external)	$\lvert Z_i \rvert$	typ.	47	kΩ
Output impedance (external)	$\lvert Z_o \rvert$	typ.	5,1	kΩ
Output voltage (r.m.s. value)	$V_{o(rms)}$	typ.	400	mV
Total harmonic distortion (300 Hz to 10 kHz) (mono, stereo and mono + pilot)	THD	typ.	0,2	%
Total harmonic distortion at $V_{o(rms)} = 0,6$ V	THD	<	1	%
Signal-to-noise ratio (DIN A-curve)	S/N	typ.	80	dB
Channel separation (for L = 1 and R = 0)	α	typ.	40	dB
SDS control				
10 dB channel separation	I_4	typ.	50	μA
full stereo (channel separation ⩾ 26 dB)	I_4	>	100	μA
full mono (channel separation ⩽ 1 dB)	I_4	<	10	μA
Stereo/mono switch (for R2 = ▲kΩ)				
for switching to stereo	V_i	<	18	mV
for switching to mono	V_i	> typ.	5 13	mV mV
hysteresis	ΔV_i	typ.	2,5	dB
VCO frequency (adjustable)	f_{VCO}	typ.	228	kHz
Capture range (deviation from 228 kHz centre frequency) $V_{pilot} = 32$ mV		typ.	3,5	%
Temperature coefficient (uncompensated)	TC	typ.	▲	kHz/K
VCO off switching voltage (pin 7)	V_{off}	>	3	V
Carrier suppression (adjusted by R2) at:				
f = 19 kHz	α_{19}	typ.	50	dB
f = 38 kHz	α_{38}	typ.	50	dB
f = 228 kHz	α_{228}	typ.	70	dB
ACI suppression at: *				
f = 114 kHz	α_{114}	typ.	80	dB
f = 190 kHz	α_{190}	typ.	60	dB
SCA suppression at f = 67 kHz	α_{67}	typ.	66	dB
VWF suppression**	α_{VWF}	typ.	70	dB
Ripple rejection at f = 100 Hz				
$V_S = 3,6$ V	RR	typ.	20	dB
$V_S = 8$ V	RR	typ.	26	dB

* ACI suppression: $\alpha_{114} = 20 \log \frac{V_o \text{ (at 1 kHz)}}{V_o \text{ (at 4 kHz)}}$.

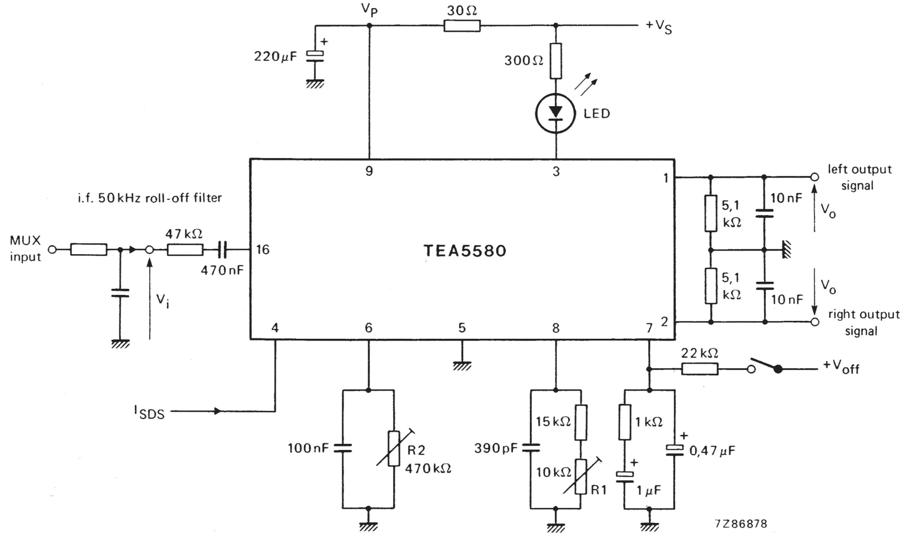
90% S-signal (L = –R, f_m = 1 kHz); 9% pilot signal; 1% spurious signal (f = 110 kHz).

** VWF suppression: $\alpha_{VWF} = 20 \log \frac{V_o \text{ (at 1 kHz + 23 Hz)}}{V_o \text{ (at 1 kHz)}}$.

90% S-signal (L = –R, f_m = 1 kHz); 9% pilot signal; 5% VWF signal (f = 57 kHz, f_m = 23 Hz AM, m = 60%).

▲ Value to be established.

APPLICATION INFORMATION



V_P
30Ω
+V_S
220µF
300Ω
LED
9
3
1
left output signal
i.f. 50kHz roll-off filter
5,1 kΩ
10nF
V_o
MUX input
47kΩ
16
TEA5580
470nF
V_i
5,1 kΩ
10nF
V_o
right output signal
4
6
5
8
7
2
22kΩ
+V_{off}
I_{SDS}
15kΩ
1kΩ
100nF
R2
470kΩ
390pF
10kΩ
R1
0,47µF
1µF
7Z86878

Fig. 2 Test and application diagram.

Notes

R1: VCO frequency adjustment; f = 228 kHz.
R2: pilot cancelling and pilot level.

FM/IF SYSTEM AND MICROCOMPUTER-BASED TUNING INTERFACE

GENERAL DESCRIPTION

The TEA6000 is a monolithic integrated FM/IF system circuit intended for microcomputer controlled radio receivers. The circuit includes an AM/FM-IF counter and an analogue-to-digital interface. The i.f. counter generates AM/FM precision tuning and accurate stop information.

Features

- Three-stage i.f. limiting amplifier with separate AM and FM inputs, to drive the ratio detector and counter stage
- Two-stage level detector with high field-strength dependent d.c. output current and multi-path dependent a.c. output current
- Operational amplifier for active filtering (e.g. multi-path detector)
- High resolution frequency counter for AM and FM-IF signals
- External timebase reference (SAA1057) or internal crystal-controlled oscillator
- 3-bit analogue-to-digital (A/D) converter for two input signals (multi-path and field-strength) with software controlled sensitivity
- I^2C bus slave transceiver

QUICK REFERENCE DATA (at T_{amb} = 25 °C)

Supply voltage				
logic part (pin 2)	$V_{P1} = V_{2\text{-}1}$	typ.	8,4	V
i.f. part (pin 12)	$V_{P2} = V_{12\text{-}10}$	typ.	8,4	V
Sensitivity				
FM (limiting sensitivity −3 dB)		typ.	150	μV
frequency counter (AM and FM)		typ.	100	μV
A/D converter		typ.	2 or 6	V*
Ratio detector output voltage				
at Δf = 22,5 kHz; f_m = 1 kHz		typ.	200	mV
Level detector output voltage (pin 13)	$V_{13\text{-}10}$	max.	7	V
Resolution frequency counter				
AM		typ.	250	Hz
FM		typ.	6,4	kHz
Reference frequency		typ.	32 or 40	kHz
Gain operational amplifier		typ.	10^4	

* Full scale.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102HE).

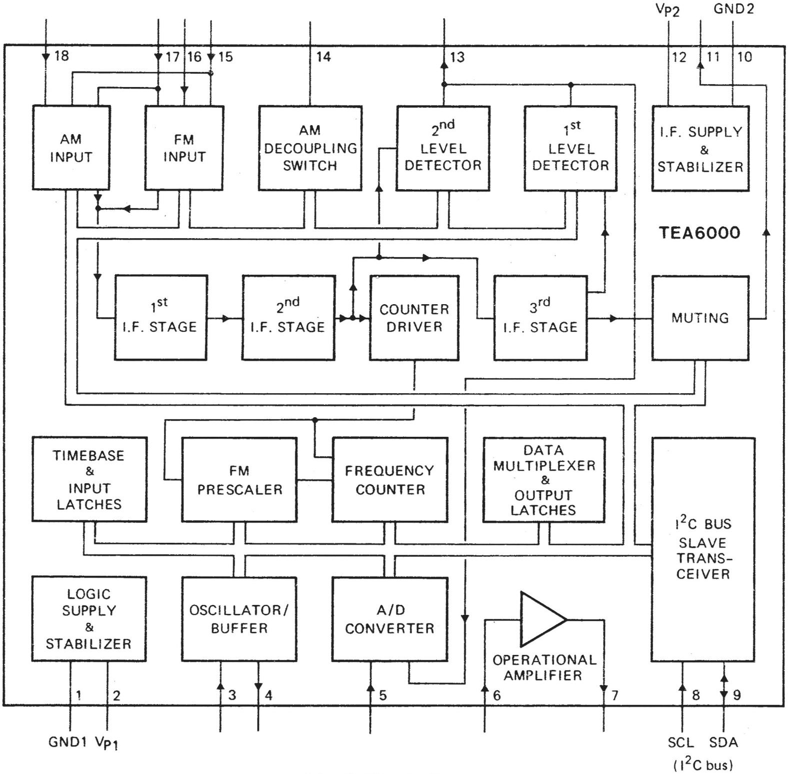

VP2
GND2
18
17
16
15
14
13
12
11
10
AM INPUT
FM INPUT
AM DECOUPLING SWITCH
2nd LEVEL DETECTOR
1st LEVEL DETECTOR
I.F. SUPPLY & STABILIZER
TEA6000
1st I.F. STAGE
2nd I.F. STAGE
COUNTER DRIVER
3rd I.F. STAGE
MUTING
TIMEBASE & INPUT LATCHES
FM PRESCALER
FREQUENCY COUNTER
DATA MULTIPLEXER & OUTPUT LATCHES
I2C BUS SLAVE TRANS- CEIVER
LOGIC SUPPLY & STABILIZER
OSCILLATOR/ BUFFER
A/D CONVERTER
OPERATIONAL AMPLIFIER
1
2
3
4
5
6
7
8
9
GND1
VP1
SCL
SDA
(I2C bus)

Fig. 1 Block diagram.

7Z89921

PINNING

1	ground 1 (GND1); logic part
2	positive supply 1 (V_{P1}); logic part
3	oscillator/buffer input
4	oscillator feedback
5	A/D multi-path input
6	operational amplifier input
7	operational amplifier output
8	serial clock line (SCL)
9	serial data line (SDA)
10	ground 2 (GND2); i.f. part
11	i.f. output
12	positive supply 2 (V_{P2}); i.f. part
13	level detector output
14	level detector decoupling
15	d.c. feedback input stage
16	FM input
17	d.c. feedback decoupling
18	AM input

BIPOLAR ICs FOR RADIO AND AUDIO EQUIPMENT

FUNCTIONAL AND NUMERICAL INDEX
MAINTENANCE TYPE LIST

GENERAL

PACKAGE OUTLINES

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